

STB75NF75L

N-channel 75V - 0.009Ω - 75A - D²PAK STripFET™ II Power MOSFET

Features

Туре	V _{DSS}	R _{DS(on)}	I _D
STB75NF75L	75V	<0.011Ω	75A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Applications

■ Switching applications

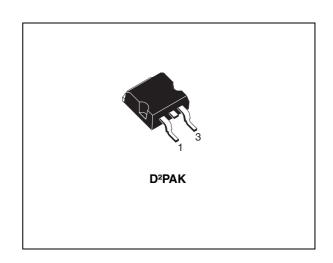


Figure 1. Internal schematic diagram

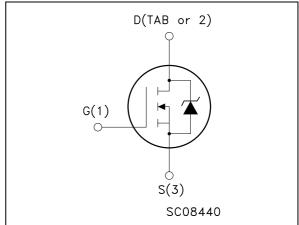


Table 1. Device summary

Order code	Marking	Package	Packaging
STB75NF75LT4	STB75NF75LT4 B75NF75L		Tape & reel

Contents STB75NF75L

Contents

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STB75NF75L Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V _{GS} = 0)	75	V
V _{GS}	Gate-source voltage	± 15	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25°C	75	Α
I _D Drain current (continuous) at T _C = 100°C		70	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	300	Α
P _{TOT}	Total dissipation at T _C = 25°C	300	W
	Derating factor	2	W/°C
dv/dt ⁽³⁾ Peak diode recovery voltage slope		10	V/ns
E _{AS} ⁽⁴⁾ Single pulse avalanche energy		680	mJ
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

- 1. Current limited by package
- 2. Pulse width limited by safe operating area
- 3. $I_{SD} \le 75A$, di/dt $\le 500A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX}$
- 4. Starting $T_J = 25$ °C, $I_D = 37.5A$, $V_{DD} = 30V$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance junction-case Max	0.5	°C/W
R _{thJA}	Thermal resistance junction-ambient Max	62.5	°C/W
T _I	Maximum lead temperature for soldering purpose	300	°C

Electrical characteristics STB75NF75L

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS} Drain-source breakdown voltage		$I_D = 250\mu A, V_{GS} = 0$	75			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	$V_{DS} = Max rating,$ $V_{DS} = Max rating @ 125°C$			1 10	μ Α μ Α
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±15V			±100	nA
V _{GS(th)} Gate threshold voltage		$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		2.5	V
R _{DS(on)}	Static drain-source on resistance	V_{GS} = 10V, I_{D} = 37.5A V_{GS} = 5V, I_{D} = 37.5A		0.009 0.010	0.011 0.013	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	$V_{DS} = 15V, I_D = 37.5A$		120		S
C _{iss} Input capacitance C _{oss} Output capacitance C _{rss} Reverse transfer capacitance		V _{DS} =25V, f = 1 MHz, V _{GS} = 0		4300 660 205		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 60V$, $I_D = 75A$ $V_{GS} = 5V$ see Figure 15		75 18 31	90	nC nC nC

^{1.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$\begin{array}{c} t_{\rm d(on)} \\ t_{\rm r} \\ t_{\rm d(off)} \\ t_{\rm f} \end{array}$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 40V$, $I_D = 37.5A$, $R_G = 4.7\Omega$, $V_{GS} = 4.5V$ see Figure 14		35 155 110 60		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				75	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				300	Α
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 75A, V_{GS} = 0$			1.3	٧
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 75A, di/dt = 100A/ μ s, V_{DD} = 24V, T_{J} = 150°C see <i>Figure 16</i>		120 500 9		ns nC A

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Electrical characteristics STB75NF75L

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

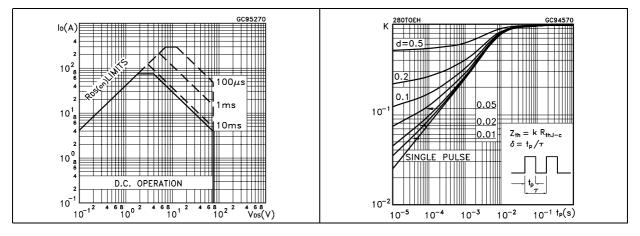


Figure 4. Output characteristics

Figure 5. Transfer characteristics

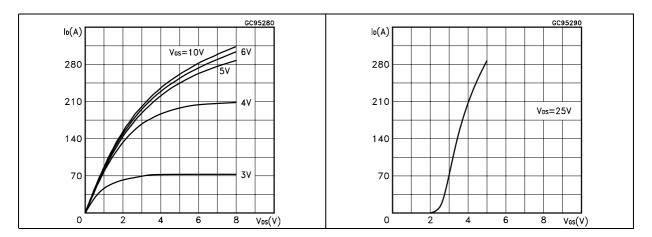
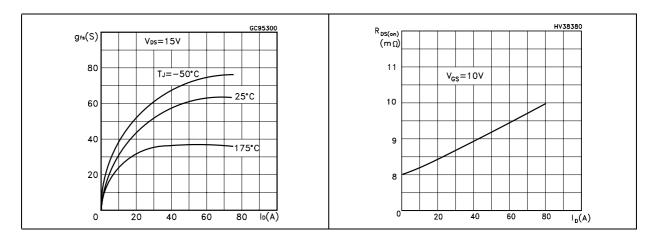


Figure 6. Transconductance

Figure 7. Static drain-source on resistance



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Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

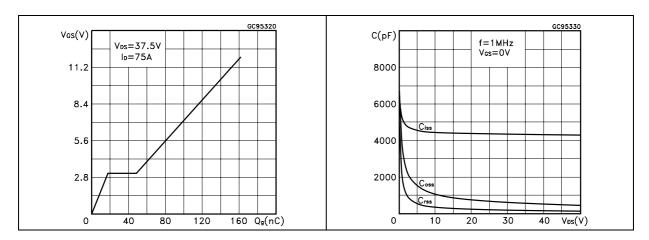


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

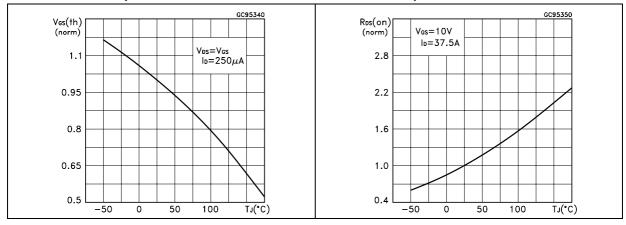
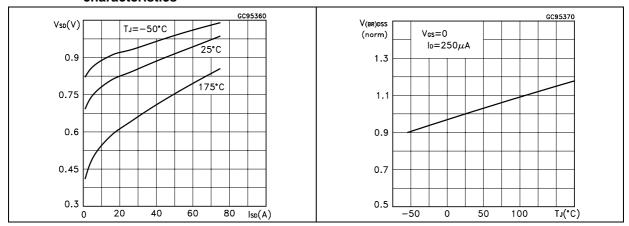


Figure 12. Source-drain diode forward characteristics

Figure 13. Normalized B_{VDSS} vs temperature



Test circuit STB75NF75L

3 Test circuit

Figure 14. Switching times test circuit for resistive load

Figure 15. Gate charge test circuit

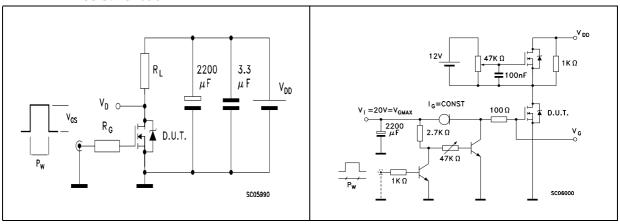


Figure 16. Test circuit for inductive load switching and diode recovery times

Figure 17. Unclamped Inductive load test circuit

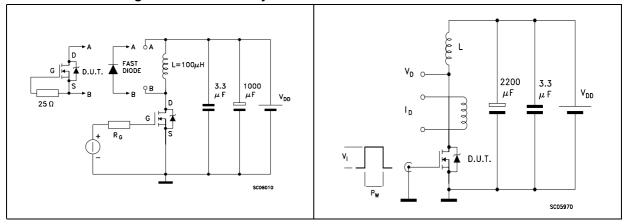
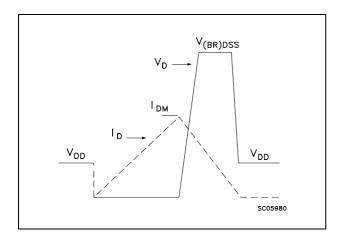


Figure 18. Unclamped inductive waveform



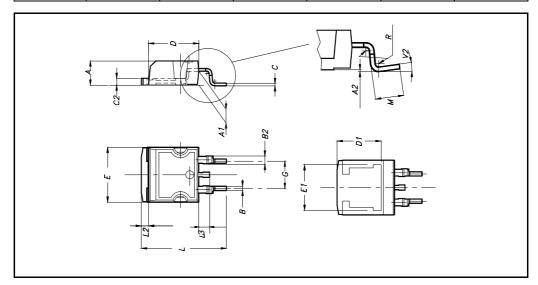
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4 Package mechanical data

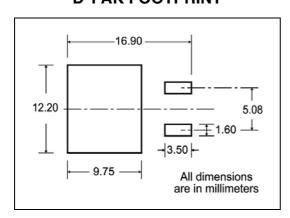
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

D²PAK MECHANICAL DATA

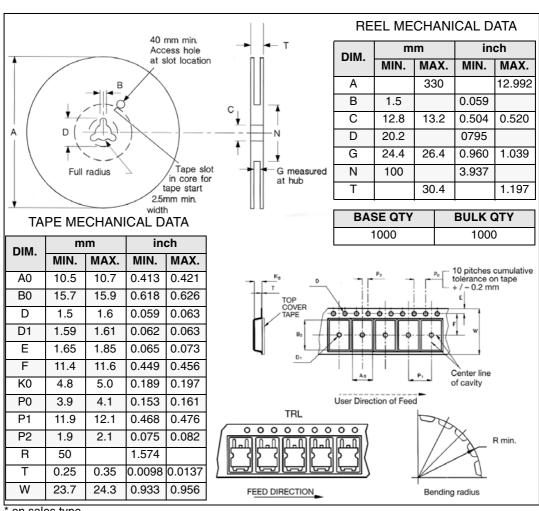
DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
В	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
С	0.45		0.6 0.017	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
М	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0 ₀		4º			



5 Packaging mechanical data D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



Revision history STB75NF75L

6 Revision history

Table 8. Revision history

	Date	Revision	Changes
	21-Jun-2004	1	First release
	02-Oct-2006	2	New template, no content change
Ī	13-Jul-2007	3	New updates on <i>Table 7</i>

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