TS4601

High performance stereo headphone amplifier with capacitorless outputs and I²C bus interface

Features

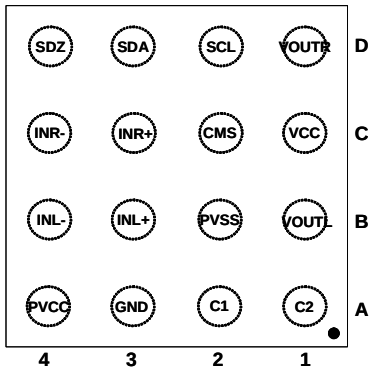
- Power supply range: 2.9 V to 5.5 V
- 107 dB of PSRR at 217 Hz
- Fully differential inputs
- I²C interface for volume control
- Digital volume control range from -60 dB to +4 dB
- 101 dB of SNR A-weighted
- Independent right and left channel shutdown control
- Low quiescent current: 4.8 mA typ. at 3.0 V
- Low standby current: 2 µA max
- Output-coupling capacitors removed
- Flip-chip package 2.1 mm x 2.1 mm, 500 µm pitch, 16 bumps

Applications

- Cellular phones
- Notebook computers
- CD/MP3 players

TS4601EIJT - Flip-chip

Pinout (top view)



Balls are underneath

Description

The TS4601 is a stereo headphone driver dedicated to high audio performance and space-constrained applications.

It is based on low power dissipation amplifier core technology. Special care was taken in the design of the amplification chain to achieve peerless PSRR (107 dB typ. at 217 Hz) and 101 dB of SNR.

The TS4601 can drive 0.9 V_{rms} output voltage into 16 Ω and 1.6 V_{rms} into 10 kΩ, whatever the power supply voltage, in the 2.9 V to 5.5 V range.

An I²C interface offers volume control in 64 steps from -60 dB to +4 dB and multiple configuration modes for the device.

The traditionally used output-coupling capacitors can be removed and a dedicated common-mode sense pin removes parasitic noise from the jack.

The TS4601 is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads.

The TS4601 is packaged in a tiny 16-bump flip-chip with a pitch of 500 µm and a 300 µm diameter ball size.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{in}	Input voltage In Master standby mode, and I²C1, 6 and 7 In I²C 2, 3, 4 and 5	 0 to V_{CC} -2.4 to +2.4	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (2)	200	°C/W
P_d	Power dissipation	Internally limited(3)	
ESD	HBM - human body model(4)	2	kV
	MM - machine model (min. value)(5)	200	V
Latch-up	Latch-up immunity	200	mA
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The device is protected in case of over temperature by a thermal shutdown active @ 150° C.
3. Exceeding the power derating curves during a long period may provoke abnormal operation.
4. Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
5. Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.9 to 5.5	V
R_L	Load resistor	≥ 16	Ω
C_L	Load capacitor Serial resistor of 12Ω minimum, R_L ≥ 16Ω,	0.8 to 100	nF
T_{oper}	Operating free air temperature range	-40 to +85	°C
R_{thja}	Flip-chip thermal resistance junction to ambient	90	°C/W

2 Typical application schematics

Figure 1. Typical application schematics for the TS4601

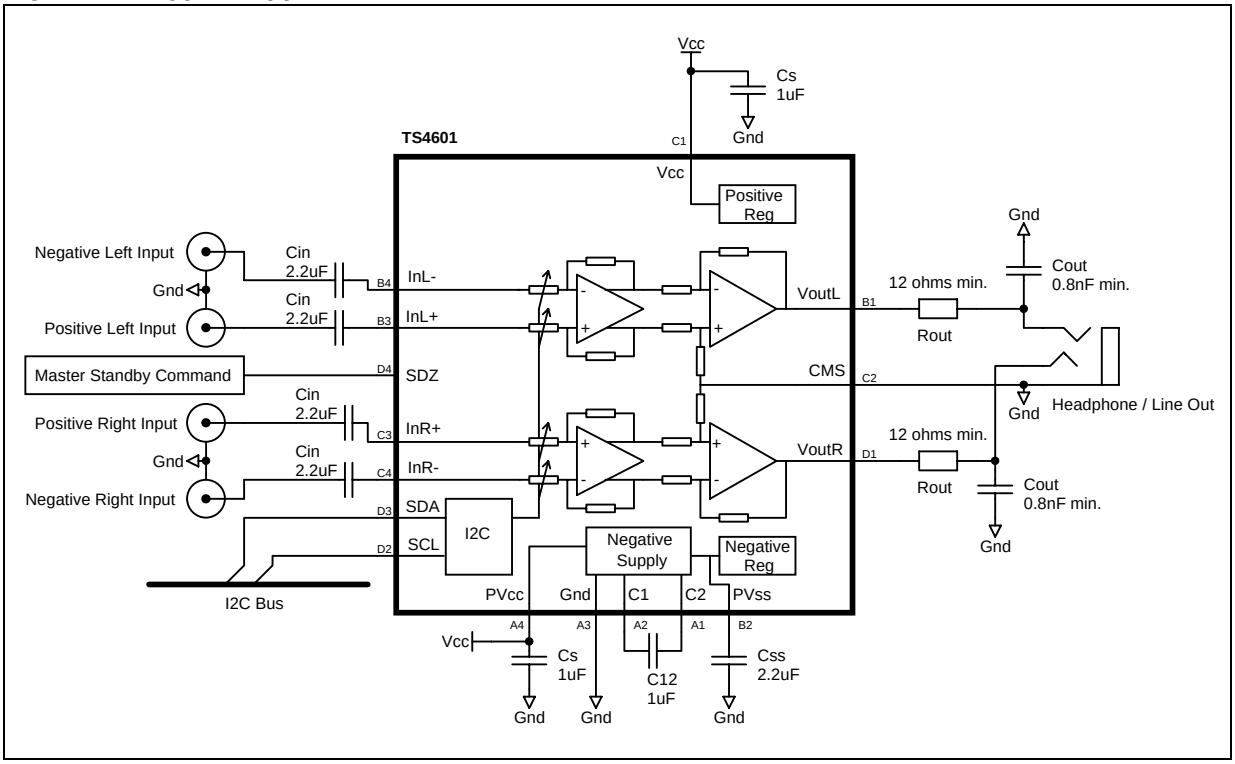


Table 3. Pin description for the TS4601

Pin number	Pin name	Pin definition
C1	VCC	Analog supply voltage, connect to $V_{battery}$.
A4	PVCC	Power supply voltage, connect to $V_{battery}$.
A2	C1	Capacitor terminal for internal negative supply generator.
A1	C2	Capacitor terminal for internal negative supply generator.
B2	PVSS	Capacitor terminal for internal negative supply generator filtering.
D1	VOUTR	Right audio channel output signal.
B1	VOUTL	Left audio channel output signal.
A3	GND	Ground of the device.
C2	CMS	Common-mode sense, to be connected as close as possible to the ground of headphone / line out plug.
B4	INL-	Left audio channel negative input signal.
B3	INL+	Left audio channel positive input signal.
D4	SDZ	Master standby of the circuit. When SDZ = 0, the device is also reset to initial state. Up to V_{CC} tolerant input.
C4	INR-	Right audio channel negative input signal.

Table 3. Pin description for the TS4601 (continued)

Pin number	Pin name	Pin definition
C3	INR+	Right audio channel positive input signal.
D3	SDA	I²C signal data. Up to V_{CC} tolerant input.
D2	SCL	I²C clock signal. Up to V_{CC} tolerant input.

Table 4. Component description for the TS4601

Component	Value	Description
Cs	1µF	Decoupling capacitors for V_{CC} and PV_{CC}. Two 1µF capacitors are enough for proper decoupling of TS4601. X5R dielectric and 10V rating voltage is recommended to minimize $\Delta C/\Delta V$ when V_{CC}= 5V. Must be placed as close as possible to the TS4601 to minimize parasitic inductance and resistance.
C12	1µF	Capacitor for internal negative power supply operation. X5R dielectric and 10V rating voltage is recommended to minimize $\Delta C/\Delta V$ when V_{CC}= 5V. Must be placed as close as possible to the TS4601 to minimize parasitic inductance and resistance.
C_{SS}	2.2µF	Filtering capacitor for internal negative power supply. X5R dielectric and 10V rating voltage is recommended to minimize $\Delta C/\Delta V$ when V_{CC} = 5V.
C_{in}	$Cin = \frac{1}{2\pi ZinFc}$	Input coupling capacitor that forms with Z_{in}, a first order high pass filter with a -3dB cut-off frequency F_C. Z_{in} is 12kΩ typical and independent of the gain setting. For example F_C = 13Hz, C_{in} = 1µF and for F_C = 6Hz, C_{in} = 2.2µF
C_{out}	0.8nF to 100nF	Output capacitor of 0.8nF minimum to 100nF maximum. This capacitor is mandatory for operation of the TS4601.
R_{out}	12Ω min.	Output resistor in series with the TS4601 output. This 12Ω minimum resistor is mandatory for operation of the TS4601.

3 Electrical characteristics

3.1 Electrical characteristics tables

Table 5. Electrical characteristics of the I²C interface from V_{CC}=+2.9 V to V_{CC}=+5.5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage on SDZ pins			0.63	V
V_{IH}	High level input voltage on SDZ pins	1.1			V
V_{IL}	Low level input voltage on SDA, SCL pins			0.6	V
V_{IH}	High level input voltage on SDA, SCL pins	1.3			V
F_{SCL}	I^2C clock frequency			400	kHz
V_{OL}	Low level output voltage, SDA pin, I_{sink} = 3mA			0.4	V
I_{in}	Input current on SDA, SCL from 0.4V to 4.5V			10	µA
	Pull-down resistor on SDZ	480	600	720	kΩ

Table 6. Electrical characteristics of the amplifier from V_{CC}=+2.9 V to V_{CC}=+5.5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Quiescent supply current, no input signal, both channels enabled, R_L= 16Ω V_{CC} = 3.0V V_{CC} = 5.0V		 4.8 5.6	 6 7	mA
I_{STBY}	Master standby current, No input signal V_{SDZ}= 0V V_{SDZ}= 0.35V, V_{CC}= 5V		0.5	 2 10	µA
I_{STBY}	I²C standby current, no input signal			75	µA
V_{in}	Input differential voltage range(1)			1.2	V_{rms}
V_{oo}	Output offset voltage No input signal, R_L = 32Ω	-5		+5	mV
V_{out}	Maximum output voltage, in-phase signals R_L = 16Ω, THD+N = 1% max, f = 1kHz R_L = 10kΩ, R_S=15Ω, C_L=1nF, THD+N = 1% max, f = 1kHz	 0.9 1.6			V_{rms}
Frequency range	R_L = 16Ω, G = 0dB, P_{out} = 20mW, +/- 0.5dB (related to1kHz) C_{in} = 4.7µF	10		22000	Hz
THD + N	Total harmonic distortion + noise, G = 0dB R_L = 16Ω, P_o = 5mW, F = 1kHz R_L = 16Ω, P_o = 10mW, 20Hz < F < 20kHz		 0.2	0.02	%

Table 6. Electrical characteristics of the amplifier from V_{CC}=+2.9 V to V_{CC}=+5.5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
PSRR	Power supply rejection ratio(2) F = 217Hz, R_L = 16Ω, G = 0dB V_{ripple} = 200mV_{pp}, grounded inputs F = 10kHz, R_L = 16Ω, G = 0dB V_{ripple} = 200 mV_{pp}, grounded inputs	100	107 70		dB
CMRR	Common mode rejection ratio R_L = 16Ω, F = 20Hz to 20 kHz, G = 0dB, V_{ic} = 200 mV_{pp}		65		dB
Crosstalk	Channel separation R_L = 16Ω, G = 0dB, F = 1kHz, P_o = 40mW R_L = 10kΩ, G = 0dB, F = 1kHz, V_{out} = 1.6V_{rms}	60 80	82 84		dB
SNR	Signal to noise ratio, A-weighted, R_L=16 Ω, V_{out} = 0.9V_{rms} THD+N < 1%, F = 1kHz, G=+4 dB(3)		101		dB
ONoise	Output noise voltage, A-weighted(3) G= +4dB G=-19.5dB		 -103	-100	dBV
G	Gain range with Gain(dB) = 20xlog[(V_{out}L/R)/(InL/R+ - InL/R-)]	-60		+4	dB
Mute	InL/R+ - InL/R- = 1V_{rms}			-80	dB
-	Gain step size from -60dB to -36dB from -36dB to -16.5dB from -16.5dB to +4dB		 3 1.5 0.5		dB
-	Step size error	-1		+1	stepsize
	Gain error (G = +4dB)	-0.45		+0.42	dB
Z_{in}	Left and right channel input impedance all gains setting Single-ended inputs referenced to GND Differential inputs	 10 20	 12 24	 14.5 29	kΩ
Z_{out}	Output impedance in Mode 5 (negative supply is ON and amplifier output stages are OFF)(3) F < 40kHz F = 6MHz F = 36MHz	 10 500 75			 kΩ Ω Ω
t_{wu}	Wake-up time		12	22	ms
t_{STBY}	Standby time		10		µs

1. Guaranteed by design and parameter correlation.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is an added sinus signal to V_{CC} @ F = 217 Hz.
3. Guaranteed by design and parameter correlation.

3.2 Electrical characteristic curves

Current consumption vs. power supply voltage	see *Figure 2*
Standby current consumption vs. power supply voltage	see *Figure 3* and *Figure 4*
Maximum output power vs. power supply voltage	see *Figure 5*
Maximum output power vs. power supply voltage	see *Figure 6*
Maximum output voltage vs. power supply voltage	see *Figure 7*
PSRR vs. frequency	see *Figure 8* to *Figure 12*
PSRR vs. gain setting	see *Figure 13*
THD+N vs. output power	see *Figure 14* to *Figure 25*
THD+N vs. output voltage	see *Figure 26*
THD+N vs. frequency	see *Figure 27*
THD+N vs. frequency	see *Figure 28* to *Figure 39*
CMRR vs. frequency	see *Figure 40* and *Figure 41*
Crosstalk vs. frequency	see *Figure 42* to *Figure 45*
Common mode response vs. frequency	see *Figure 46*
THD+N vs. input voltage. Line in mode 5	see *Figure 47*
Input impedance vs. frequency. Line in mode 5	see *Figure 48*
Gain vs. frequency	see *Figure 49*

Note: When the label “RC network” is present in a curve, it means that a 12 Ω+ 1 nF low pass filter connected on outputs is used (refer to Figure 1: Typical application schematics for the TS4601 on page 4).

Figure 2. Current consumption vs. power supply voltage

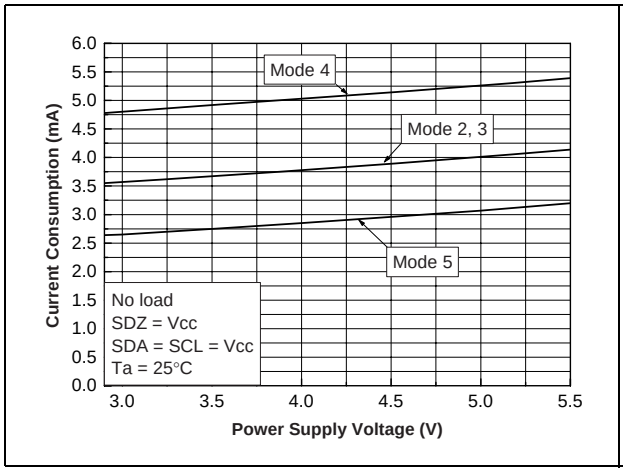


Figure 3. Standby current consumption vs. power supply voltage

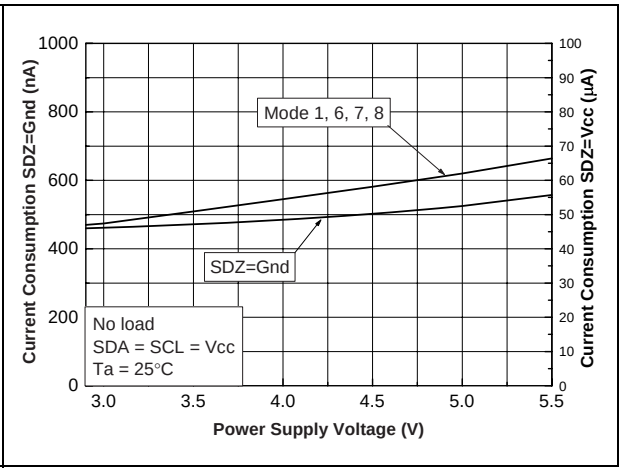


Figure 4. Standby current consumption vs. standby voltage

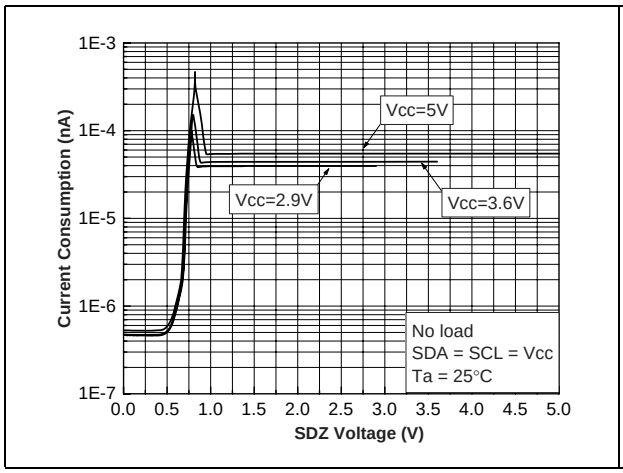


Figure 5. Maximum output power vs. power supply voltage

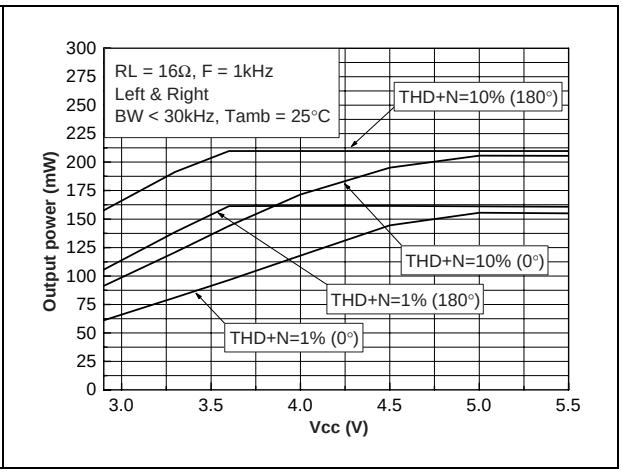


Figure 6. Maximum output power vs. power supply voltage

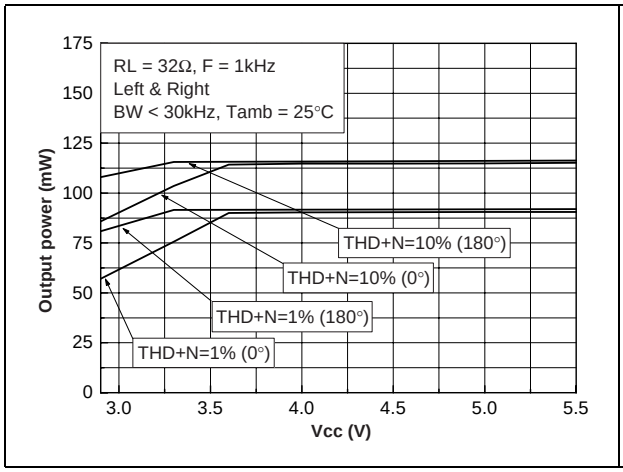


Figure 7. Maximum output voltage vs. power supply voltage

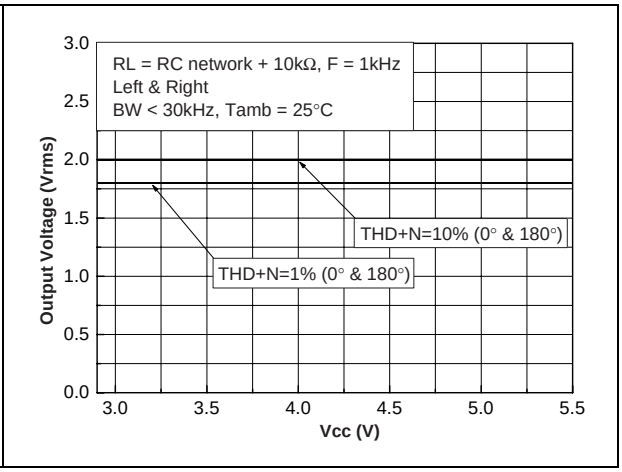


Figure 8. PSRR vs. frequency

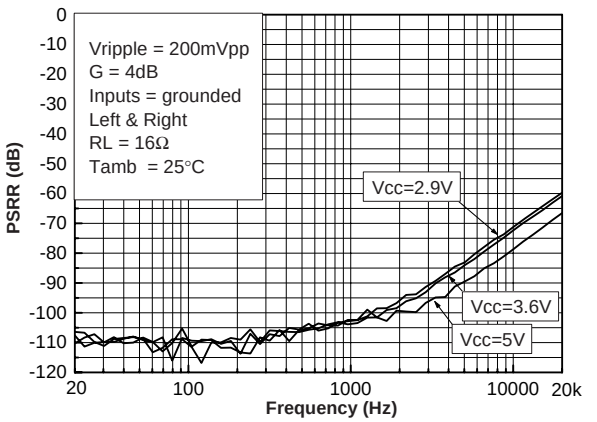


Figure 9. PSRR vs. frequency

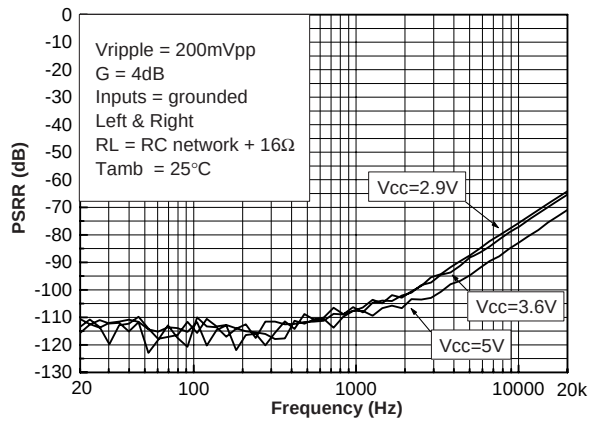


Figure 10. PSRR vs. frequency

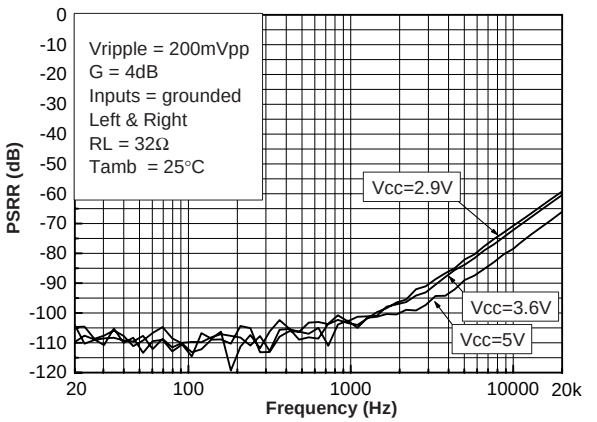


Figure 11. PSRR vs. frequency

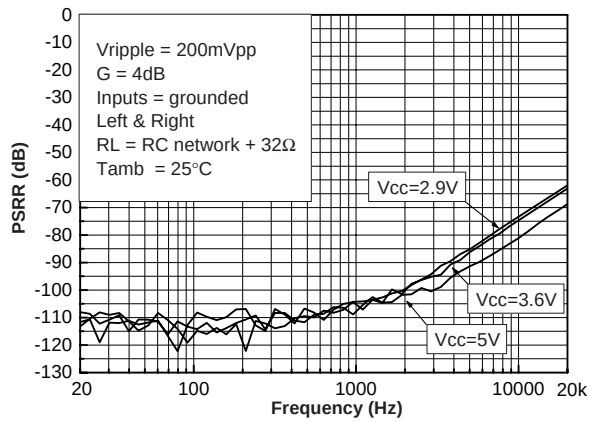


Figure 12. PSRR vs. frequency

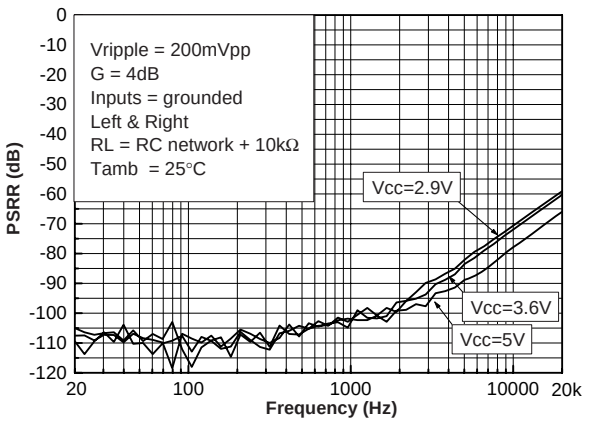


Figure 13. PSRR vs. gain setting

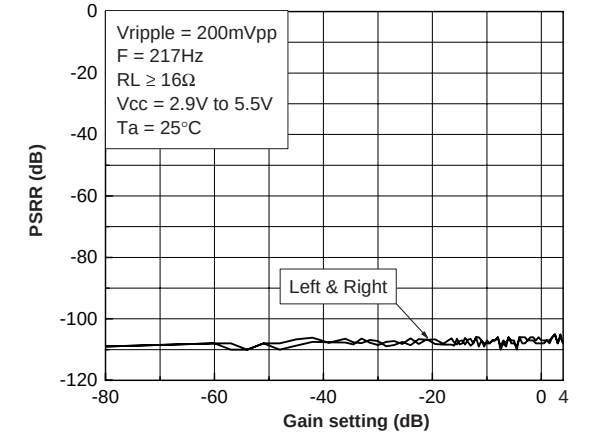


Figure 14. THD+N vs. output power

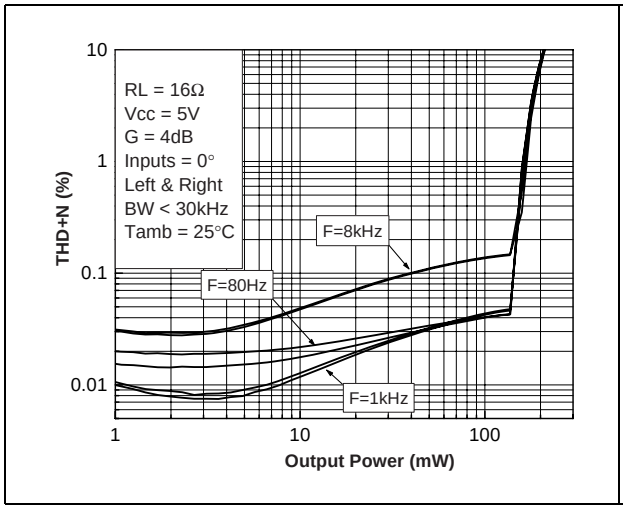


Figure 15. THD+N vs. output power

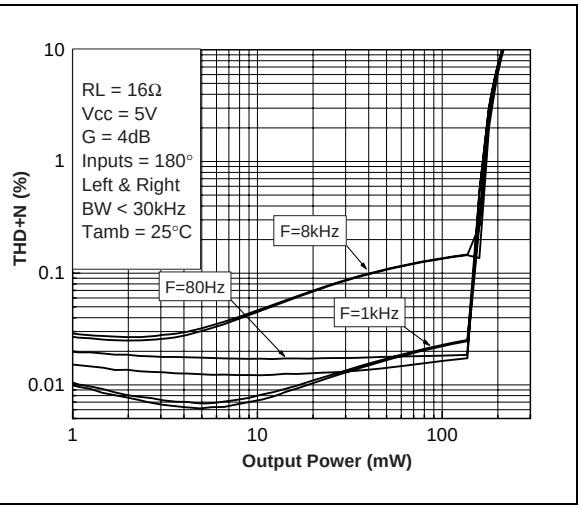


Figure 16. THD+N vs. output power

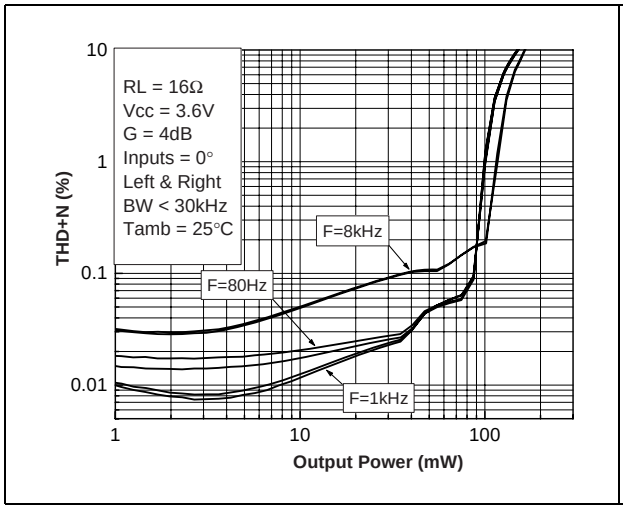


Figure 17. THD+N vs. output power

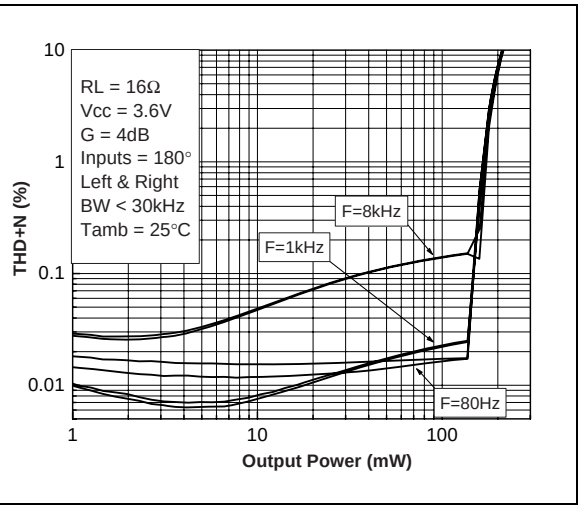


Figure 18. THD+N vs. output power

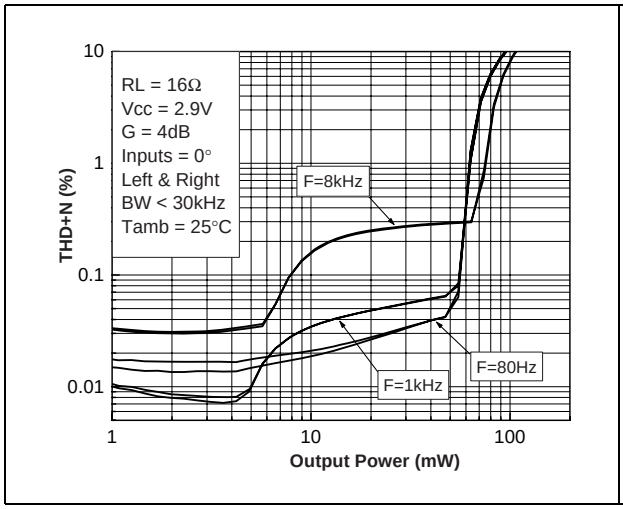


Figure 19. THD+N vs. output power

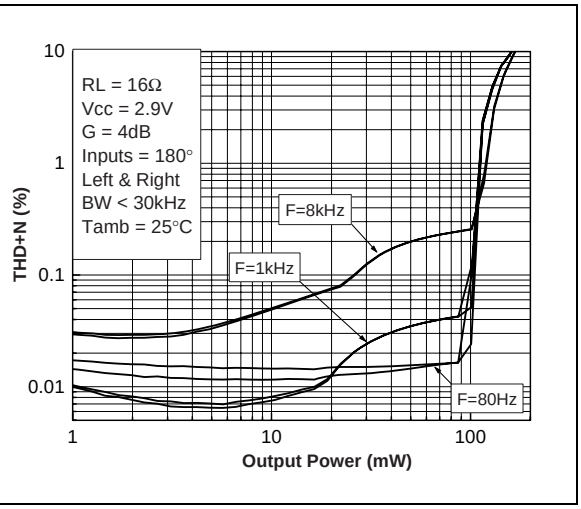


Figure 20. THD+N vs. output power

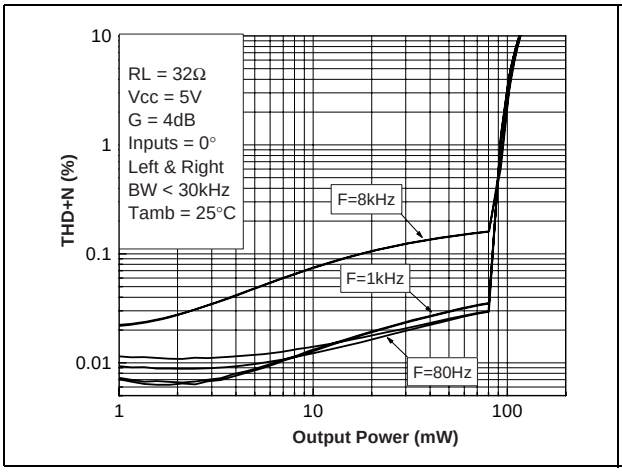


Figure 21. THD+N vs. output power

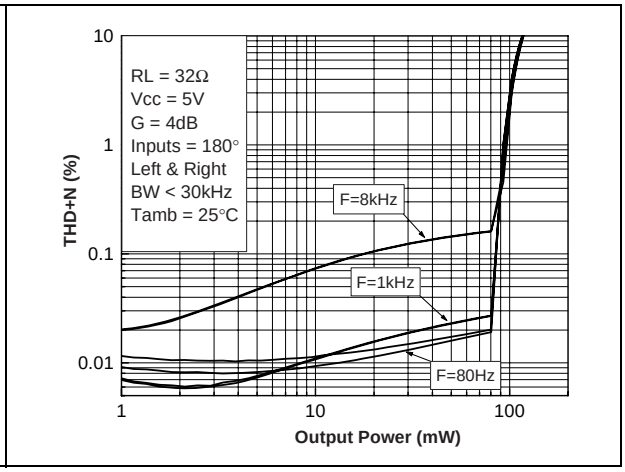


Figure 22. THD+N vs. output power

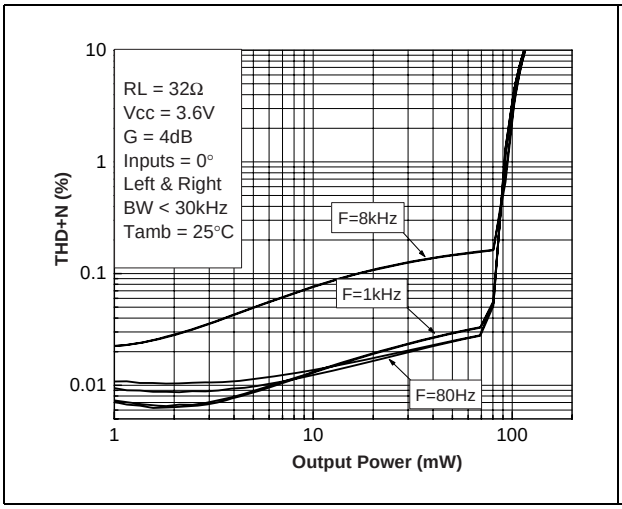


Figure 23. THD+N vs. output power

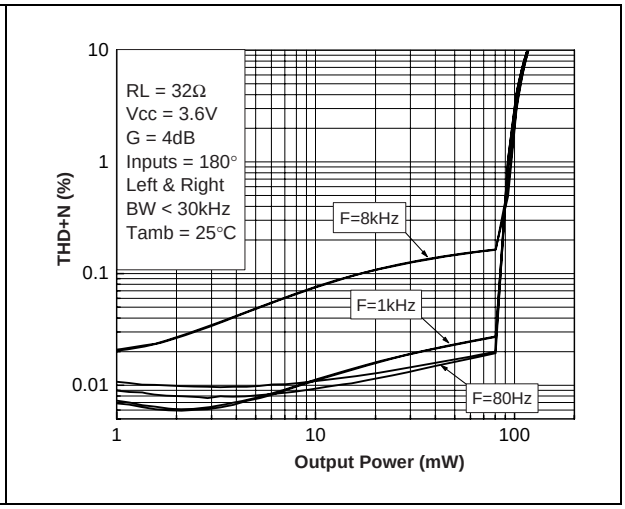


Figure 24. THD+N vs. output power

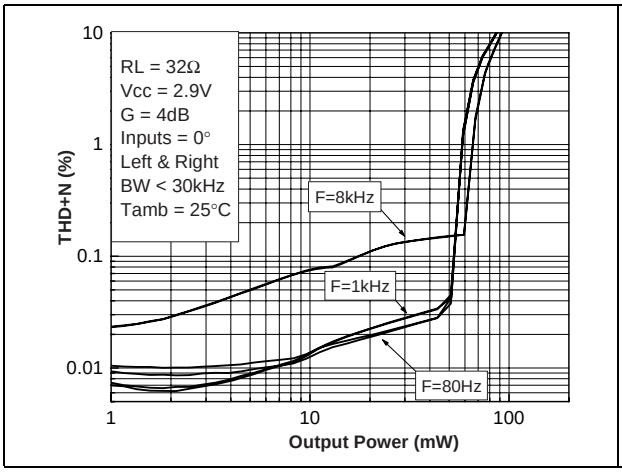


Figure 25. THD+N vs. output power

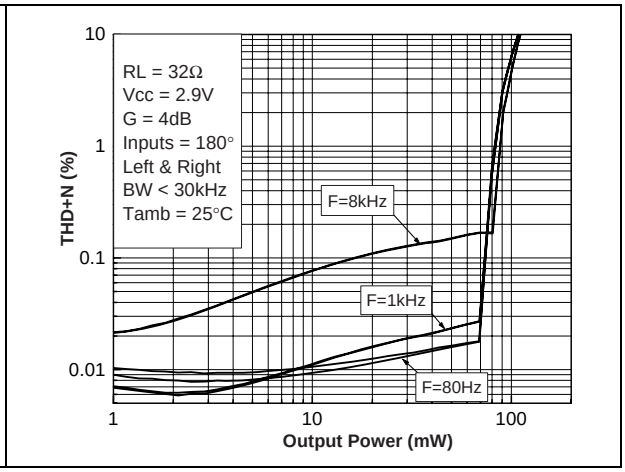


Figure 26. THD+N vs. output voltage

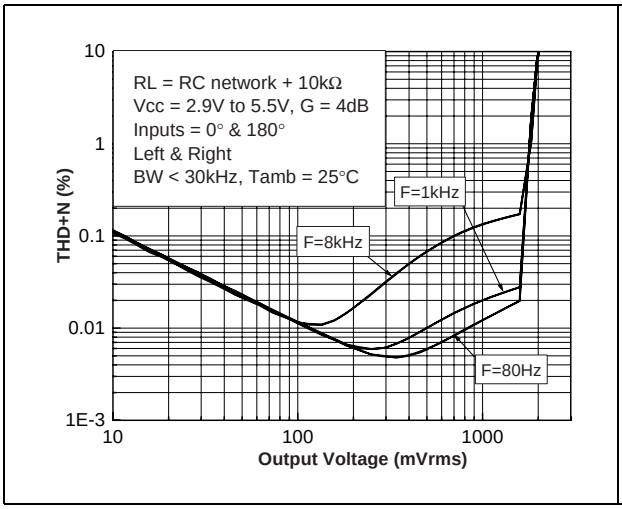


Figure 27. THD+N vs. frequency

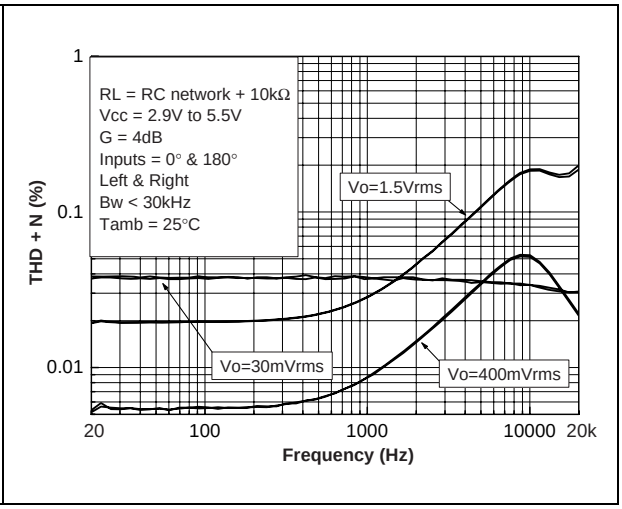


Figure 28. THD+N vs. frequency

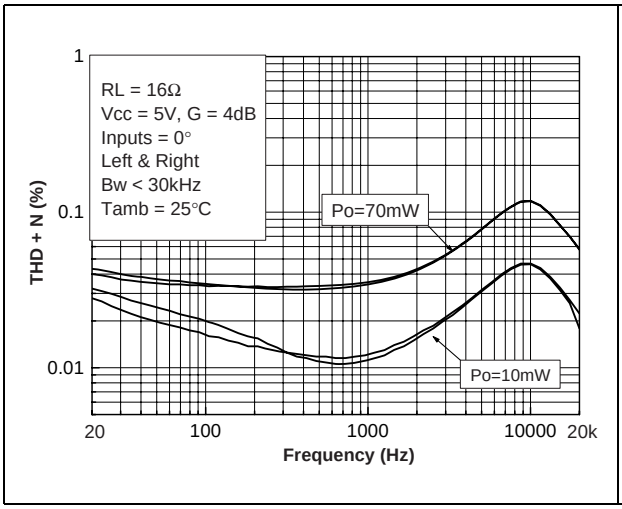


Figure 29. THD+N vs. frequency

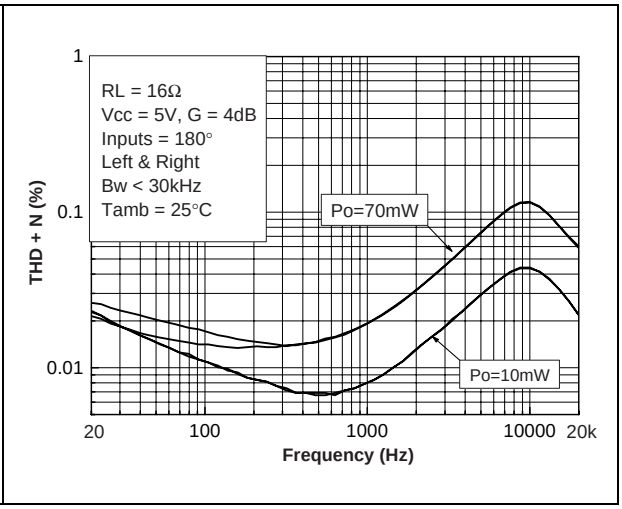


Figure 30. THD+N vs. frequency

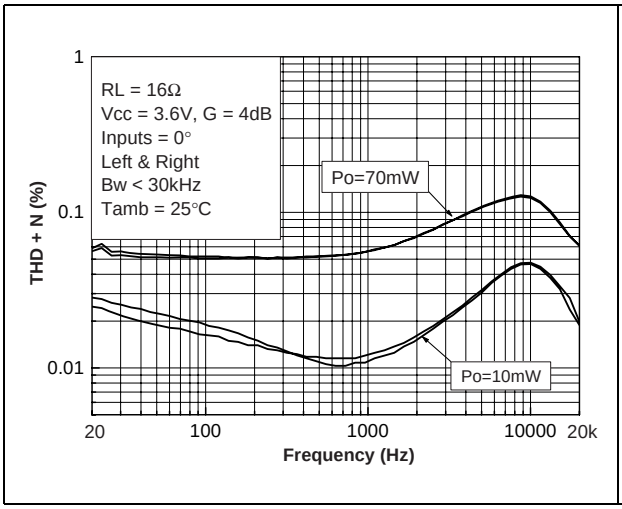


Figure 31. THD+N vs. frequency

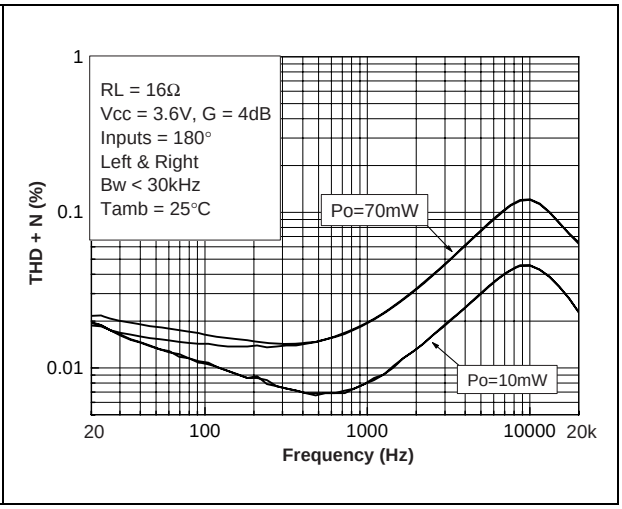


Figure 32. THD+N vs. frequency

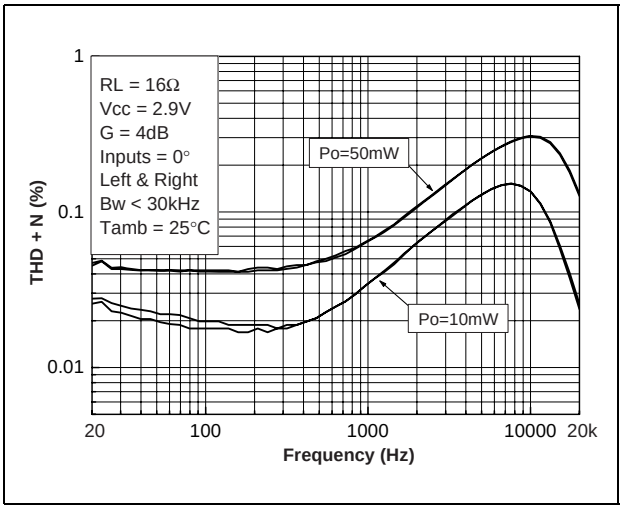


Figure 33. THD+N vs. frequency

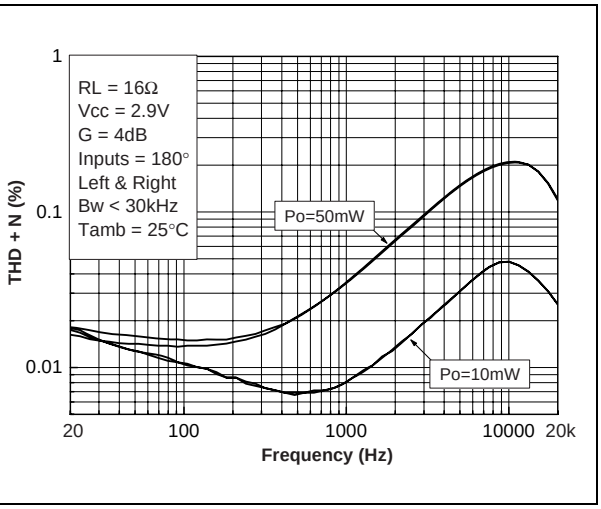


Figure 34. THD+N vs. frequency

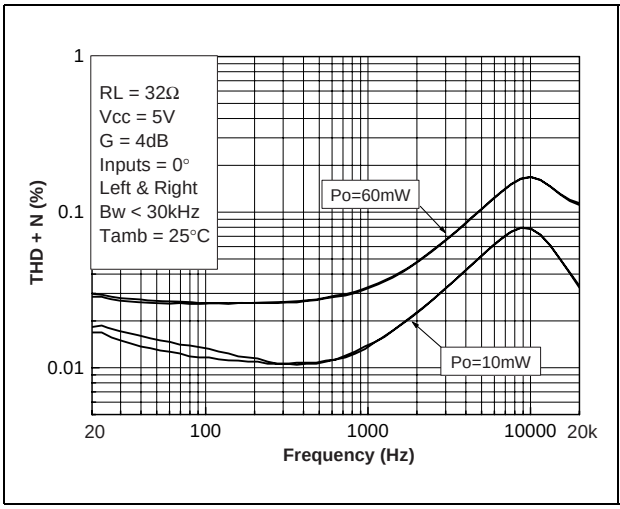


Figure 35. THD+N vs. frequency

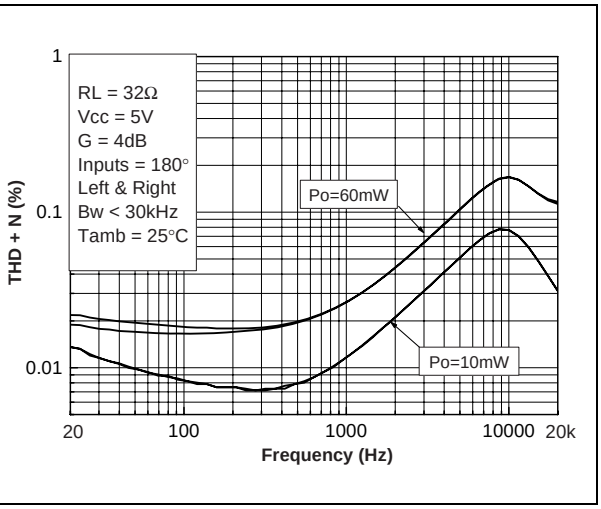


Figure 36. THD+N vs. frequency

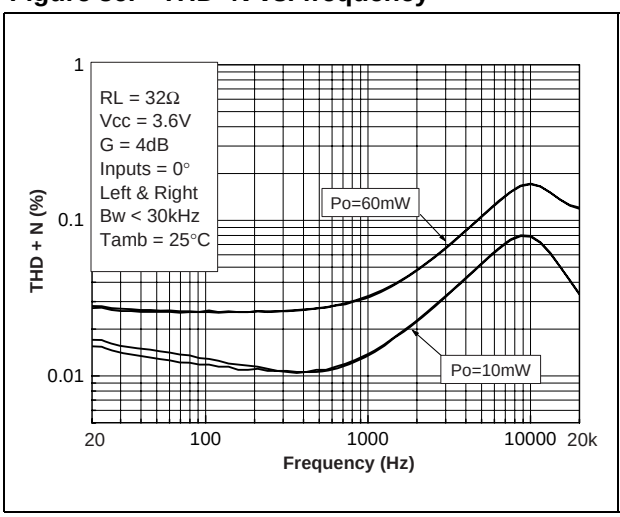


Figure 37. THD+N vs. frequency

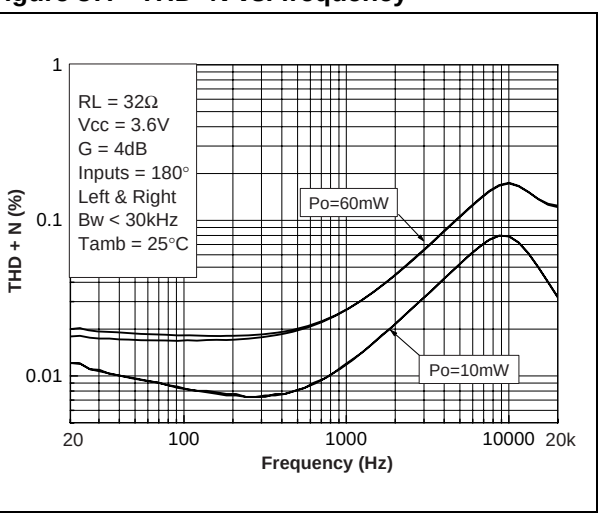


Figure 38. THD+N vs. frequency

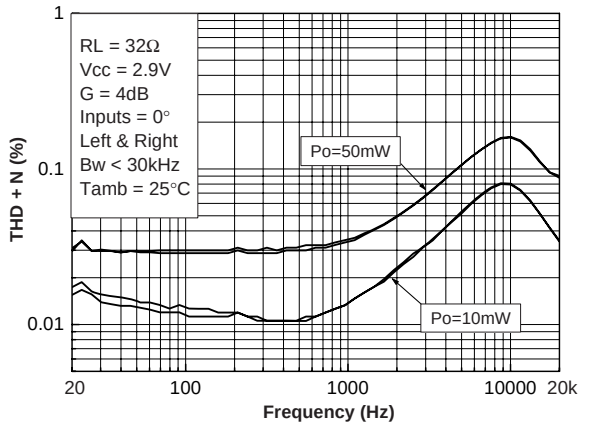


Figure 39. THD+N vs. frequency

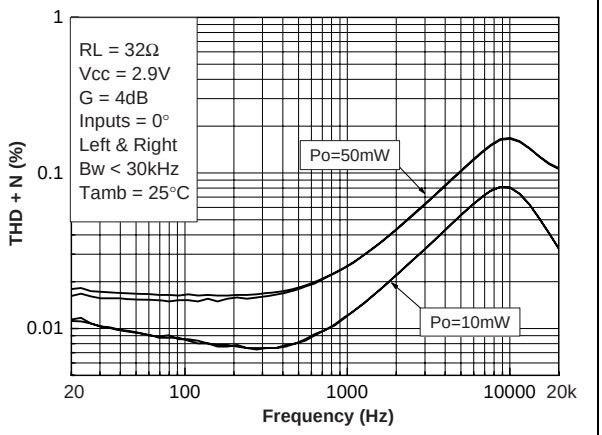


Figure 40. CMRR vs. frequency

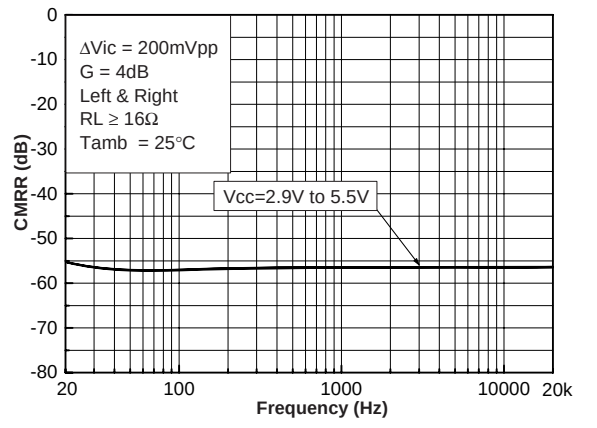


Figure 41. CMRR vs. frequency

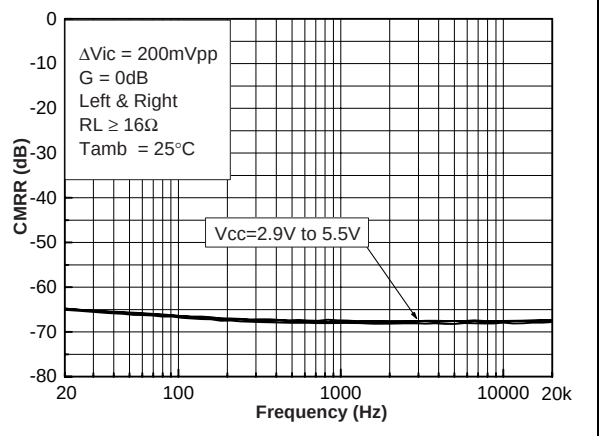


Figure 42. Crosstalk vs. frequency

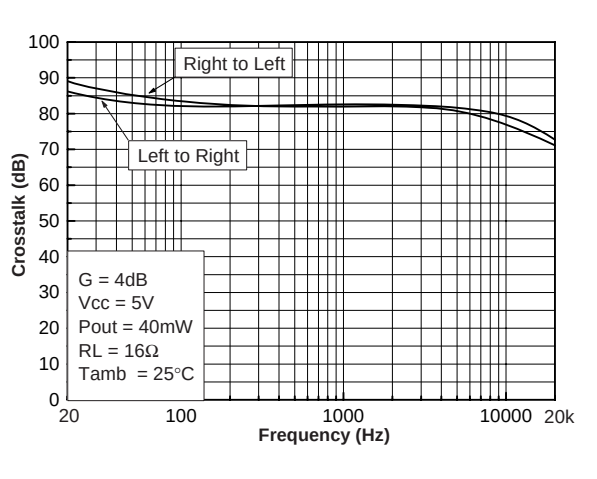


Figure 43. Crosstalk vs. frequency

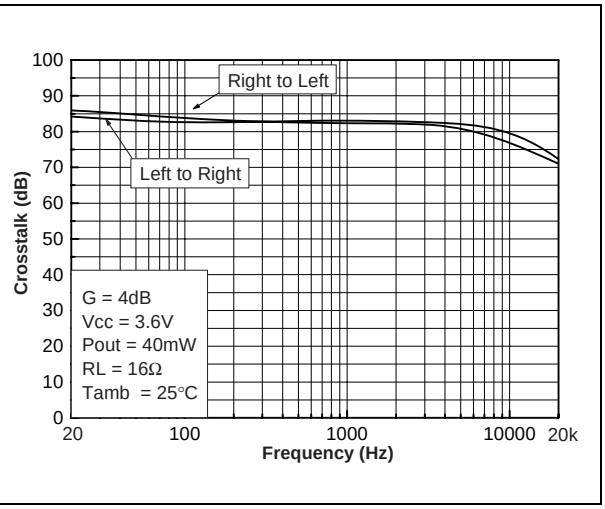


Figure 44. Crosstalk vs. frequency

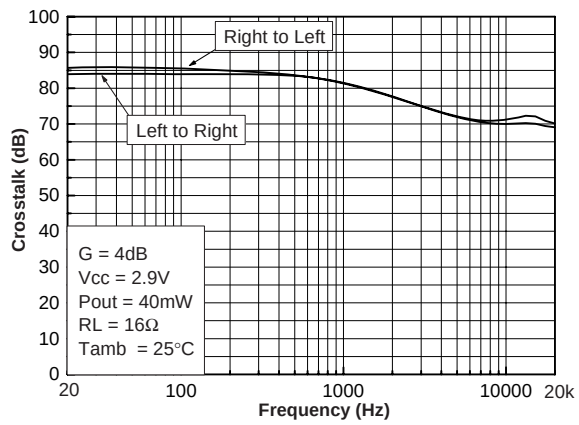


Figure 45. Crosstalk vs. frequency

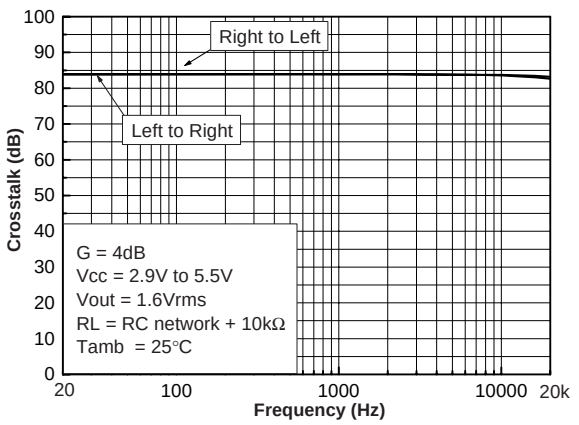


Figure 46. Common mode response vs. frequency

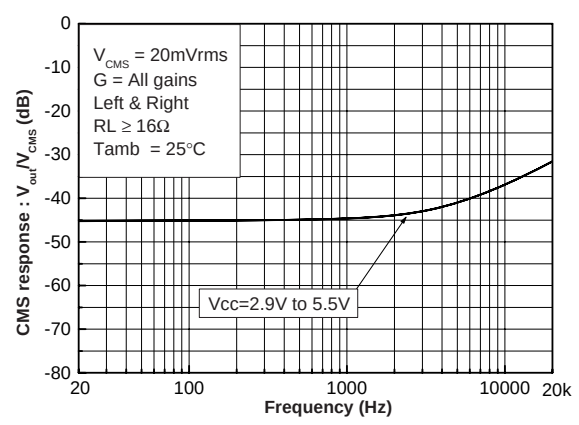


Figure 47. THD+N vs. input voltage. Line in mode 5

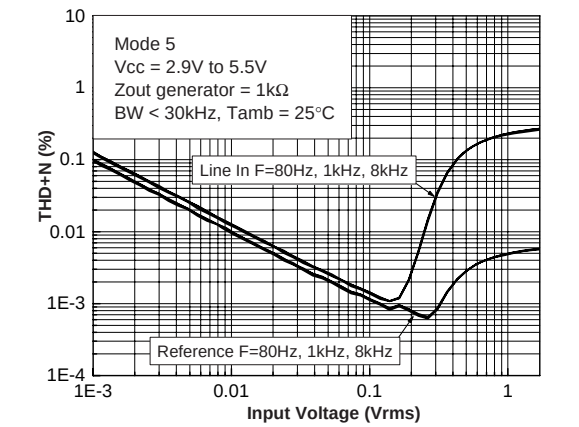


Figure 48. Input impedance vs. frequency. Line in mode 5

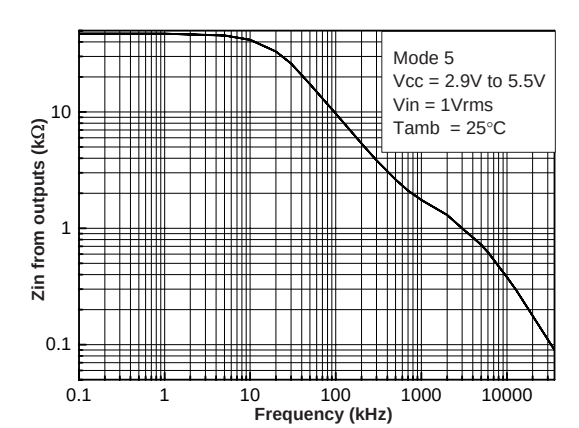
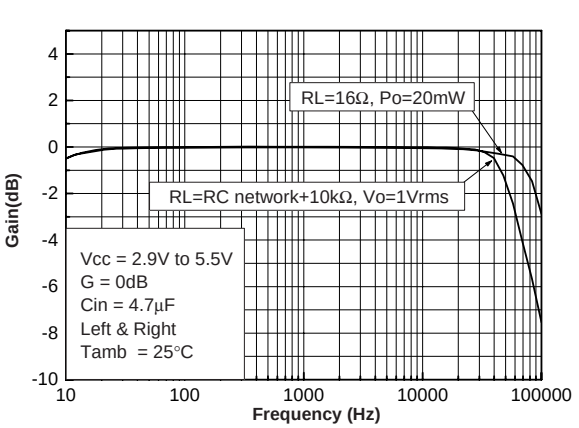


Figure 49. Gain vs. frequency



4 Application information

4.1 Common-mode sense

The TS4601 implements a common-mode sense to correct the voltage differences that might occur between the headphone jack return and the GND of the device, thus creating parasitic noise in the headphone and/or line-out.

The solution to strongly reduce and practically eliminate this noise, is to connect the headphone jack ground to the CMS of the device that is a common-mode sense pin. It will sense the difference of potential (voltage noise) between the TS4601 ground and headphone ground. Thanks to CMS frequency response (refer to *Figure 46 on page 16*), this noise is removed from the TS4601 outputs. *Figure 1: Typical application schematics for the TS4601* illustrates this connection.

4.2 I²C bus interface

In compliance with the I²C protocol, the TS4601 uses a serial bus to control the chip's functions with two wires: Clock (SCL) and Data (SDA). The clock line and the data line are bi-directional (open-collector) with an external chip pull-up resistor (typically 10 kΩ). The maximum clock frequency in fast-mode specified by the I²C standard is 400 kHz, which TS4601 supports. In this application, the TS4601 is always the slave device and the controlling microcontroller MCU is the master device.

The slave address of the TS4601 is 1100 000x (C0h).

An SDZ pin is available to shut down the circuit from a master MCU.

Table 7 summarizes the pin descriptions for the I²C bus interface.

Table 7. I²C bus interface pin descriptions

Pin	Functional description
SDA	Serial data pin
SCL	Clock input pin
SDZ	Master standby of the TS4601

4.2.1 I²C bus operation

The host MCU can write into the TS4601 control register to control the TS4601, and read from the control register to get a configuration from the TS4601. The TS4601 is addressed by the byte consisting of the 7-bit slave address and R/$\overline{W}$ bit.

Table 8. The first byte after the START message for addressing the device

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	0	0	0	0	X

There are five control registers (see *Table 9*) named CR0 to CR4. In read mode, all the control registers can be accessed. In write mode, only CR1 and CR2 can be addressed.

Table 9. Control registers summary

Description	D7	D6	D5	D4	D3	D2	D1	D0
CR0	SC_L	SC_R	T_SH	0	0	0	0	0
CR1 - modes	Output modes			0	0	0	0	0
CR2 - volume control	Mute_L	Mute_R	Volume control					
CR3	0	0	0	0	0	0	0	0
CR4 - identification	0	1	0	0	0	0	0	1

To write in the control registers:

In order to write data into the TS4601, after the “start” message, the MCU must:

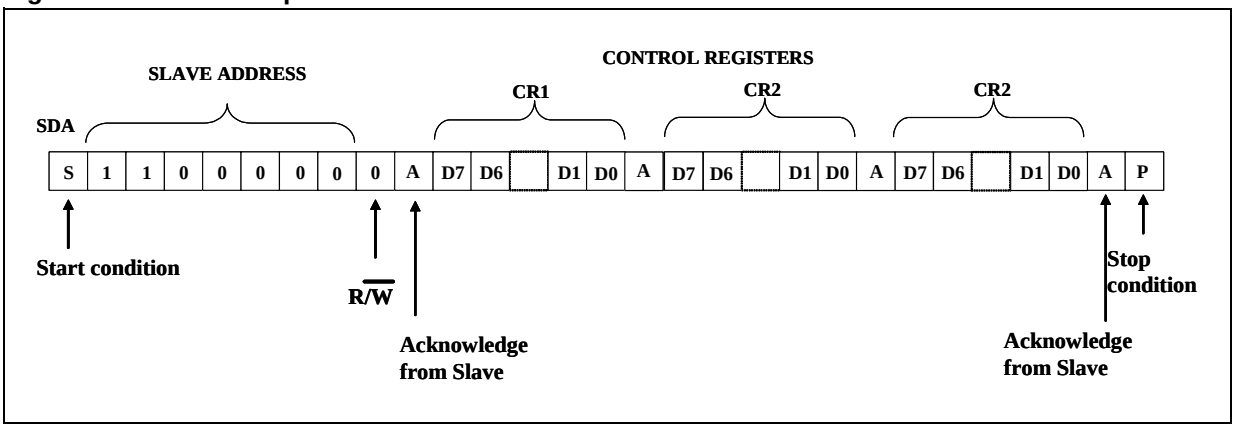
- send byte with the I²C 7-bit slave address and with a low level for the R/$\overline{W}$ bit
- send the data (control register setting)

All bytes are sent with MSB first. The transfer of written data ends with a “stop” message. When transmitting several data, the data can be written with no need to repeat the “start” message and addressing byte with the slave address.

When writing several bytes, the data is transmitted as follows:

- CR1 CR2 CR2 CR2... this is an advantage for a fast increase/decrease of the volume control.

Figure 50. I²C write operations



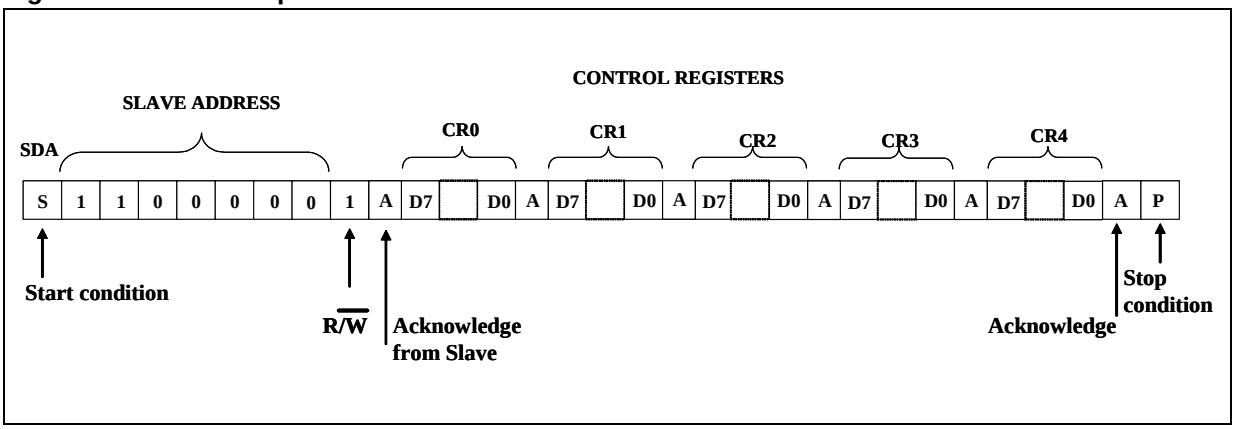
To read from the control registers:

In order to read data from the TS4601, after the “start” message, the MCU must:

- send byte with the I²C 7-bit slave address and with a high level for the R/$\overline{W}$ bit
- receive the data (control register value)

All bytes are read with MSB first. The transfer of read data ends with the “stop” message. When transmitting several data, the data can be read with no need to repeat the “start” message and the byte with the slave address. In this case, the value of the control register is read repeatedly, CR0, CR1, CR2, CR3, CR4, CR0, CR1 etc.

Figure 51. I²C read operations



4.2.2 Control registers

Table 10. Output mode configuration - CR1

Modes register				Headphone output Left	Headphone output Right	Negative supply and regulators
0	0	0	Mode 1: standby	SD(1)	SD	SD
0	0	1	Mode 2: channel R	SD	GxINR	ON
0	1	0	Mode 3: channel L	GxINL	SD	ON
0	1	1	Mode 4: on	GxINL	GxINR	ON
1	0	0	Mode 5: Line-in mode	SD	SD	ON
1	0	1	Mode 6: standby	SD	SD	SD
1	1	0	Mode 7: standby	SD	SD	SD
1	1	1	Mode 8: standby	SD	SD	SD

1. SD: shutdown,I NR: audio input right, INL: audio input left, G: gain for channel R and channel L, ON: when a function is active.

The TS4601 can be set to standby in two different ways:

- A master standby from an MCU using SDZ input, can set the TS4601 in master standby. The lowest current consumption (I_{stby}=2 µA maximum) is achieved with a 0 V on SDZ. At 0.63 V, I_{stby} is 20 µA maximum. Note that the SDZ input has a 600 kΩ +/-20% pull-down resistor. If VSDZ > 0 V, an additional current consumption has to be taken into consideration and provided by the MCU IO. This additional current is V_{SDZ}/600kΩ (+/-20%). During master standby mode, amplifiers, power management and I²C part are disabled thus offering the most current-saving standby mode.
- The TS4601 can also be set to I²C standby by an I²C command. In this case the I_{stby} is slightly higher and is I_{stby}=75 µA maximum (including current consumption on SDA and SCL inputs).

When the TS4601 is in Master standby or I²C standby mode (on one or both channels), the corresponding amplifier output is forced to ground through a 16 Ω resistor. In mode 5, in which amplifiers are inactive but the power management part is active, the amplifier outputs are in high impedance state to allow line in function.

Table 11. Volume control register - CR2

Volume control range: -60 dB to +4 dB													
D5	D4	D3	D2	D1	D0	Gain (in dB)	D5	D4	D3	D2	D1	D0	Gain (in dB)
0	0	0	0	0	0	Mute: -80dB	1	0	0	0	0	0	-11.5dB
0	0	0	0	0	1	-60dB	1	0	0	0	0	1	-11dB
0	0	0	0	1	0	-57dB	1	0	0	0	1	0	-10.5dB
0	0	0	0	1	1	-54dB	1	0	0	0	1	1	-10dB
0	0	0	1	0	0	-51dB	1	0	0	1	0	0	-9.5dB
0	0	0	1	0	1	-48dB	1	0	0	1	0	1	-9dB
0	0	0	1	1	0	-45dB	1	0	0	1	1	0	-8.5dB
0	0	0	1	1	1	-42dB	1	0	0	1	1	1	-8dB
0	0	1	0	0	0	-39dB	1	0	1	0	0	0	-7.5dB
0	0	1	0	0	1	-36dB	1	0	1	0	0	1	-7dB
0	0	1	0	1	0	-34.5dB	1	0	1	0	1	0	-6.5dB
0	0	1	0	1	1	-33dB	1	0	1	0	1	1	-6dB
0	0	1	1	0	0	-31.5dB	1	0	1	1	0	0	-5.5dB
0	0	1	1	0	1	-30dB	1	0	1	1	0	1	-5dB
0	0	1	1	1	0	-28.5dB	1	0	1	1	1	0	-4.5dB
0	0	1	1	1	1	-27dB	1	0	1	1	1	1	-4dB
0	1	0	0	0	0	-25.5dB	1	1	0	0	0	0	-3.5dB
0	1	0	0	0	1	-24dB	1	1	0	0	0	1	-3dB
0	1	0	0	1	0	-22.5dB	1	1	0	0	1	0	-2.5dB
0	1	0	0	1	1	-21dB	1	1	0	0	1	1	-2dB
0	1	0	1	0	0	-19.5dB	1	1	0	1	0	0	-1.5dB
0	1	0	1	0	1	-18dB	1	1	0	1	0	1	-1dB
0	1	0	1	1	0	-16.5dB	1	1	0	1	1	0	-0.5dB
0	1	0	1	1	1	-16dB	1	1	0	1	1	1	0dB
0	1	1	0	0	0	-15.5dB	1	1	1	0	0	0	0.5dB
0	1	1	0	0	1	-15dB	1	1	1	0	0	1	1dB
0	1	1	0	1	0	-14.5dB	1	1	1	0	1	0	1.5dB
0	1	1	0	1	1	-14dB	1	1	1	0	1	1	2dB
0	1	1	1	0	0	-13.5dB	1	1	1	1	0	0	2.5dB
0	1	1	1	0	1	-13dB	1	1	1	1	0	1	3dB
0	1	1	1	1	0	-12.5dB	1	1	1	1	1	0	3.5dB
0	1	1	1	1	1	-12dB	1	1	1	1	1	1	4dB

In the volume register, MUTE_L, and MUTE_R are dedicated bits to enable the mute independently from the channel. When MUTE_L, MUTE_R are set to VIH, the mute function is enabled on the corresponding channel. When MUTE_L, MUTE_R are set to VIL, the gain level is applied to the channel.

Control register CR0

Amplifier output short-circuit detection:

The outputs of the amplifier are protected against short-circuits that might occur accidentally during manipulation of the device. In the typical application, if a short-circuit arises on the jack plug, there is no detection due to the serial resistor present on the amplifier output, thus the output current threshold is not reached.

To be active, the detection has to occur directly on the amplifier output with a signal modulation on the inputs of the TS4601.

If a short-circuit is detected on one channel, a flag is raised in the I²C read register CR0.

- SC_L: equals 0 during normal operation, equals 1 when a short-circuit is detected on the left channel
- SC_R: equals 0 during normal operation, equals 1 when a short-circuit is detected on the right channel

The corresponding channel output stage is then set to high impedance mode. An I²C read command allows the reading of the SC_L and SC_R flags but does not reset them. An I²C write command has to be sent to reset the flags to 0 and restore normal operation.

When the TS4601 is in I²C standby mode, the SC_L and SC_R flags are in an undetermined state.

Thermal shutdown protection:

A thermal shutdown protection is implemented to protect the device from overheating. If the temperature rises above the thermal junction of 150°C, the device is put into standby mode and a flag is raised in the read register CR0.

- T_SH: equals 0 during normal operation, equals 1 when a thermal shutdown is detected.

When the temperature decreases to safe levels, the circuit switches back to normal operation and the corresponding flag is cleared.

4.3 Wake-up and standby time definition

The wake-up time of the TS4601 is guaranteed at 12 ms typical (refer to *Section 3.1: Electrical characteristics tables on page 6*). However, as the TS4601 is activated with an I^2C bus, the wake-up start procedure is as follows:

1. The master sends a start bit
2. The master sends the address.
3. The slave (TS4601) answers by an acknowledge.
4. The master sends the output mode configuration (CR1).
5. If the TS4601 was in I^2C standby (mode 1, 6, 7), the wake-up starts on the falling edge of the eighth clock signal (SCL) corresponding to CR1 byte.
6. 12 ms after (de-pop sequence time), the TS4601 outputs are operational.

The standby time is guaranteed as 10 µs typical (refer to *Section 3.1: Electrical characteristics tables on page 6*). However, as the TS4601 is de-activated with an I^2C bus, the standby time operates as follows:

1. The master sends a start bit
2. The master sends the address.
3. The slave (TS4601) answers by an acknowledge.
4. The master sends the output mode configuration (CR1) and in this case it corresponds to mode 1, 6, 7.
5. The standby time starts on the falling edge of the eighth clock signal (SCL) corresponding to CR1 byte.
6. After 10 µs, the TS4601 is in standby mode.

4.4 Decoupling considerations

The TS4601 needs two decoupling capacitors for the positive power supply (battery) and two capacitors for normal operation of the internal negative supply (refer to *Figure 1: Typical application schematics for the TS4601 on page 4*). These capacitors must be placed as close as possible of the TS4601 to minimize parasitic inductance and resistance that have a negative impact on audio performance.

Two decoupling capacitors (Cs) of 1 µF and low ESR are recommended for positive power supply decoupling. Packages like the 0402 or 0603 are also recommended because the placement close to TS4601 is easier. X5R dielectric for capacitor tolerance behavior and 10 V DC rating voltage for 5 V operation or 6.3 V DC rating operation for 3.6 V operation to take into consideration the $\Delta C/\Delta V$ variation of this type of dielectric.

Two decoupling capacitors (C12 and Css) of respectively 1 µF and 2.2 µF and low ESR are recommended for internal negative power supply decoupling. Packages like the 0402 or 0603 are also recommended because the placement close to TS4601 is easier. X5R dielectric for capacitor tolerance behavior and 10 V DC rating voltage for 5 V operation or 6.3 V DC rating operation for 3.6 V operation to take into consideration the $\Delta C/\Delta V$ variation of this type of dielectric.

4.5 Low frequency response

Input coupling capacitors C_{in} (see *Figure 1: Typical application schematics for the TS4601 on page 4*) are mandatory for TS4601 operation. C_{in} with Z_{in} (see *Section 3.1: Electrical characteristics tables on page 6*) form a first order high pass filter and the -3 dB cut-off frequency is:

$$F_c(-3dB) = \frac{1}{2\pi Z_{in} C_{in}}$$

Z_{in} is the single-ended input impedance.

Because Z_{in} is independent from the gain setting, determining the appropriate C_{in} is very simple. However, the tolerance of Z_{in} (refer to *Section 3.1: Electrical characteristics tables on page 6*) must be taken into consideration for determining C_{in}.

Therefore, for a given F_c, the value of C_{in} is given by the following equation:

$$\left(C_{in_{min}} = \frac{16}{F_c}\right) \leq \left(C_{in_{typ}} = \frac{13.3}{F_c}\right) \leq \left(C_{in_{max}} = \frac{11}{F_c}\right)$$

(With C_{in} in µF and F_c in Hz).

4.6 Low pass output filter

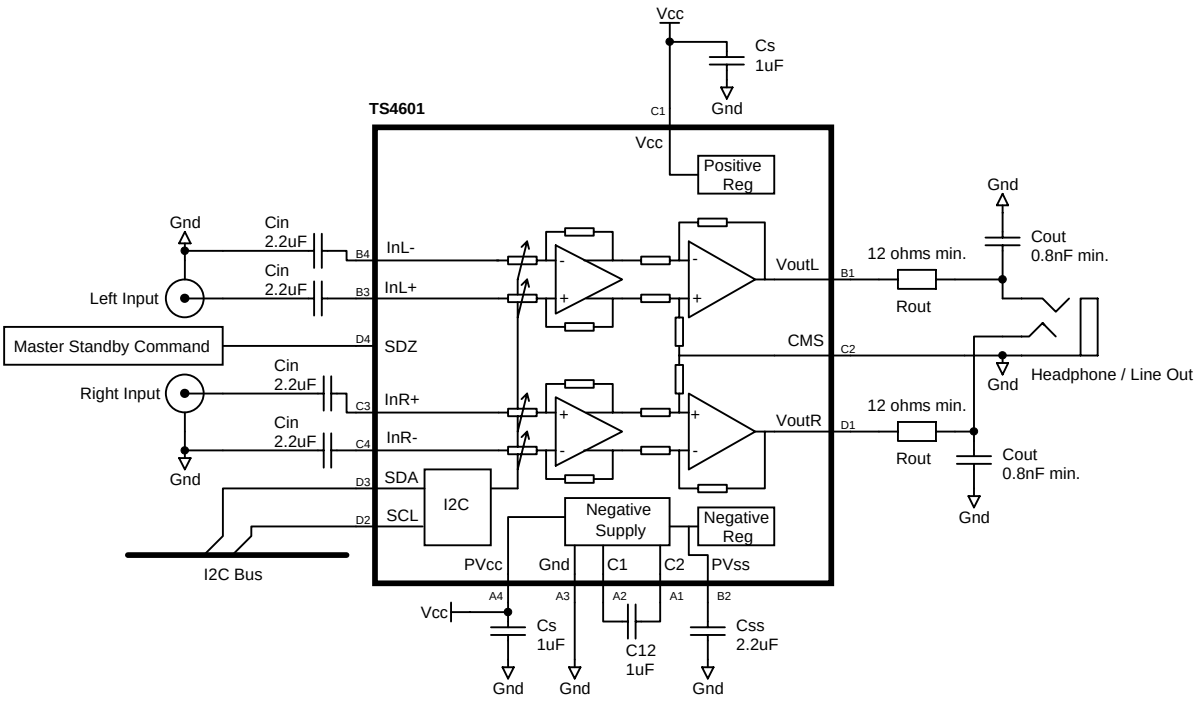
The TS4601 is designed to operate with a passive first order low pass filter (see *Figure 1: Typical application schematics for the TS4601 on page 4*). This low pass filter is mandatory to ensure stability of the TS4601.

R_{out} must have a value of 12 Ω minimum and C_{out} a value of 0.8 nF minimum up to 100 nF maximum. Values of 12 Ω and 1 nF are a good start point for a design able to drive a classic headphone (16 Ω, 32 Ω, 60 Ω) and the line-in of any Hi-fi system or sound card. The cut-off frequency of this filter (12 Ω and 1 nF) is about 13 MHz and clearly above the audio band.

4.7 Single-ended input configuration

The TS4601 can be used in single-ended input configuration. InR- and InL- must be shorted to ground through input capacitors. All C_{in} capacitors must have the same value to keep the same PSRR performance as in differential input configuration. *Figure 52* shows an example.

Figure 52. Typical application schematics for the TS4601 in single-ended input



The gain in this configuration is given by:

$$Gain(dB) = 20\log\left(\frac{V_{outL}}{V_{inputLeft}}\right)$$

or:

$$Gain(dB) = 20\log\left(\frac{V_{outR}}{V_{inputRight}}\right)$$

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 53. TS4601 footprint recommendation

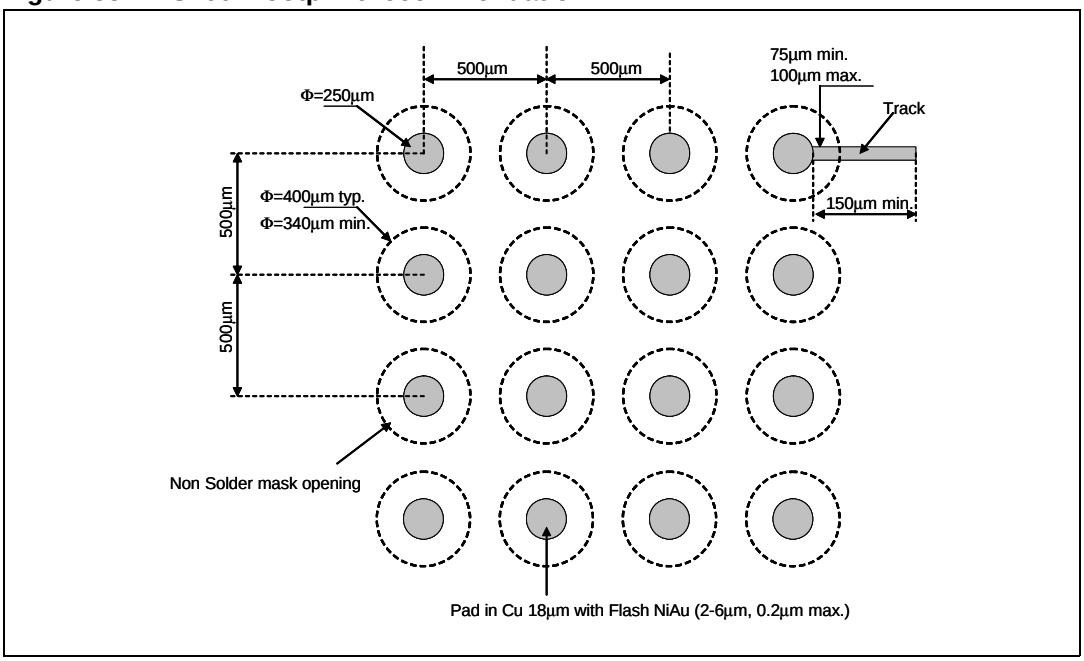


Figure 54. Pinout

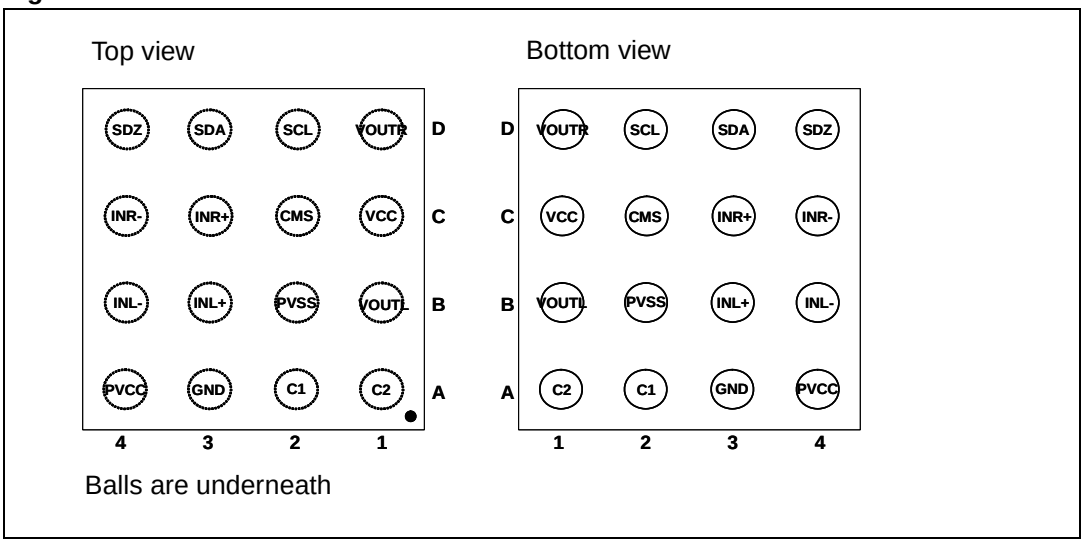


Figure 55. Marking (top view)

- Logo: ST
- Symbol for lead-free: E
- Part number: 01
- X digit: Assembly code
- Date code: YWW
- The dot marks pin A1

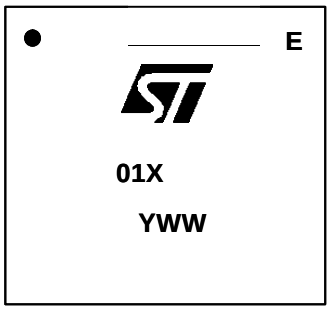
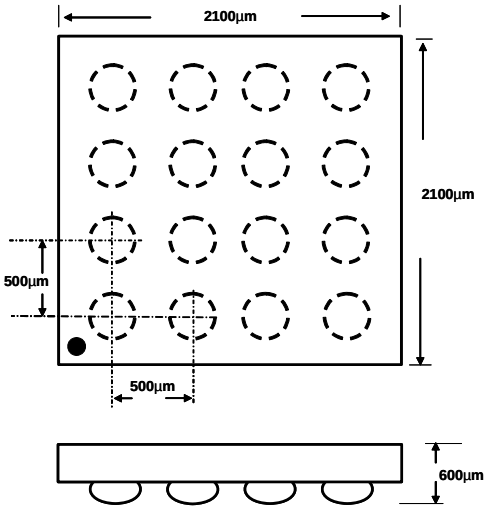
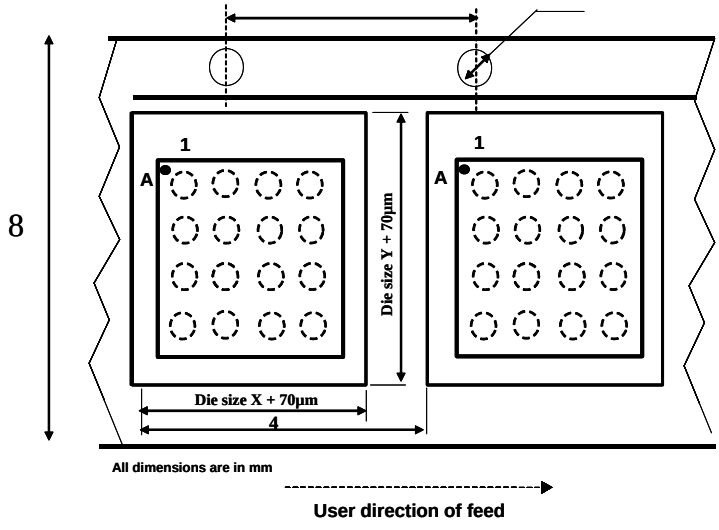


Figure 56. Flip-chip - 16 bumps



- Die size: 2.1mm x 2.1mm ± 30µm
- Die height (including bumps): 600µm
- Bumps diameter: 315µm ±50µm
- Bump diameter before reflew: 300µm ±10µm
- Bump height: 250µm ±40µm
- Die height: 350µm ±20µm
- Pitch: 500µm ±50µm
- Coplanarity: 60µm max

Figure 57. Device orientation in the tape pocket



6 Ordering information

Table 12. Order codes

Order code	Temperature range	Package	Packing	Marking
TS4601EIJT	-40° C to +85° C	Flip-chip	Tape & reel	01

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
15-Jan-2008	1	Initial release, preliminary information.
20-Feb-2008	2	Complete datasheet for release to market of the device.

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