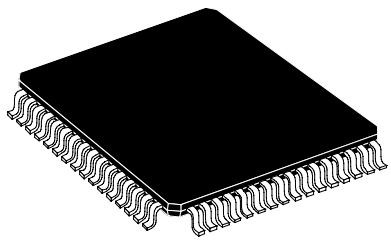
STV6414A

Audio/video switch matrix

Features

- I²C bus control
- Standby mode with interrupt signal output
- Video section
  - 3 CVBS inputs, 2 CVBS outputs
  - 3 Y/C inputs, 2 Y/C outputs
  - Switchable LPFs (low pass filters) on 6 inputs
  - 6 dB gain on all CVBS/Y and C outputs
  - Integrated 150 Ω buffers
  - 2 RGB/FB inputs, 1 tri-state RGB/FB output with 6 dB adjustable gain (from +3 dB to +9 dB)
  - Video muting on all outputs
  - 2 slow blanking inputs/outputs
  - Sync bottom clamp on all CVBS/Y and RGB inputs, average clamp on C inputs
  - SVHS switch on C VCR output
  - Bandwidth: 15 MHz
  - Crosstalk: 50 dB minimum
- Audio section
  - 3 stereo inputs, 3 stereo outputs
  - Stereo-to-mono sound capability
  - 0/6/9 dB selectable gain on one stereo input
  - Full range volume control with soft control
  - Audio muting on all outputs



LQFP64
(10 × 10 × 1.4 mm)
(Low-profile Quad Flat Package)
Marking:
STV6414ADT

Description

The STV6414A is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides the audio and video routings required in a two SCART set-top box design.

In an LQFP64 (10 × 10 × 1.4 mm) package, the STV6414A is compatible with the STV6413.

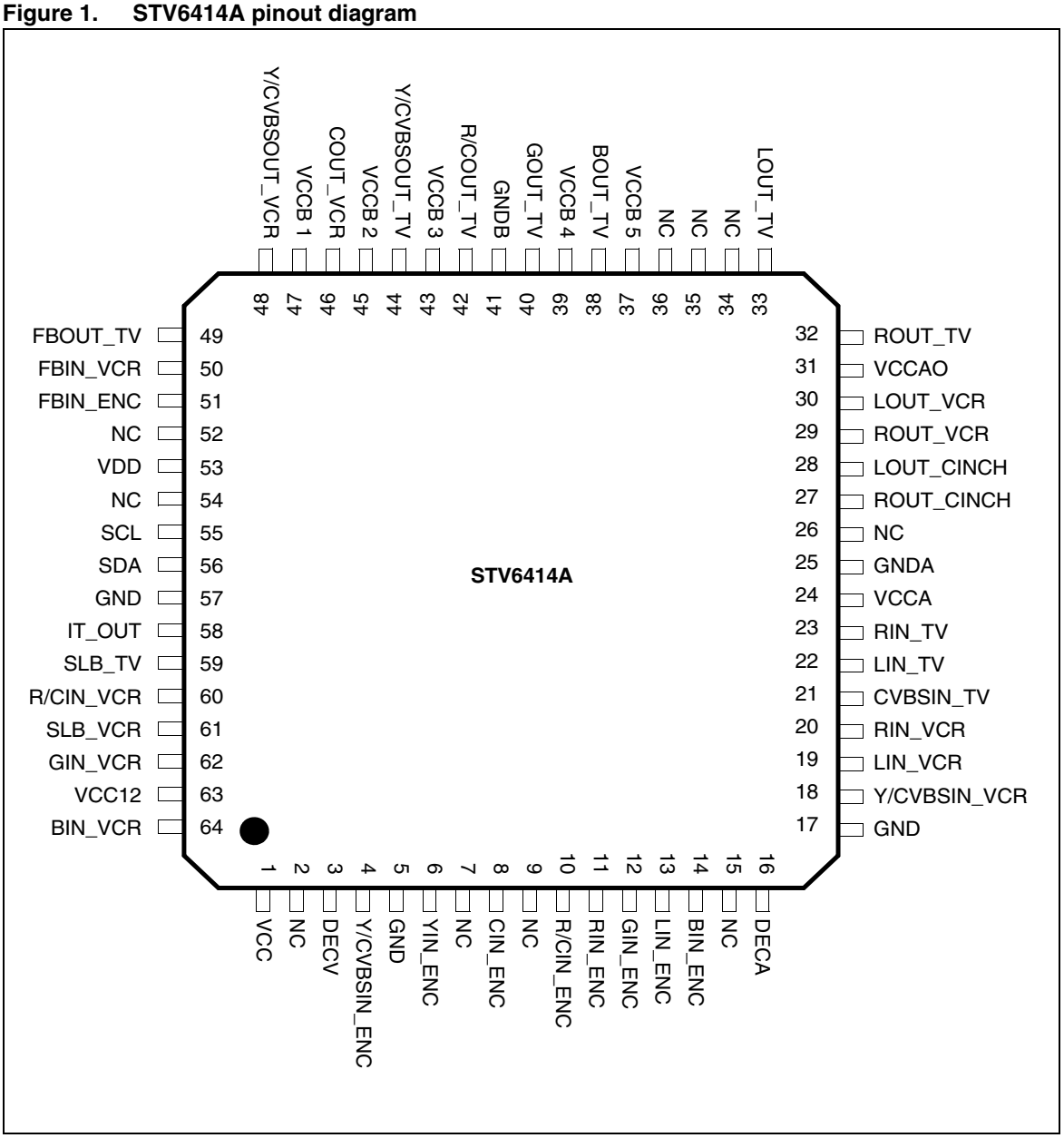
Table 1. Device summary

Order code	Packaging
STV6414AD	Tray
STV6414ADT	Tape and reel

Contents

1 General information

Figure 1. STV6414A pinout diagram



1.1 I/O pin description

Table 2. I/O pin description

Pin No.	Name	Function
1	VCC	+5 V Supply
2	NC	Not connected
3	DECV	Video decoupling capacitor
4	Y/CVBSIN_ENC	Y/CVBS input from encoder
5	GND	Ground
6	YIN_ENC	Y input from encoder
7	NC	Not connected
8	CIN_ENC	Chroma input from encoder
9	NC	Not connected
10	R/CIN_ENC	Red/Chroma input from encoder
11	RIN_ENC	Audio right, input from encoder
12	GIN_ENC	Green input from encoder
13	LIN_ENC	Audio left, input from encoder
14	BIN_ENC	Blue input from encoder
15	NC	Not connected
16	DECA	Audio decoupling capacitor
17	GND	Ground
18	Y/CVBSIN_VCR	Y/CVBS input from VCR SCART
19	LIN_VCR	Audio left, input from VCR SCART
20	RIN_VCR	Audio right, input from VCR SCART
21	CVBSIN_TV	CVBS input from TV SCART
22	LIN_TV	Audio left, input from TV SCART
23	RIN_TV	Audio right, input from TV SCART
24	VCCA (see *Figure 2*)	9V audio supply voltage output if VCCAO is used as 12V supply voltage input or 9V audio supply voltage input, VCCAO must be used as 9V supply voltage input
25	GNDA	Audio ground
26	NC	Not connected
27	ROUT_CINCH	Audio right output to CINCH
28	LOUT_CINCH	Audio left output to CINCH
29	ROUT_VCR	Audio right output to VCR SCART
30	LOUT_VCR	Audio left output to VCR SCART

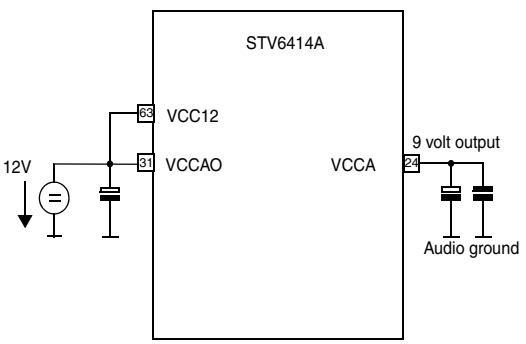
Table 2. I/O pin description (continued)

Pin No.	Name	Function
31	VCCAO (see *Figure 2*)	12V supply voltage input, VCCA is regulated 9V output for decoupling or 9v Supply Voltage input, VCCA must be used as 9V supply voltage input.
32	ROUT_TV	Audio right output to TV SCART
33	LOUT_TV	Audio left output to TV SCART
34	NC	Not connected
35	NC	Not connected
36	NC	Not connected
37	VCCB5	Video output buffer supply pin
38	BOUT_TV	Blue output to TV SCART
39	VCCB4	Video output buffer supply pin
40	GOUT_TV	Green output to TV SCART
41	GNDB	Video buffer ground
42	R/COUT_TV	Red/Chroma output to TV SCART
43	VCCB3	Video output buffer supply pin
44	Y/CVBSOUT_TV	Y/CVBS output to TV SCART
45	VCCB2	Video output buffer supply pin
46	COUT_VCR	Chroma output to VCR SCART
47	VCCB1	Video output buffer supply pin
48	Y/CVBSOUT_VCR	Y/CVBS output to VCR SCART
49	FBOUT_TV	Fast blanking output to TV SCART
50	FBIN_VCR	Fast blanking input from VCR SCART
51	FBIN_ENC	Fast blanking input from encoder
52	NC	Not connected
53	VDD	+5 V I²C supply
54	NC	Not connected
55	SCL	I²C bus clock
56	SDA	I²C bus data
57	GND	Ground digital
58	IT_OUT	Interrupt output
59	SLB_TV	Slow blanking input/output from TV SCART
60	R/CIN_VCR	Red input (or C Input) from VCR SCART
61	SLB_VCR	Slow blanking input/output from VCR SCART
62	GIN_VCR	Green input from VCR SCART

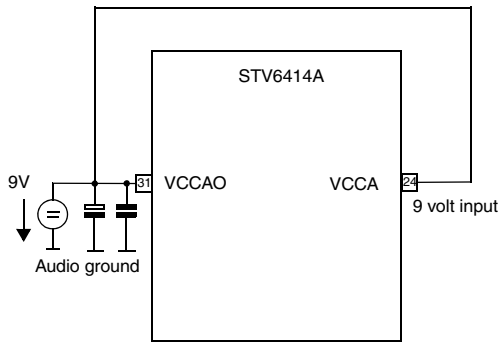
Table 2. I/O pin description (continued)

Pin No.	Name	Function
63	VCC12	+12 V supply
64	BIN_VCR	Blue input from VCR SCART

Figure 2. Power supply configuration



In applications where a 12 volt supply from slow blanking is used to derive the internal audio 9 Volt supply voltage, the VCCAO pin must be connected to the 12 volt supply as shown in the example. The VCCA pin will show the regulated 9 volt audio supply voltage which must be decoupled by capacitors.



In applications having a dedicated audio supply voltage, the VCCAO pin must be connected together with the VCCA pin to the audio supply as shown in the example. The VCCA pin acts as power supply input for the internal audio block.

Figure 3. STV6414A block diagram

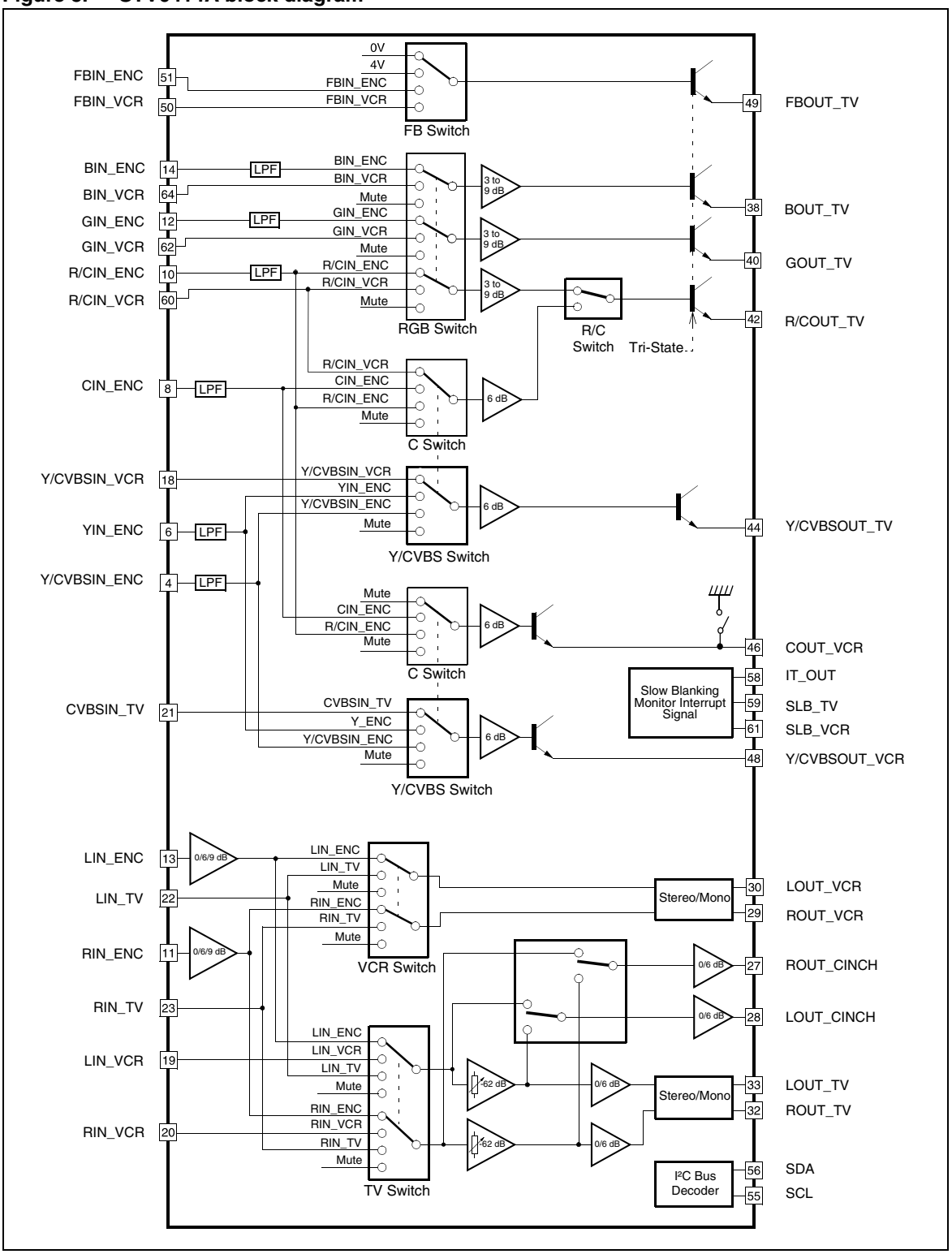
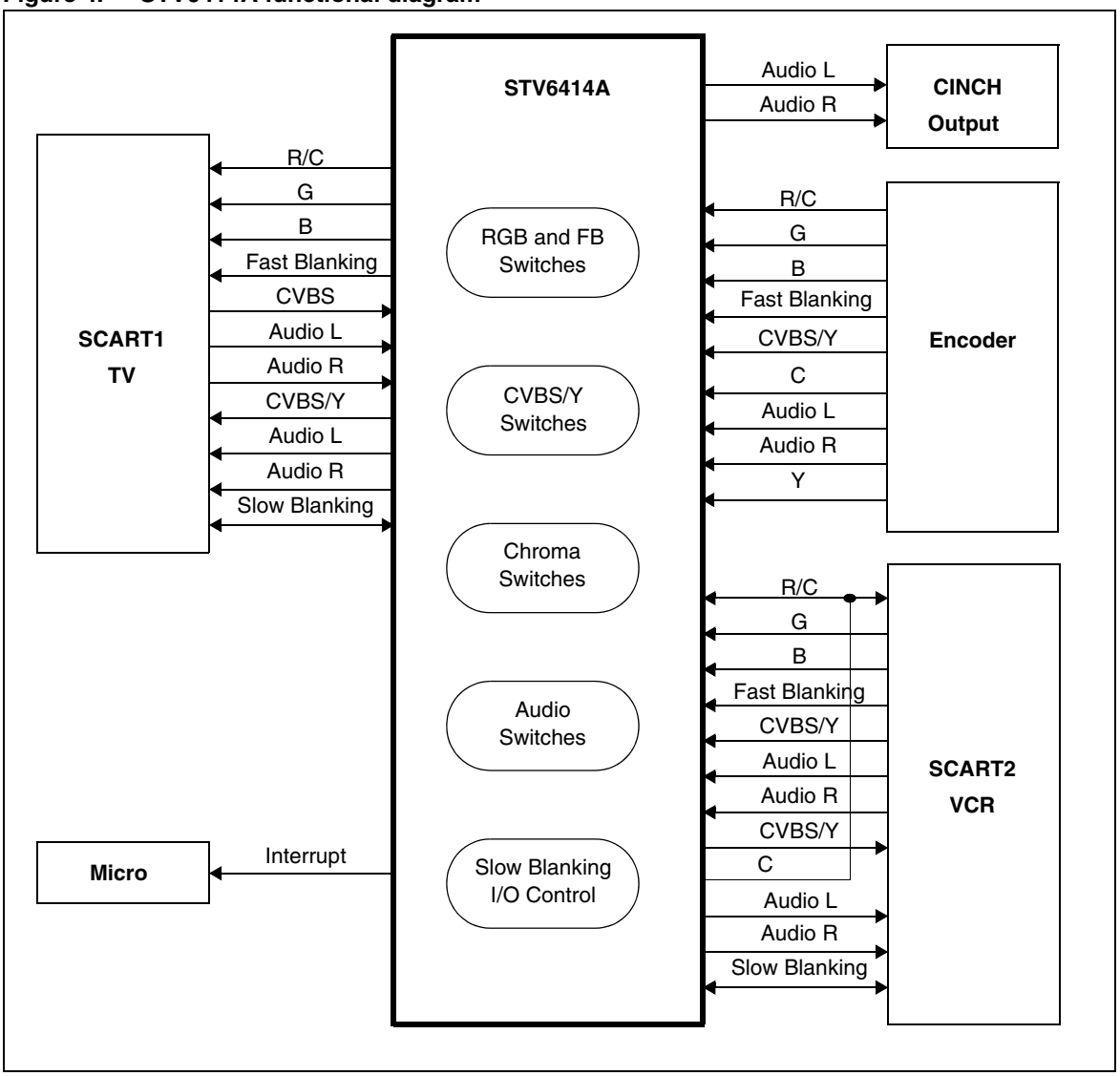


Figure 4. STV6414A functional diagram



2 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC12}	Supply voltage for slow blanking sections		13.2	V
V_{CCAO}	Supply voltage for audio drivers		13.2	V
V_{CCA}	Supply voltage for digital audio sections		10	V
V_{DD}	Supply voltage for digital sections		6	V
V_{CC}, V_{CCBI}	Supply voltage for video sections		6	V
V_{IN}	Input voltage at pin (in reference to GND)	Audio pins Video pins Bus pins Slow Blanking pins	0, V_{CCA} 0, V_{CC} or V_{CCBI} 0, 5.5 0, V_{CC12}	V
V_{ESD}	Maximum ESD Voltage allowed. (human body model: 100 pF capacitor discharged through 1.5 kOhm serial resistor)		±4	kV

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum junction-to-ambient thermal resistance	58	°C/W
T_{STG}	Storage temperature	-20, +150	°C
T_{OPER}	Operating free air temperature range	0 to +70	°C
T_j	Maximum junction temperature	150	°C

2.1 Latch-up data

At an ambient temperature of 25 °C, all pins meet the following specifications:

I trigger = 200 mA or I trigger = -200 mA.

2.2 Recommended operating conditions

T_{AMB} = 25° C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V, R_{LOUTA} = 10 kΩ, R_{LOUTV} = 150 Ω (unless otherwise specified)

Table 5. Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Supply voltages						
V_{DD}	Digital supply voltage		4.75	5	5.25	V
V_{CCAO}	Audio operating supply voltage	- Decoupling capacitor on V_{CCA} - Connected to V_{CCA}	11.2 8.5	12 9	12.8 9.5	V

Table 5. Recommended operating conditions (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Video operating supply voltage		4.75	5	5.25	V
V_{CC12}	Slow blanking control supply voltage		11.2	12	12.8	V
Active mode (all channels ON)						
I_{DD}	Digital supply current	V_{DD} = 5 V		6	10	mA
I_{CCA}	Audio supply current	V_{CCAO} = 12 V, no load		8	15	mA
I_{CCV}	Total video supply current (V_{CC}+V_{CCB1}+V_{CCB2}+V_{CCB3}+V_{CCB4}+V_{CCB5})	V_{CC} = 5 V, no load, LPF OFF V_{CC} = 5 V, no load, LPF ON V_{CC} = 5 V, with load, LPF OFF V_{CC} = 5 V, with load, LPF ON		35 50 48 63	45 65 62 80	mA
I_{CC12}	12 V supply current	V_{CC12} = 12 V SLB input mode SLB output mode, no load		0 3	1 4	mA
Standby mode (all channels OFF + LPF OFF)						
I_{DD}	Digital supply current	V_{DD} = 5 V		6	10	mA
I_{CCAstd}	Audio supply current	V_{CCA0} = 12 V, no load		3		mA
I_{CCVstd}	Total video supply current	V_{CC} = 5 V		1		mA

2.3 Audio section characteristics

T_{AMB} = 25°C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V, R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

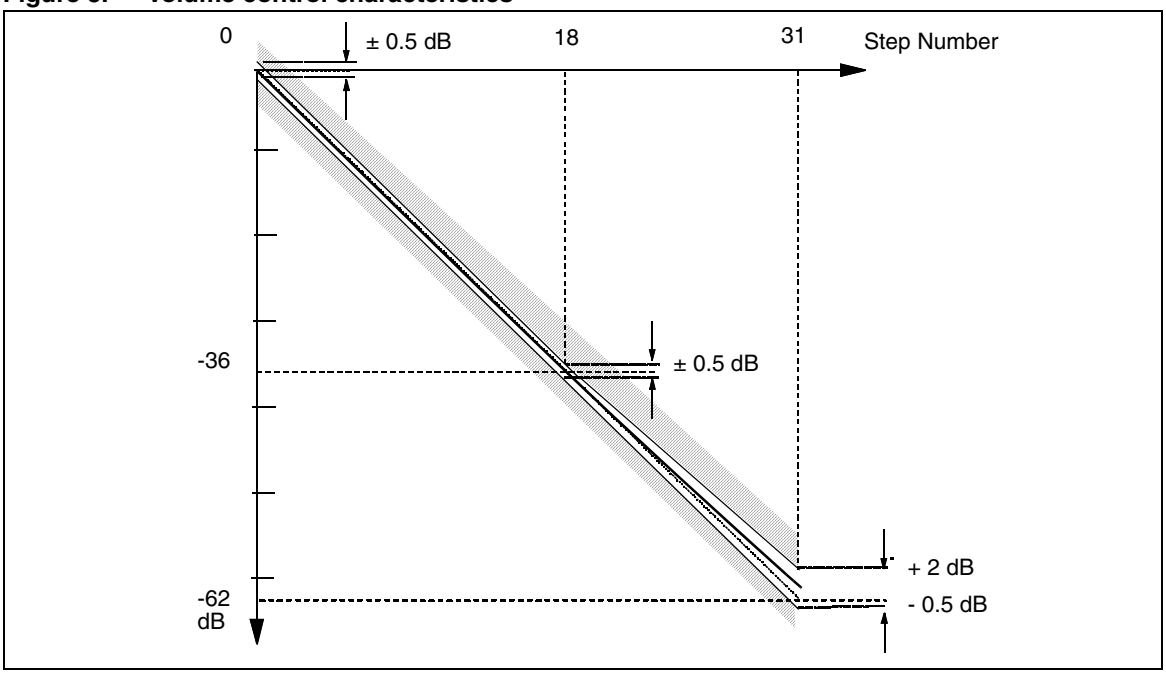
Table 6. Audio section characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SVR100	Supply voltage rejection	V_{RIPPLE} = 500 mV_{RMS} at 100 Hz, Gain= 0 dB DECA filter cap = 47 µF DECA filter cap = 220 µF	60	70 80		dB
SVR1K	Supply voltage rejection	V_{RIPPLE} = 500 mV_{RMS} at 1 kHz, Gain = 0 dB	70	80		dB
V_{INDC}	Input DC level			3.2		V
V_{INAC}	Input signal amplitude				2	V_{RMS}
R_{IN}	Input resistance		30	50		kΩ
$R_{INmatch}$	Input resistance matching			±2	±10	%
F_{RANGE}	Bandwidth	-3 dB, 0.5 V_{RMS}, R_{LOAD} = 10 kΩ, Gain = 0 dB	50			kHz
Flatness	Spread of gain in audio band	-0.5 V_{RMS}, 20 Hz to 20 kHz, Gain = 0 dB			0.5	dB

Table 6. Audio section characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
CS	Channel separation, from audio inputs Between L & R of TV outputs	V_{IN} = 0.5 V_{RMS} at 1 kHz on one input, R_{LOAD} = 10 kΩ, Gain = 0 dB	80 70	90 74		dB dB
Ci	Channel isolation from video inputs	V_{IN} = 1 V_{PP} at 15 kHz on one point		85		dB
V_{OUT}	Output DC level	V_{CCA} = 9 V		$V_{CCA/2}$		V
V_{OFF}	DC offset change	Switching between inputs		1	±15	mV
R_{OUT}	Output resistance			60	120	W
PHD	Phase difference	1 V_{RMS} input on each input channel at 1 kHz			3	° deg.
ASN	S/N ratio	V_{IN} = 1 V_{RMS} at 1 kHz input weighted CCIR 468-4 quasi peak, Gain = 0 dB	75	85		dB
eNI	Equivalent rms input voltage noise	BW = 20 Hz, 20 kHz Flat, Gain = 0 dB		5		µV
G0	0 dB gain	0.5 V_{RMS}, R_{LOAD} = 10 kΩ, Gain = 0 dB	-0.5		+0.5	dB
G_{STEP}	Gain step	-62 dB to +6 dB (see *Figure 5*)		2		dB
G_{MATCH1}	Gain matching between different inputs of one output	V_{IN} = 0.5 V_{RMS} at 1 kHz, Gain = 0 dB	-0.5		0.5	dB
G_{MATCH2}	Gain matching between left/right outputs of one input channel	V_{IN} = 0.5 V_{RMS} at 1 kHz, Gain = 0 dB	-0.5		0.5	dB
THD0 THD6 THD9	Total harmonic distortion ENC Input at 0 dB ENC Input at 6 dB ENC Input at 9 dB	V_{OUT} = 0.5 V_{RMS} at 1 kHz, LPF at 80 kHz, Volume level adjustment = 0 dB		 0.01 0.01 0.01	 0.05 0.05 0.05	%
V_{CL}	Output clipping level	THD = 0.2%, 1 kHz	2.1	2.3		V_{RMS}
R_L	Output load resistance	V_{IN} = 1 V_{RMS}, THD = 0.3%, Gain = 0 dB	2	2.25		kΩ
Mute	Mute suppression	V_{IN} = 0.5 V_{RMS}, on one point	-90			dB

Figure 5. Volume control characteristics



2.4 Video section characteristics

T_{AMB} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V, R_{LOUTA} = 10 kΩ, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 7. Video characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DCIN}	DC input level	Bottom sync pulse		2		V
I_{CLAMP}	Clamping current	at V_{DCIN} - 400 mV	1	2		mA
I_{LEAK}	Input leakage current	$V_{IN} = V_{DCIN}$ +1 V		1	10	µA
C_{IN}	Input capacitance			2		pF
V_{IN}	Max input signal	V_{CC} = 5 V			1.5	V_{PP}
DYN	Dynamic output signal	V_{CC} = 5 V			3	V_{PP}
BW	Bandwidth at -3 dB - Y/CVBS - RGB	Input without low pass filter V_{IN} = 1 V_{PP} V_{IN} = 1 V_{PP} V_{INC} = muted	 10 10	 15 15		MHz
Flatness	Spread of gain in video band (15 kHz - 20 MHz) - Y/CVBS - RGB	Input without low pass filter V_{IN} = 1 V_{PP} V_{IN} = 1 V_{PP}, V_{INC} = muted			 +/-0.5 +/-0.5	dB
BW LPF	Low pass filter bandwidth at -3dB	V_{IN} = 1 V_{PP}, CL=10pF		7.5		Mhz
ATT	Low pass filter attenuation	27 MHz		-47	-36	dB

Table 7. Video characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
CTi	Crosstalk isolation between input channel	V_{IN} = 1 V_{PP} at 4.43 MHz on one point		60		dB
CTo	Crosstalk Isolation between output channel	V_{IN} = 1 V_{PP} at f = 4.43 MHz, on one point, R_{LOAD} = 150Ω		50		dB
R_{OUT}	Output resistance			5	10	Ω
G_{RGB}	Gain at RGB outputs	V_{IN} = 1 $V_{pp,}$ gain = 6 dB	5.5	6	6.5	dB
G_{RGBM}	Gain matching between R, G, B	V_{IN} = 1 $V_{pp,}$ gain = 6 dB	-0.3	0	0.3	dB
$G_{RGBSTEP}$	Step of gain	3 dB to 6 dB	0.75	1	1.25	dB
G_{YCVBS}	Gain on Y,/CVBS channels	V_{IN} = 1 V_{PP}	5.5	6	6.5	dB
G_{YCVBSM}	Gain matching between Y, CVBS inputs	V_{IN} = 1 V_{PP}	-0.5	0	0.5	dB
DC_{OUT}	DC output voltage	Bottom sync pulse		0.6		V
DPHI	Differential phase	V_{IN} = 1 V_{PP} at 4.43 MHz		1	5	° deg.
DG	Differential gain	V_{IN} = 1 V_{PP} at 4.43 MHz		1	5	%
Mute	Mute suppression	V_{IN} = 1 V_{PP} at 5 MHz on one point	-55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video S/N Ratio	Refer to note below	65			dB

Note: S/N = 20 log (V_{OUT} black to white = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) weighted CCIR 567).

2.5 Chroma section characteristics

T_{AMB} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V, R_{LOUTA} = 10 kΩ, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 8. Chroma section characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DCIN}	DC input level			3		V
R_{IN}	Input resistance		30	50		kΩ
C_{IN}	Input capacitance			2		pF
V_{IN}	Max input signal				1.5	V_{PP}
DYN	Dynamic output signal				3	V_{PP}
DC_{OUT}	DC output VCR voltage			2.2		V
CBW	Chroma bandwidth	C_{IN} = 1 V_{PP} at -3 db	10	15		MHz
CTi	Crosstalk isolation between input channel	V_{IN} = 1 V_{PP} at 4.43 MHz on one input		55		dB

Table 8. Chroma section characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
CTo	Crosstalk isolation between output channel	V_{IN} = 1 V_{PP} at 4.43 MHz on one input, R_{LOAD} = 150 Ω		50		dB
R_{OUT}	Output resistance			5	10	W
G_{OUTC}	Gain at OUTC	V_{IN} = 1 V_{pp}	5.5	6	6.5	dB
G_{CM}	Gain matching between C inputs	V_{IN} = 1 V_{PP}	-0.5	0	0.5	dB
Mute	Mute suppression	V_{IN} = 1 V_{PP} at 4.43 MHz on one input	55			dB
CToYdel	Chroma to luma delay, source Y/C	V_{PP} at 4.43 MHz			20	ns
Z_{COUT_VCR}	Output impedance when switched to ground	2.7V applied to COUT_VCR with series 75Ω Resistor		2		W

2.6 Blanking section

T_{AMB} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V, R_{LOUTA} = 10 kΩ, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 9. Slow blanking section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Input mode						
SLBlow	Input low level threshold		2.5	3.25	4	V
SLBhigh	Input high level threshold		7.5	8.25	9	V
I_{IN}	Input current			50	100	µA
Output mode						
SLBlow	Output low level (int. TV)		0	0.02	1.5	V
SLBmed	Output medium level (ext. 16/9)		5	5.75	6.5	V
SLBhigh	Output high level (ext. 4/3)		10	11	12	V

Table 10. Fast blanking section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Input mode						
FBlow/high	Input low/high level threshold		0.4	0.7	0.9	V
I_{IN}	Input current			2	10	µA
Output mode						
FB_{LOW}	Output Low Level	R_{LOAD} = 150 Ω			0.5	V
FB_{HIGH}	Output High Level		3.0	3.4	3.8	V

Table 10. Fast blanking section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
FB_{DEL}	Fast Blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, C_{LOAD} = 10pF maximum		15		ns
FB_{TRANS}	FB Transitions at FB output Rise Time Fall Time	C_{LOAD} = 10 pF maximum between 10% and 90% between 90% and 10%		 10 10		 ns ns

Table 11. Interrupt output

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
IT-Leak	High level leakage	External pull-up to 5 V			10	µA
IT-Low	Output low level (active)	I_{IN} = 0 mA I_{IN} = 1 mA			0.3 0.7	V V

Note: The interrupt is forced low when a change is detected on slow blanking inputs. It can be used in standby mode to wake up the microprocessor. It is released when the I²C bus register is read.

Table 12. Address selection input

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ADDsel_L	Address selection low level			0	0.2	V
ADDsel_H	Address selection high level		2.5		V_{DD}	V
I_{LEAK}	Leakage current				10	µA

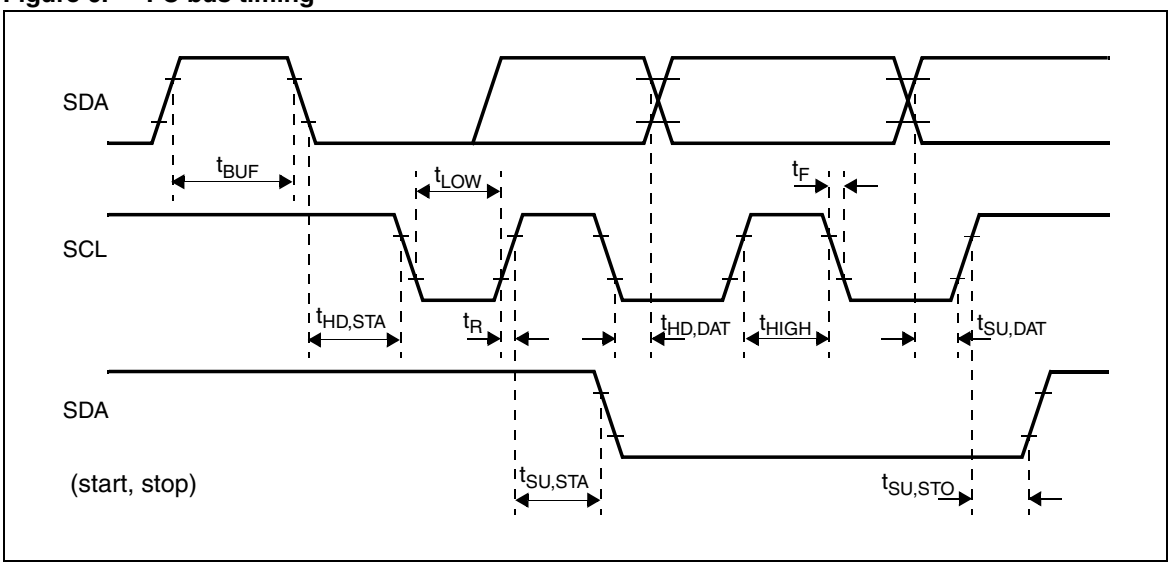
2.7 I²C bus characteristics

T_{AMB} = 25°C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V, R_{LOUTA} = 10kΩ, R_{LOUTV} = 150Ω, unless otherwise specified.

Table 13. I²C bus characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SCL						
V_{IL}	Low level input voltage		-0.3		1.5	V
V_{IH}	High level input voltage		2.3		5.5	V
I_{LI}	Input leakage current	V_{IN} = 0 to 5.5 V	-10	0	10	µA
f_{SCL}	Clock frequency				400	kHz
t_R	Input rise time	1.5 V to 3 V			1	µs
t_F	Input fall time	1.5 V to 3 V			300	ns
C_I	Input capacitance				10	pF
SDA						
V_{IL}	Low level input voltage		-0.3		1.5	V
V_{IH}	High level input voltage		2.3		5.5	V
I_{LI}	Input leakage current	V_{IN} = 0 to 5.5 V	-10	0	10	µA
C_I	Input capacitance				10	pF
t_R	Input rise time	1.5 V to 3 V			1	µs
t_F	Input fall time	3 V to 1.5 V			300	ns
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.4	V
t_F	Output fall time	3 V to 1.5 V			250	ns
C_L	Load capacitance				400	pF
Timing: SCL frequency = 400 kHz						
t_{LOW}	Clock low period		1.3			µs
t_{HIGH}	clock high period		0.6			µs
$t_{SU,DAT}$	Data setup time		100			ns
$t_{HD,DAT}$	Data hold time		0		340	ns
$t_{SU,STO}$	Setup Time from clock high to stop		0.6			µs
t_{BUF}	Start setup time following a stop		1.3			µs
$t_{HD,STA}$	Start hold time		0.6			µs
$t_{SU,STA}$	Start setup time following clock low to high transition		0.6			µs

Figure 6. I²C bus timing



3 I²C bus selection

Data transfers follow the usual I²C format; that is, after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I²C bus decoder enables the automatic incrementation mode in write mode.

The circuit operates at clock frequencies of up to 400 kHz.

Table 14. String format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	SLAVE ADDRESS	0	A	SUB-ADDRESS	A	DATA	A	P

Table 15. Read only mode

S	SLAVE ADDRESS	1	A	DATA	A	P

Table 16. Slave address

Address	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	1	0	1	X

Table 17. Auto increment mode

S	SLAVE ADDRESS	0	A	SUB-ADDRESS	A	DATA0	A	DATA1	A	....	DATAn	A	P
						Sub-Address		Sub-Address +1			Sub-Address + N		

3.1 I²C bus addresses

Write Address: 1001 0110 = 96(hex), Read Address: 1001 0111 = 97(hex)

Table 18. Input signal summary (write mode)

Reg add (hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
Audio								
00h	TV Stereo Mono	TV 0/6 dB	TV Volume-62 dB to 0 dB - 2 dB steps					Soft Volume Mode
01h	VCR Stereo Mono	Not Used *(See Note)*	VCR Audio Switch Control		CINCH Audio Gain	TV/CINCH Audio Switch Control		
Video								

Table 18. Input signal summary (write mode) (continued)

Reg add (hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
02h	VCR chroma muted	VCR video and chroma switch control			TV chroma muted	TV video and chroma switch control		
03h	RGB and FB tri-state	RGB gain			RGB switch control		Fast blanking mode/input selection	
Miscellaneous								
04h	IT enable	SLB mode	LPF enable	VCR-C output control		Not used *(see Note)*	Not used *(see Note)*	TV R or C output selection
05h	VCR slow blanking		TV slow blanking		ENC audio input gain 0/6/9 dB		VCR R/C sub clamp	ENC R/C sub clamp
Standby								
06h	Not used *(see Note)*	TV outputs	CINCH outputs	VCR outputs	Not used *(see Note)*	TV inputs	VCR inputs	ENC inputs

Note: At register address 06h, bits marked "Not used" must be set to "1". All other bits from all other registers marked "Not used" must be set to "0".

Table 19. TV audio output

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
00h	Soft volume change	1	X X	X X	X X	X X	X X	X X	X X	0 1	Active Disabled
	Level adjustment	5	X X	X X	0 1	0 1	0 1	0 1	0 1	X X	0 dB -62 dB (-2 dB/step)
	6 dB extra gain	1	X X	0 1	X X	X X	X X	X X	X X	X X	0 dB +6 dB
	TV stereo or mono mode	1	0 1	X X	X X	X X	X X	X X	X X	X X	0 = stereo 1 = mono

Table 20. Audio selection and VCR audio output

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
01h	TV & CINCH audio output selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	Encoder L/R selected
			X	X	X	X	X	0	1	0	VCR L/R selected
			X	X	X	X	X	0	1	1	Not allowed
			X	X	X	X	X	1	0	0	TV L/R selected
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
			X	X	X	X	X	1	1	1	Not allowed
	CINCH audio gain	1	X	X	X	X	0	X	X	X	0 dB
			X	X	X	X	1	X	X	X	Follow TV gain
	VCR audio output selection	2	X	X	0	0	X	X	X	X	Muted
			X	X	0	1	X	X	X	X	Encoder L/R selected
			X	X	1	0	X	X	X	X	TV L/R selected
			X	X	1	1	X	X	X	X	Not allowed
	VCR stereo or mono mode	1	0	X	X	X	X	X	X	X	0 = stereo
			1	X	X	X	X	X	X	X	1 = mono

Table 21. TV and VCR video selection

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02h	TV video output selection	3	X X X X X X X X	X X X X X X X X	X X X X X X X X	X X X X X X X X	X X X X X X X X	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Y/CVBS muted & chroma muted Y/CVBS_ENC & R/C_ENC Y_ENC & C_ENC Y/CVBS_VCR & R/C_VCR Not allowed Not allowed Not allowed Not allowed
	TV chroma output control	1	X X	X X	X X	X X	0 1	X X	X X	X X	Chroma defined by d2d1d0 Chroma force to mute
	VCR video output selection	3	X X X X X X X X	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	X X X X X X X X	X X X X X X X X	X X X X X X X X	X X X X X X X X	Y/CVBS muted & chroma muted Y/CVBS_ENC & R/C_ENC Y_ENC & C_ENC CVBS_TV & chroma muted Not allowed Not allowed Not allowed Not allowed
	VCR chroma output control	1	0 1	X X	X X	X X	X X	X X	X X	X X	Chroma defined by d6d5d4 Chroma force to mute

Table 22. RGB and fast blanking outputs

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03h	Fast blanking control	2	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	0 0 1 1	0 1 0 1	FB forced to low level FB forced to high level FB from Encoder FB from VCR
	RGB selection	2	X X X X	X X X X	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	Muted RGB_ENC selected RGB_VCR selected Not allowed
	RGB gain	2	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	+6 dB gain +5 dB gain +4 dB gain +3 dB gain
		1	X X	0 1	X X	X X	X X	X X	X X	X X	+0 dB extra gain +3 dB for weak input signals
	RGB and FB control	1	0 1	X X	X X	X X	X X	X X	X X	X X	RGB and FB outputs high impedance state RGB and FB outputs active

Table 23. Miscellaneous control

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
04h	R/C TV output selection	1	X X	X X	X X	X X	X X	0 0	0 0	0 1	Red signal selected Chroma signal selected
	Not used	2	X	X	X	X	X	X	X	X	Not used
	C_VCR output control	2	X X X	X X X	X X X	0 0 1	0 1 X	0 0 0	0 0 0	X X X	Grounded Tri-state mode (high impedance) Active
	Low pass filters control	1	X X	X X	0 1	X X	X X	0 0	0 0	X X	LPF enabled LPF disabled
	Slow blanking mode	1	X X	0 1	X X	X X	X X	0 0	0 0	X X	Normal mode SLB TV is driven by SLB VCR
	IT enable	1	0 1	X X	X X	X X	X X	0 0	0 0	X X	No iterrupt flag IT enable

Table 24. Slow blanking and inputs control

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
05h	Encoder R/Csub clamp	1	X X	X X	X X	X X	X X	X X	X X	0 1	Bottom level clamp Average level clamp
	VCR R/Csub clamp	1	X X	X X	X X	X X	X X	X X	0 1	X X	Bottom level clamp Average level clamp
	Encoder input level adjustment	2	X X X	X X X	X X X	X X X	0 0 1	0 1 0	X X X	X X X	0 dB for normal audio inputs +6 dB for weak audio inputs +9 dB for weak audio inputs
	Slow blanking TV SCART	2	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format
	Slow blanking VCR SCART	2	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format

Table 25. Standby modes

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
06h	ENC inputs	1	1 1	X X	X X	X X	1 1	X X	X X	0 1	Inputs active Inputs disabled
	VCR inputs	1	1 1	X X	X X	X X	1 1	X X	0 1	X X	Inputs active Inputs disabled
	TV inputs	1	1 1	X X	X X	X X	1 1	0 1	X X	X X	Inputs active Inputs disabled
	VCR outputs	1	1 1	X X	X X	0 1	1 1	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	CINCH outputs	1	1 1	X X	0 1	X X	1 1	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	TV outputs	1	1 1	0 1	X X	X X	1 1	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	Full stop		1	1	1	1	1	1	1	1	Only I²C bus and slow blanking detection parts are supplied.

Table 26. Output signals (read mode)

Reg add (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
	Slow blanking TV SCART	2	X X X	X X X	X X X	X X X	X X X	X X X	0 1 1	1 0 1	Input < 2 V Input 16/9 format Input 4/3 format
	Slow banking VCR SCART	2	X X X	X X X	X X X	X X X	0 1 1	1 0 1	X X X	X X X	Input < 2 V Input 16/9 format Input 4/3 format
	Interrupt flag	1	X X	X X	X X	0 1	X X	X X	X X	X X	No change since read One change has been detected *(refer to Note)*

Note: The interrupt flag will be cleared when this register is read. To prepare for a new interrupt, a "1" must be re-written in the IT Enable bit (Reg. 04, d7).

4 Input/output groups

Figure 7. Bottom clamped video inputs (pins 2, 4, 6, 12, 14, 18, 21, 62, and 64)

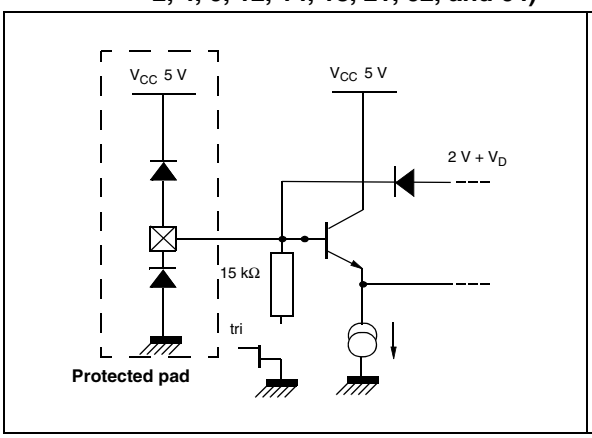


Figure 8. Average clamped video inputs (pin 8)

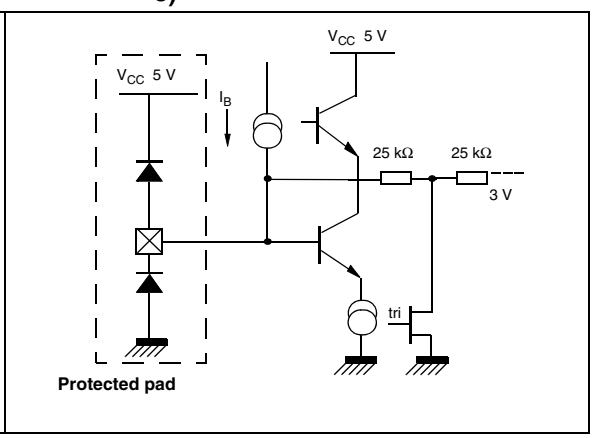


Figure 9. R/C clamped video inputs (pins 10 and 60)

R/C inputs may be configured either as a bottom clamped input or as an average clamped input. In either case, the simplified input schematic is very close to one of the graphics shown above.

Figure 10. Fast blanking output (pin 49)

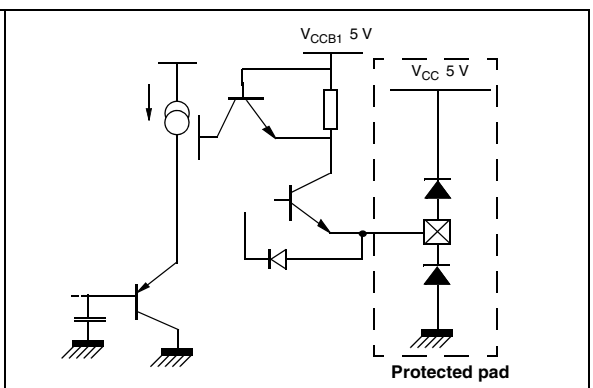


Figure 11. Fast blanking inputs (pins 50 and 51)

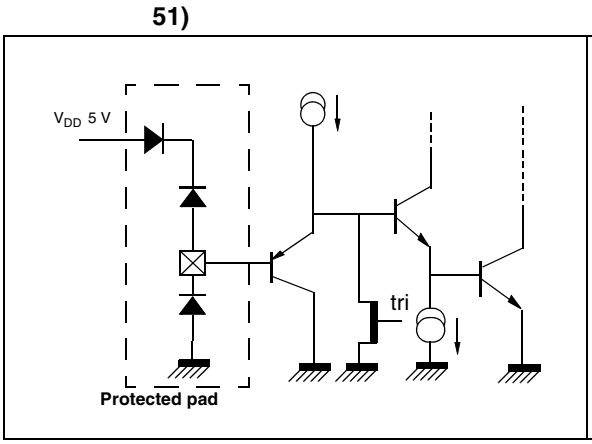


Figure 12. Video outputs (pins 36, 38, 40, 42, 44, 46, and 48)

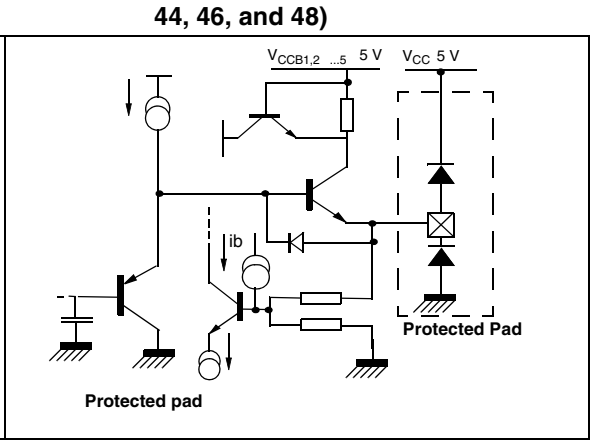


Figure 13. Audio inputs (pins 7, 9 11, 13, 19, 20, 22, and 23)

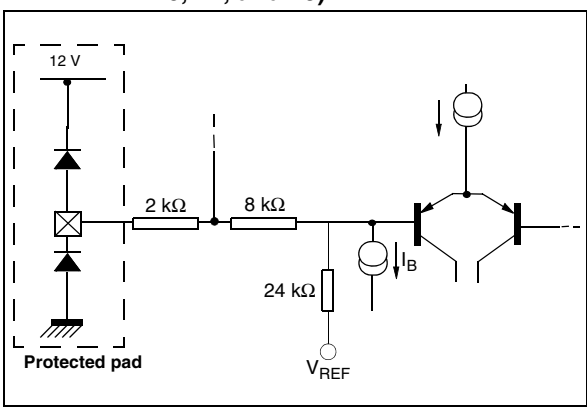


Figure 14. Audio outputs (pins 27, 28, 29, 30, 32, 33, and 35)

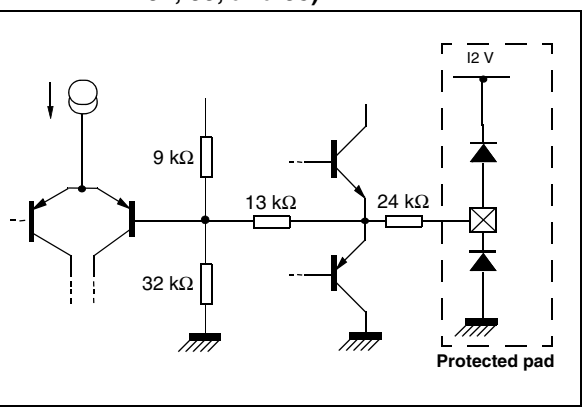


Figure 15. Slow blanking I/O (pins 59 and 61)

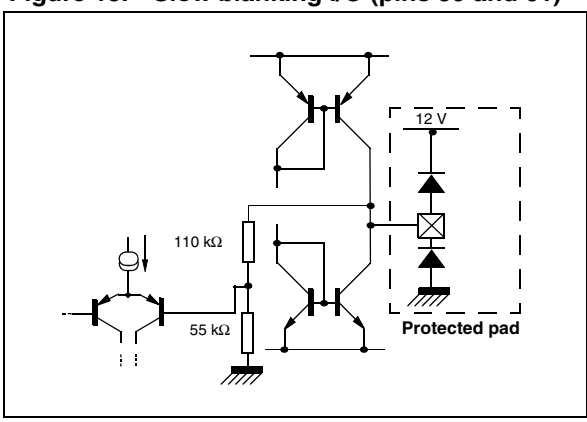


Figure 16. Interrupt output (pin 58)

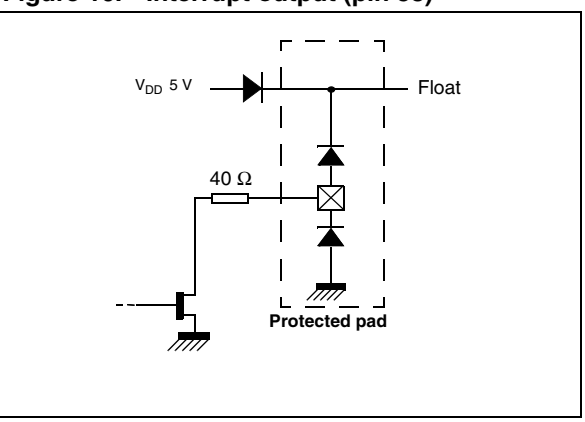


Figure 17. Trap filter (pin 34)

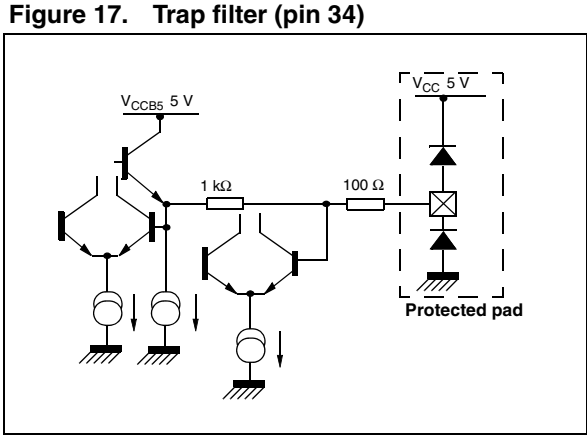


Figure 18. I²C bus (SDA) (Pin 56)

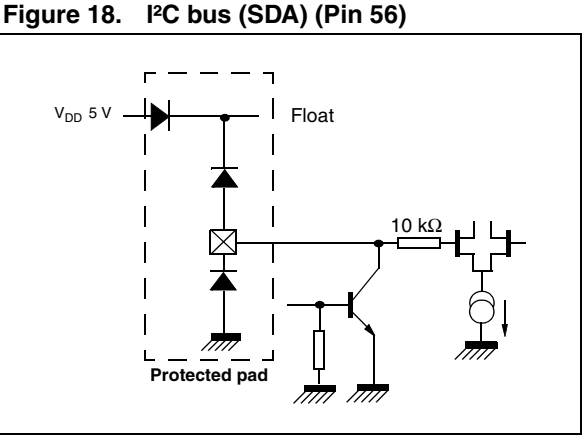


Figure 19. I²C bus (ADD) (pin 54)

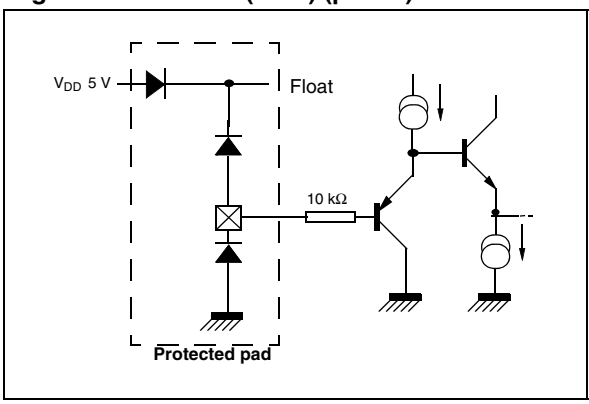


Figure 20. I²C bus (SCL) (pin 55)

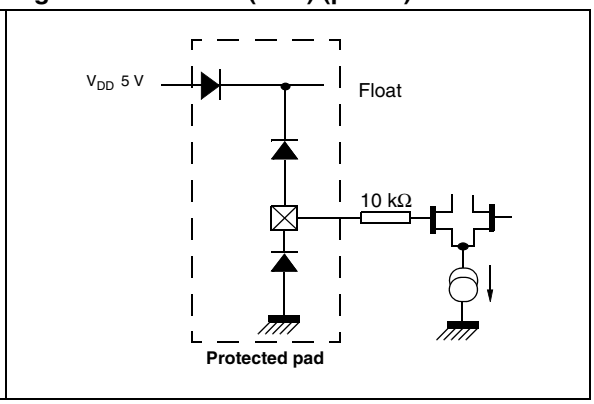
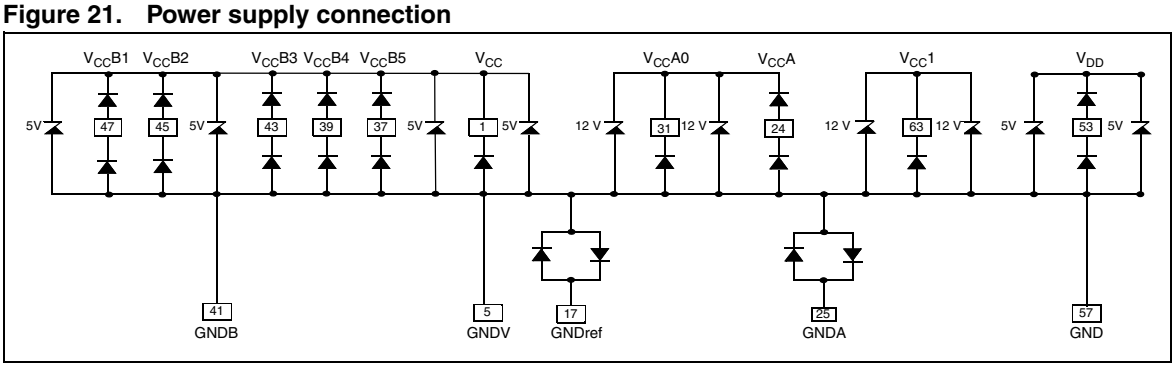


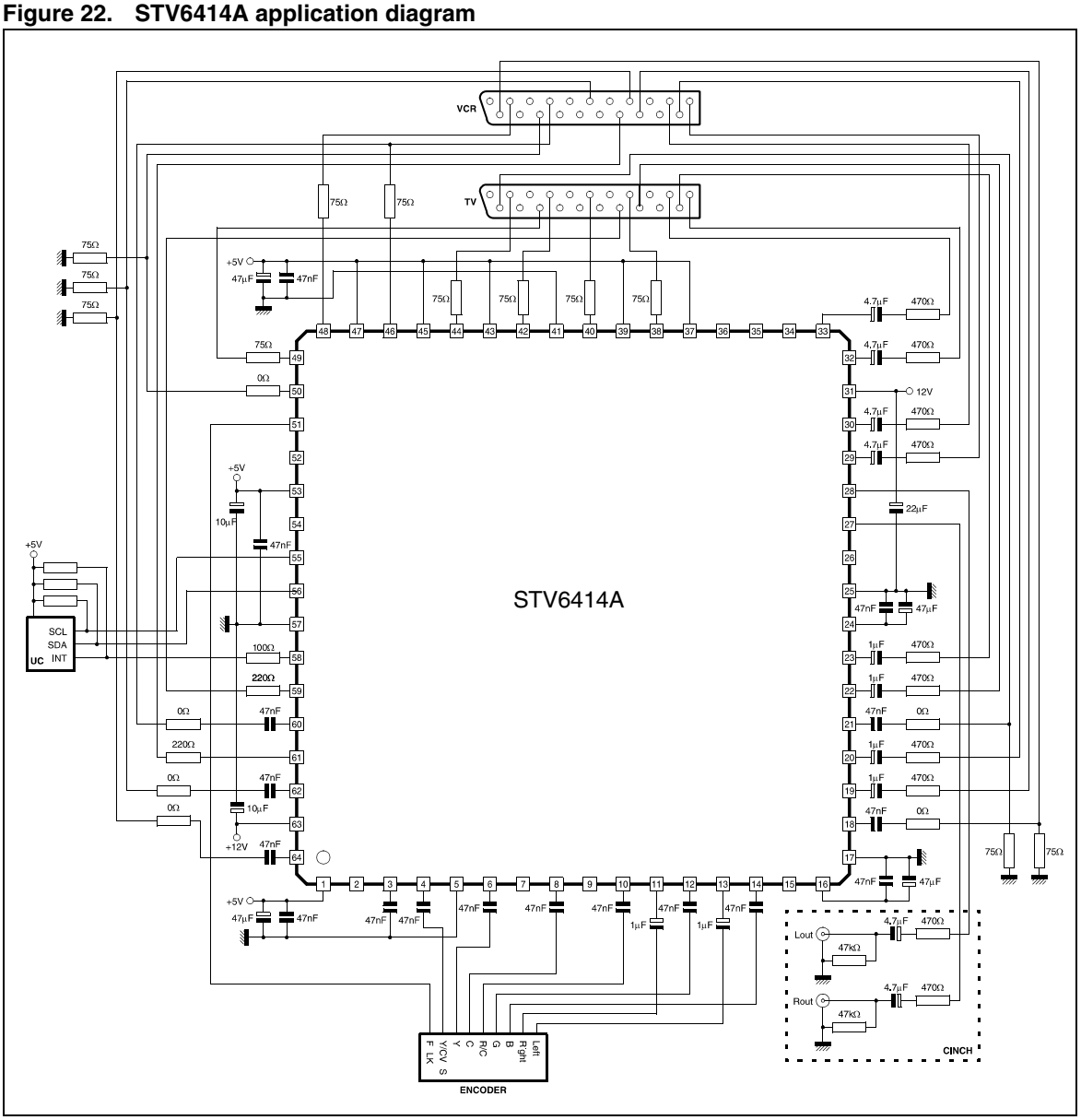
Figure 21. Power supply connection



5 Application diagram

Note: The application diagram presented here is an example only and is subject to change without notice. The real application diagram will depend on application conditions and constraints.

Figure 22. STV6414A application diagram



6 Package mechanical data

Figure 23. 64 pin, LQFP64 (low-profile quad flat package) 10 x10 x 1.4 mm

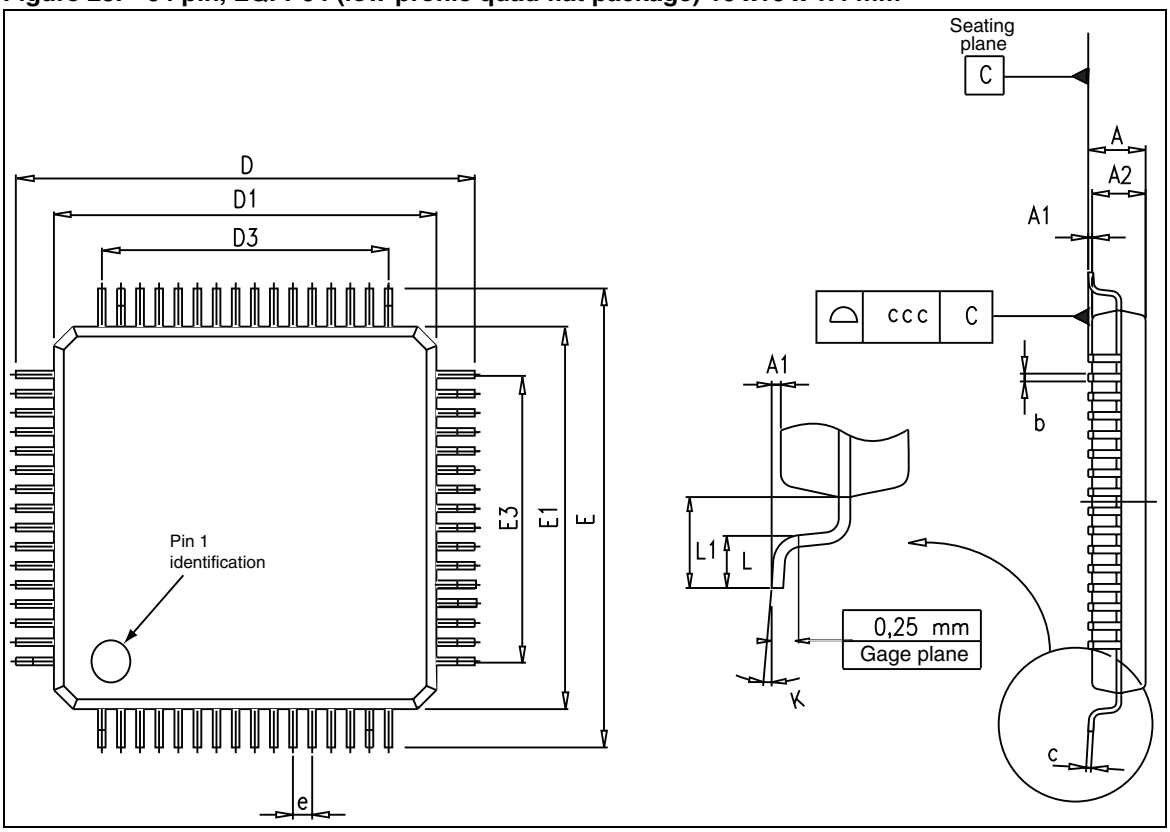


Table 27. LQFP64 package dimensions

Dimension	Millimeters			Inches		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			1.60			0.063
A1	0.05		0.15	0.002		0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09		0.20	0.003		0.0078
ccc			0.08			0.0031
D	11.80	12.00	12.20	0.464	0.472	0.48
D1	9.80	10.00	10.20	0.385	0.393	0.401
D3		7.50			0.295	
E	11.0	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.385	0.393	0.401

Table 27. LQFP64 package dimensions (continued)

Dimension	Millimeters			Inches		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
E3		7.50			0.295	
e		0.50			0.019	
L	0.45	0.60	0.75	0.017	0.023	0.029
L1		1.00			0.039	
Degrees						
K	0° minimum 3.5° typical 7° maximum					

6.1 Lead-free packaging

To meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com.*

Revision history

Table 28. Document revision history

Date	Revision	Changes
26-Jun-2008	1	Initial release

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