

2SJ244

Silicon P Channel MOS FET

REJ03G0853-0200
(Previous: ADE-208-1187)
Rev.2.00
Sep 07, 2005

Description

High speed power switching

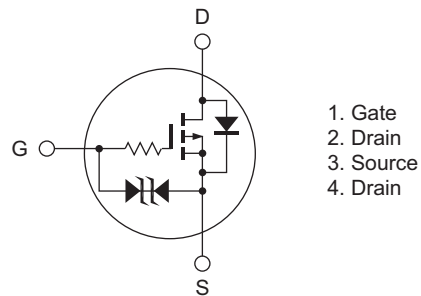
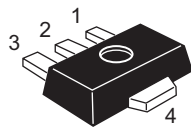
Low voltage operation

Features

- Very Low on-resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK®)



Note: Marking is "JY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-12	V
Gate to source voltage	V _{GSS}	±7	V
Drain current	I _D	±2	A
Drain peak current	I _{D (pulse)} ^{Note 1}	±4	A
Channel dissipation	P _{ch} ^{Note 2}	1	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 100 μs, duty cycle ≤ 10%

2. Value on the alumina ceramic board (12.5 × 20 × 0.7 mm)

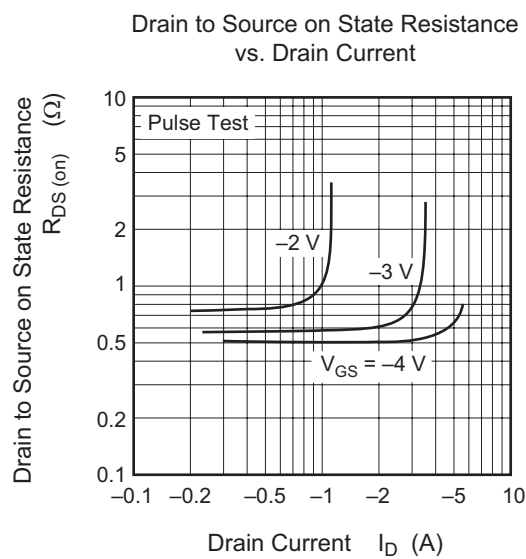
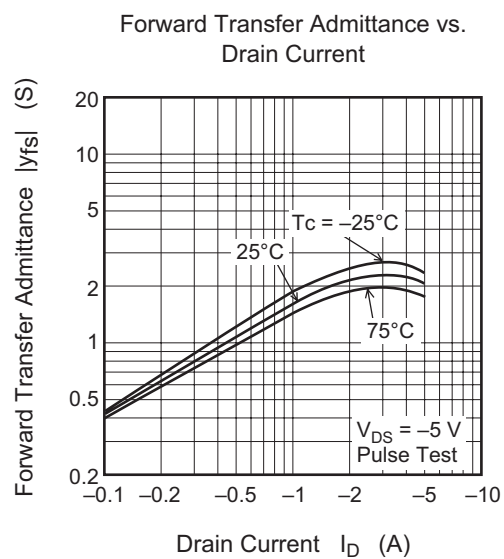
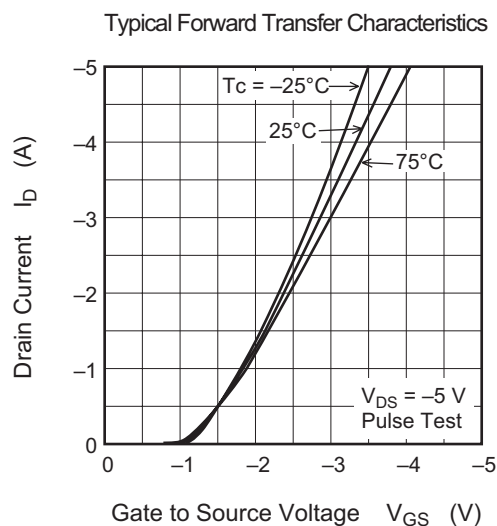
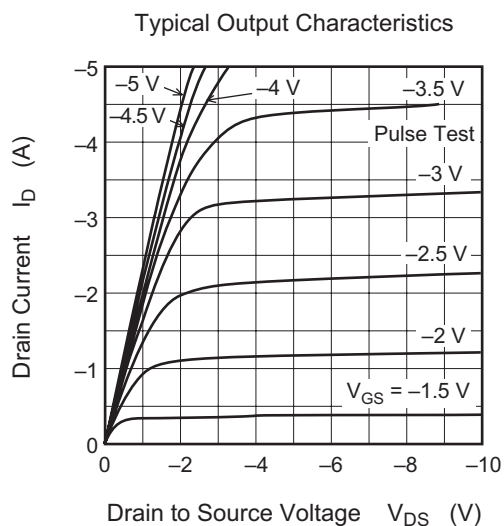
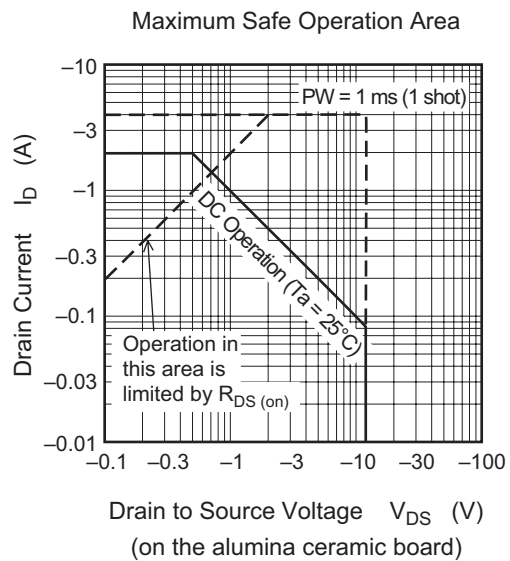
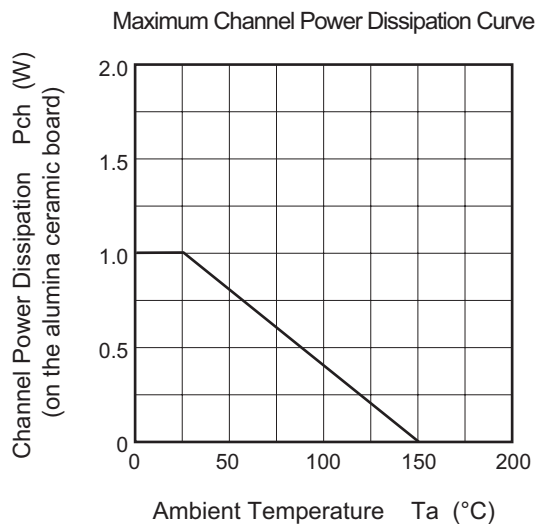
Electrical Characteristics

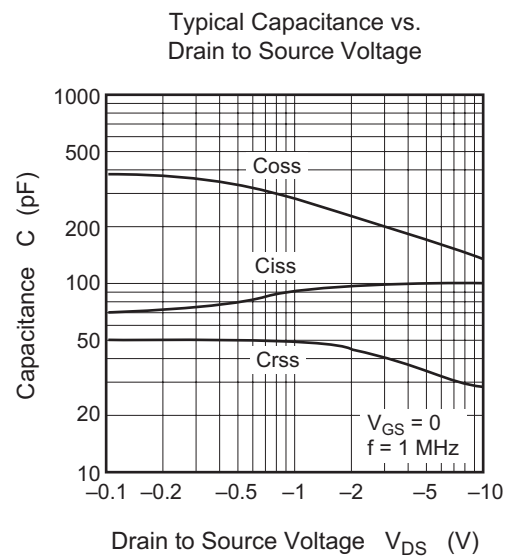
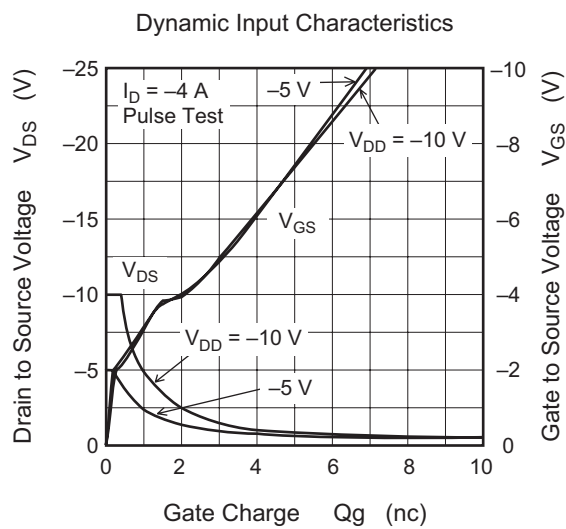
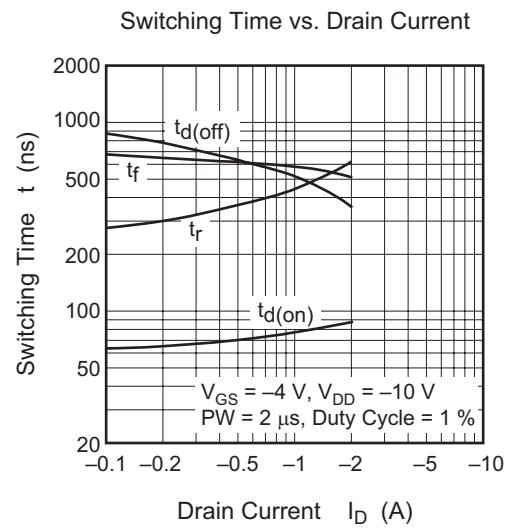
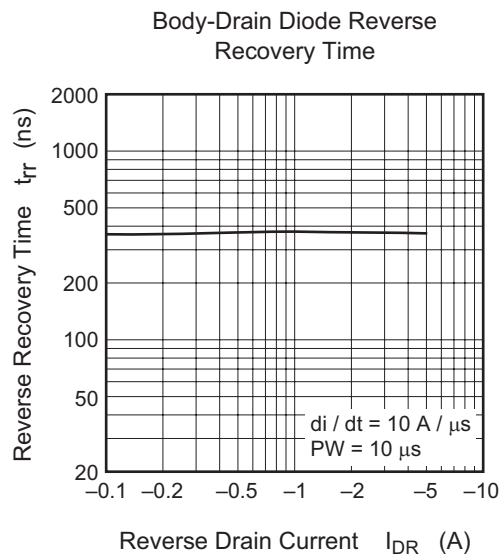
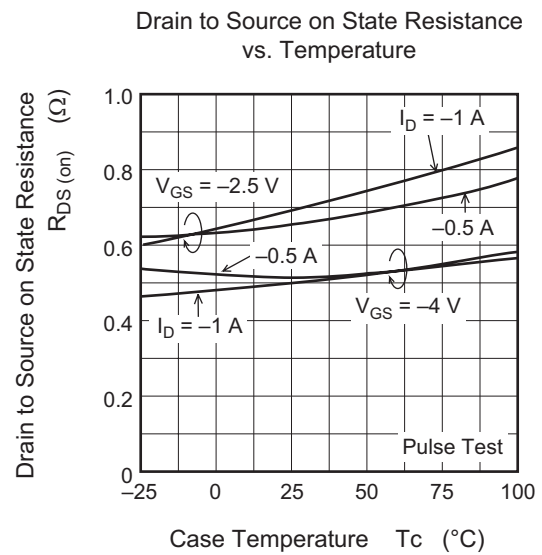
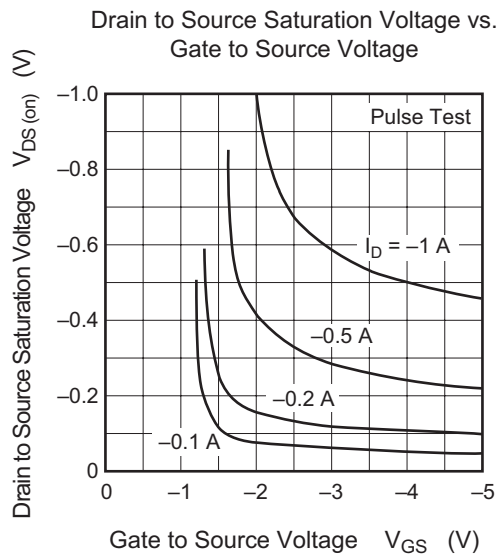
(Ta = 25°C)

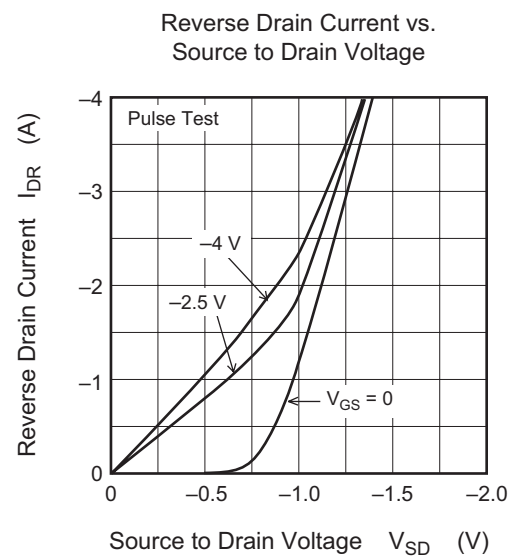
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-12	—	—	V	I _D = -1 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±7	—	—	V	I _G = ±10 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±5	μA	V _{GS} = ±6 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-1	μA	V _{DS} = -8 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-0.4	—	-1.4	V	I _D = -100 μA, V _{DS} = -5 V
Static drain to source on state resistance	R _{DS (on) 1}	—	0.65	0.9	Ω	I _D = -0.5 A, V _{GS} = -2.5 V ^{Note 3}
	R _{DS (on) 2}	—	0.5	—	Ω	I _D = -1 A, V _{GS} = -4 V ^{Note 3}
Forward transfer admittance	y _{fs}	—	1.8	—	S	I _D = -1 A, V _{DS} = -5 V ^{Note 3}
Input capacitance	C _{iss}	—	100	—	pF	V _{DS} = -5 V
Output capacitance	C _{oss}	—	168	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	35	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	365	—	ns	I _D = -0.2 A ^{Note 3}
Turn-off delay time	t _{d (off)}	—	1450	—	ns	V _{in} = -4 V, R _L = 51 Ω
Body to drain diode forward voltage	V _{DF}	—	—	7	V	I _F = 4 A ^{Note 3} , V _{GS} = 0

Note: 3. Pulse test

Main Characteristics







Package Dimensions

JEITA Package Code	RENEAS Code	Package Name	MASS[Typ.]	Unit: mm
SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g	

The drawing shows three views of the package: a top view, a side view, and an end view. The top view shows a rectangular package with a central circular feature of diameter 1.0 mm. Dimensions include a total width of 4.5 ± 0.1 mm, a maximum width of 1.8 mm for the central feature, a height of 0.4 mm, and a maximum height of 2.5 ± 0.1 mm. The side view shows a maximum width of 1.5 ± 0.1 mm and a maximum height of 0.44 mm. The end view shows a maximum width of 1.5 mm and a maximum height of 0.4 mm. The bottom view shows a maximum width of 3.0 mm and a minimum height of 0.8 mm.

Ordering Information

Part Name	Quantity	Shipping Container
2SJ244JYTL-E	1000 pcs	Taping
2SJ244JYTR-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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