

2SJ518

Silicon P Channel MOS FET

REJ03G0875-0400

(Previous: ADE-208-580B)

Rev.4.00 Sep 07, 2005

Description

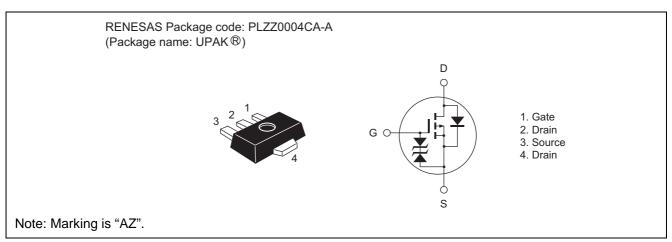
High speed power switching

Features

• Low on-resistance $R_{DS\,(on)} = 0.35~\Omega~typ.~(at~V_{GS} = -10~V,~I_D = -1~A)$

- Low drive current
- 4 V gate drive devices
- High speed switching

Outline



*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-2	Α
Drain peak current	I _{D (pulse)} Note 1	-4	Α
Body to drain diode reverse drain current	I _{DR}	-2	Α
Avalanche current	I _{AP} Note 2	-2	Α
Avalanche energy	E _{AR}	0.34	mJ
Channel dissipation	Pch Note 3	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. PW \leq 10 μ s, duty cycle \leq 1%

2. Value at Tch = 25°C, Rg \geq 50 Ω

3. Value at when using the aluminum ceramic board (12.5 \times 20 \times 0.7 mm)

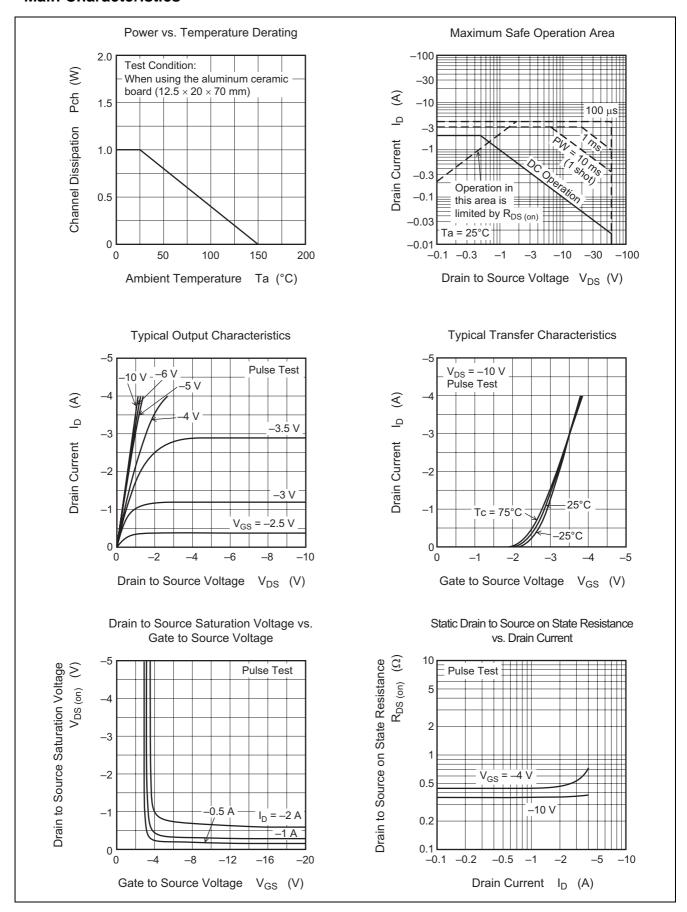
Electrical Characteristics

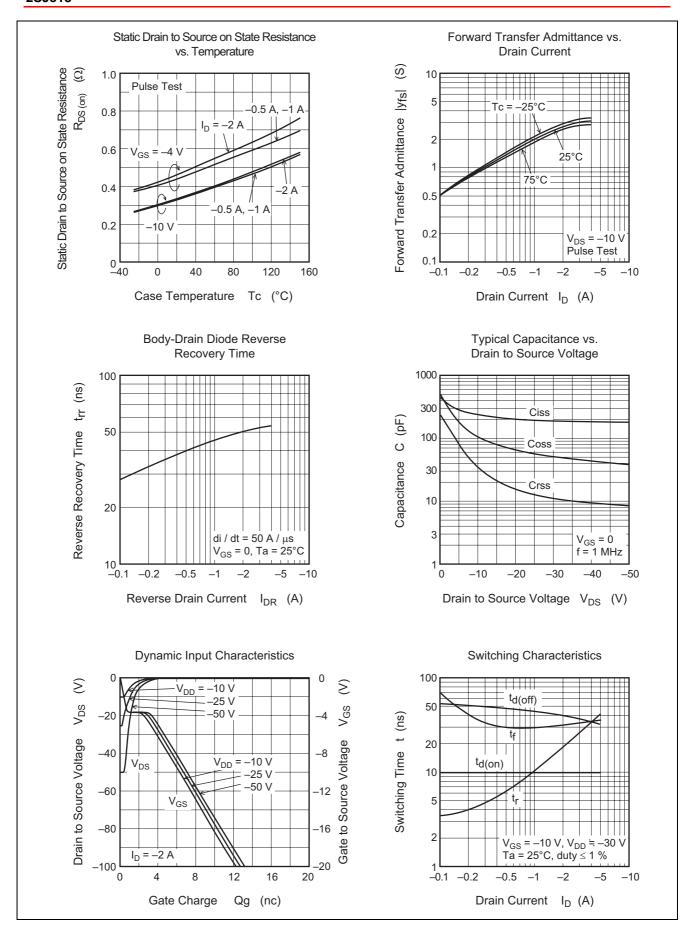
 $(Ta = 25^{\circ}C)$

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-60	_	_	V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	V _{(BR) GSS}	±20	_	_	V	$I_G = \pm 100 \ \mu A, \ V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	_	-10	μΑ	$V_{DS} = -60 \text{ V}, V_{GS} = 0$
Gate to source leak current	I _{GSS}	_	_	±10	μΑ	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Gate to source cutoff voltage	V _{GS (off)}	-1.0	_	-2.0	V	$I_D = -1 \text{ mA}, V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	R _{DS (on)}	_	0.35	0.46	Ω	$I_D = -1 \text{ A}, V_{GS} = -10 \text{ V}^{\text{Note 4}}$
	R _{DS (on)}	_	0.45	0.63	Ω	$I_D = -1 \text{ A}, V_{GS} = -4 \text{ V}^{\text{Note 4}}$
Forward transfer admittance	y _{fs}	1.2	2.0	_	S	$I_D = -1 \text{ A}, V_{DS} = -10 \text{ V}^{\text{Note 4}}$
Input capacitance	Ciss	_	220	_	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	Coss	_	110	_	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	35	_	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	_	10	_	ns	V _{GS} = -10 V
Rise time	t _r	_	11	_	ns	$I_{D} = -1 A$
Turn-off delay time	t _{d (off)}	_	45	_	ns	$R_L = 30 \Omega$
Fall time	t _f	_	30	_	ns	
Body to drain diode forward voltage	V_{DF}	_	-1.05	_	V	$I_F = -2 A, V_{GS} = 0$
Body to drain diode reverse recovery time	t _{rr}	_	50	_	ns	$I_F = -2 A, V_{GS} = 0$
						di _F /dt = 50 A/μs

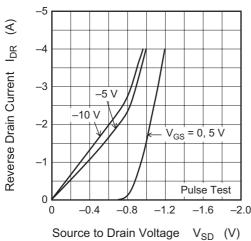
Note: 4. Pulse test

Main Characteristics

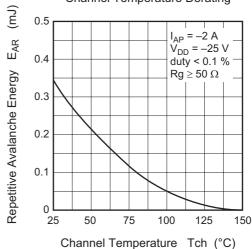




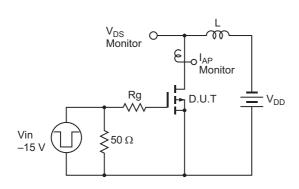
Reverse Drain Current vs. Source to Drain Voltage



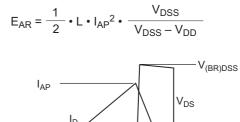
Maximum Avalanche Energy vs. Channel Temperature Derating

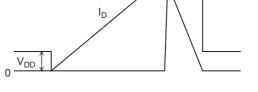


Avalanche Test Circuit

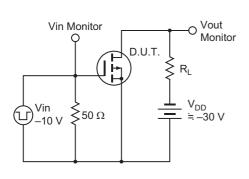


Avalanche Waveform

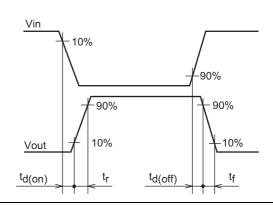




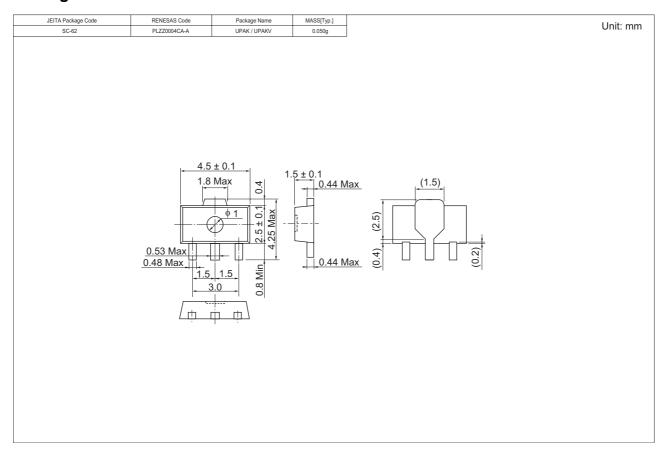
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ518AZTL-E	1000 pcs	Taping
2SJ518AZTR-E	1000 pcs	Taping

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Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia Tel: <603> 7955-9390, Fax: <603> 7955-9510