R8A66120FFA

4M-bit x 2 MULTIPLE FIELD MEMORY

REJ03F0161-0170
Rev.1.70
May.16.2008

Description

R8A66120FFA is high-speed field memory with two FIFO (First In First Out) memories of 4M-bit, which uses high-performance silicon gate process technology.

Features

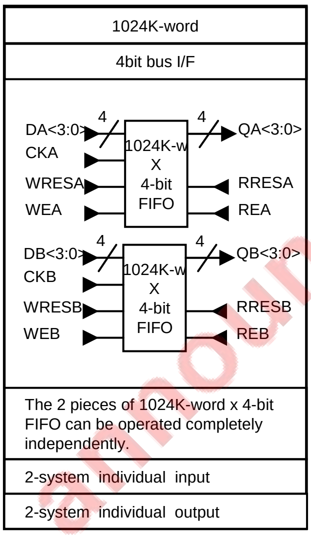
•Total memory Capacity	8Mega-bit	
•High speed operation		
cycle time	10.0ns(Min.)	fmax = 100MHz
output access time	6.0ns(Max.)	
•Output hold time	1.0ns(Min.)	
•Supply voltage	3.3 ± 0.3V	
•Variable length delay bit		
•Synchronous write/read operation		
•3 states output		
•Package	PLQP0048KB-A (48P6Q-A) (48pins 7x7mm body LQFP)	

Application

W-CDMA base station, Digital PPC, Digital TV,VTR and so on.

Mode Descriptions

1K-word = 1024-words

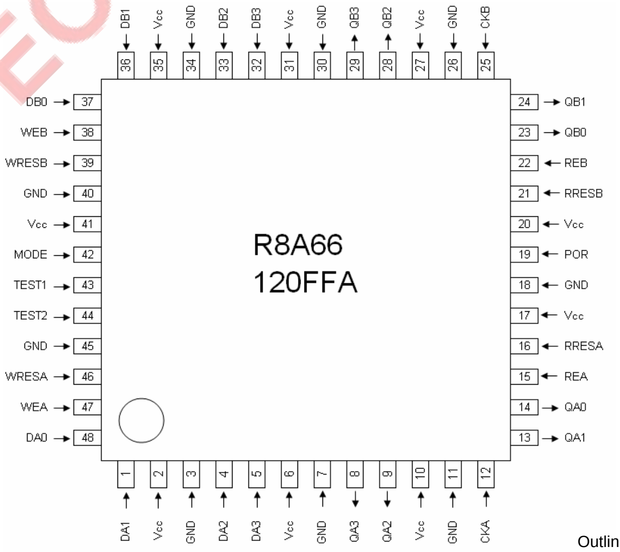


The 2 pieces of 1024K-word x 4-bit FIFO can be operated completely independently.

2-system individual input

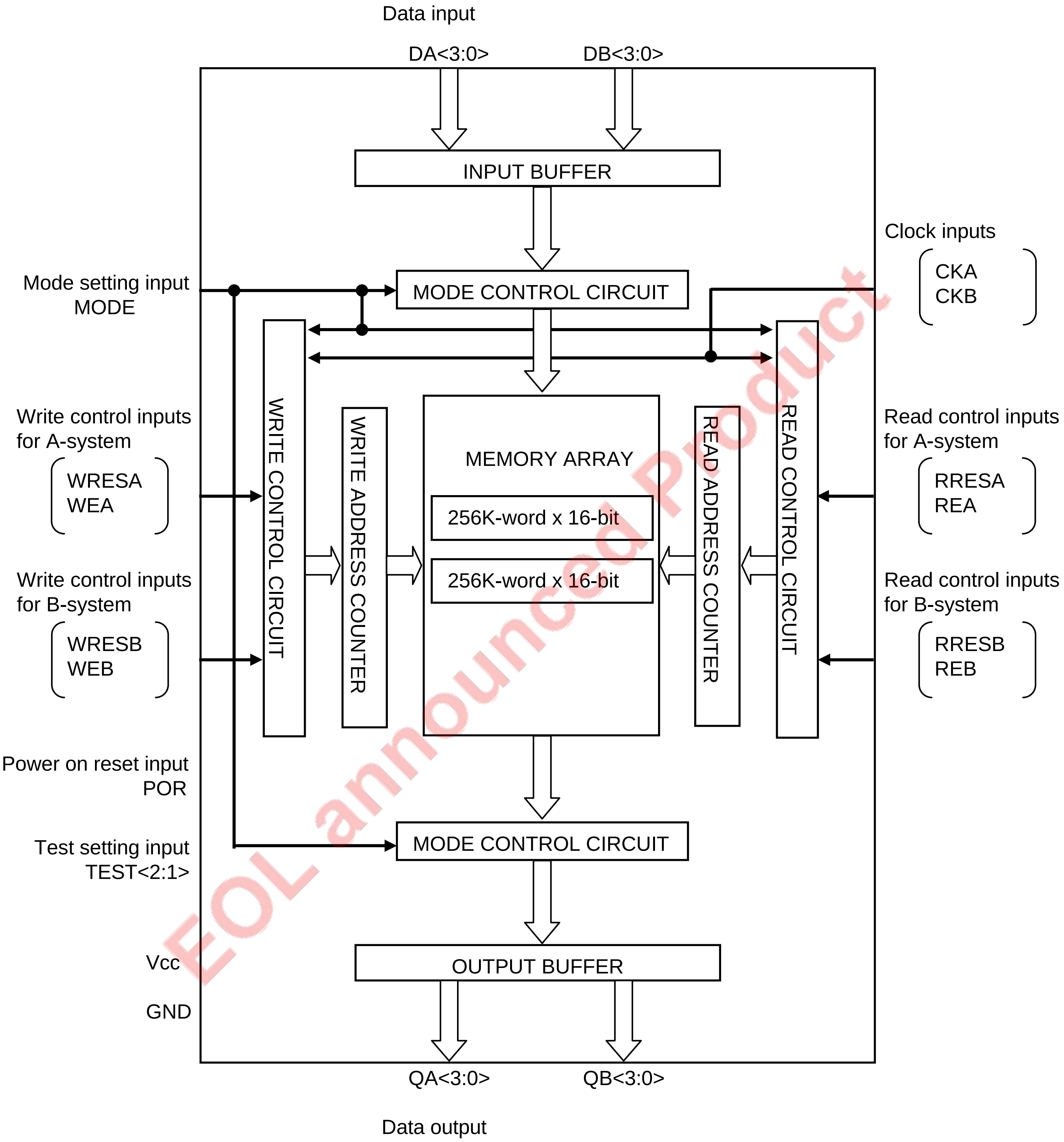
2-system individual output

Pin Configuration (Top view)



Outline: PLQP0048KB-A (48P6Q-A)

Block Diagram



Pin Function Description

Pin name **(*1)**	Name	Input/ Output	Number of pin(s)	Function
CKx	Clock input	Input	2	They are clock inputs.
WEx	Write enable input	Input	2	They are write enable control inputs. When they are "L", a write enable status is provided.
WRESx	Write reset input	Input	2	They are reset inputs to initialize a write address counter of internal FIFO. When they are "L", a write reset status is provided.
REx	Read enable input	Input	2	They are read enable control inputs. When they are "L", a read enable status is provided.
RRESx	Read reset input	Input	2	They are reset inputs to initialize a read address counter of internal FIFO. When they are "L", a read reset status is provided.
Dx<3:0>	Data input	Input	8	They are data input bus.
Qx<3:0>	Data output	Output	8	They are data output bus.
MODE	Mode setting input	Input	1	This is a pin for setting operation mode. MODE should be fixed at "L".
TEST<2:1>	Test setting input	Input	2	They are pins for test. TEST<2:1> should be fixed at "L".
POR	Power on reset input	Input	1	This is a power on reset input.
Vcc	Power supply pin	-	9	They are 3.3 V power supply pins.
GND	Ground pin	-	9	They are ground pins.

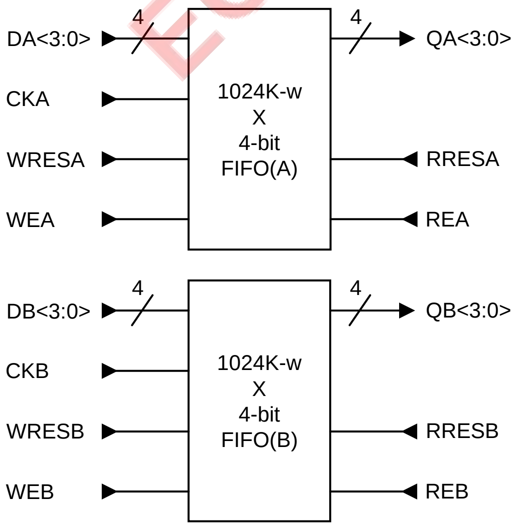
*Note1: X of the pin name shows A or B. A = A-system, B = B-system.

Mode pin Setting

In normal operation mode. It should be fixed on "L".

Pin Name	Operation MODE
MODE	
L	Normal operation
H	Out of a guarantee

Operation Description



R8A66120FFA can be controlled two pieces of 1024K-word x 4-bit FIFO completely independently. Taking FIFO (A) as an example, the operation of FIFO memory is described as follows.
The operation of FIFO (B) is the same as that of FIFO (A).

When write enable input WEA is "L", the contents of data input DA<3:0> are written into FIFO (A) in synchronization with the rising of clock input CKA.
At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", this IC disable to write data into FIFO (A) and the write address counter of FIFO (A) is not incremented.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) are outputted to data output QA<3:0> in synchronization with the rising of clock input CKA.
At this time, the read address counter of FIFO (A) is incremented.
When REA is "H", this IC disable to read data from FIFO (A) and the read address counter of FIFO (A) is not incremented.
Also QA<3:0> become high impedance state.
When read reset input RRESA is "L", the read address counter of FIFO (A) is initialized.

Electrical Characteristics

Absolute Maximum Ratings (Ta = 0 ~ 70ºC, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	A value based on GND	-0.3 ~ +3.8	V
V_I	Input voltage		-0.3 ~ Vcc+0.3	V
V_O	Output voltage		-0.3 ~ Vcc+0.3	V
Pd	Maximum power dissipation	Ta = 70°C	550	mW
Tstg	Storage temperature		-55 ~ +150	°C

Recommended Operating Conditions

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage	A value based on GND	3.0	3.3	3.6	V
V_I	Input voltage		0		Vcc	V
V_O	Output voltage		0		Vcc	V
T_{opr}	Operating ambient temperature		0		70	°C

DC Characteristics (Ta = 0 ~ 70ºC, Vcc = 3.3±0.3V, GND = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	A value based on GND	0.8×Vcc			V
V_{IL}	"L" input voltage				0.2 x Vcc	V
V_{OH}	"H" output voltage	I_{OH} = -4mA	Vcc−0.4			V
V_{OL}	"L" output voltage	I_{OL} = 4mA			0.4	V
I_{IH}	"H" input current	V_I = Vcc			10	uA
I_{IL}	"L" input current	V_I = GND			-10	uA
I_{OZH}	Off state "H" output current	V_O = Vcc			10	uA
I_{OZL}	Off state "L" output current	V_O = GND			-10	uA
Icc	Operating mean current dissipation	Vcc = 3.3 ± 0.3 V V_I : Repeat "H" and "L" V_O : Output open tCK = 10.0ns (f = 100MHz)			150	mA
C_I	Input capacitance	f = 1MHz			10	pF
C_O	Off state output capacitance	f = 1MHz			15	pF

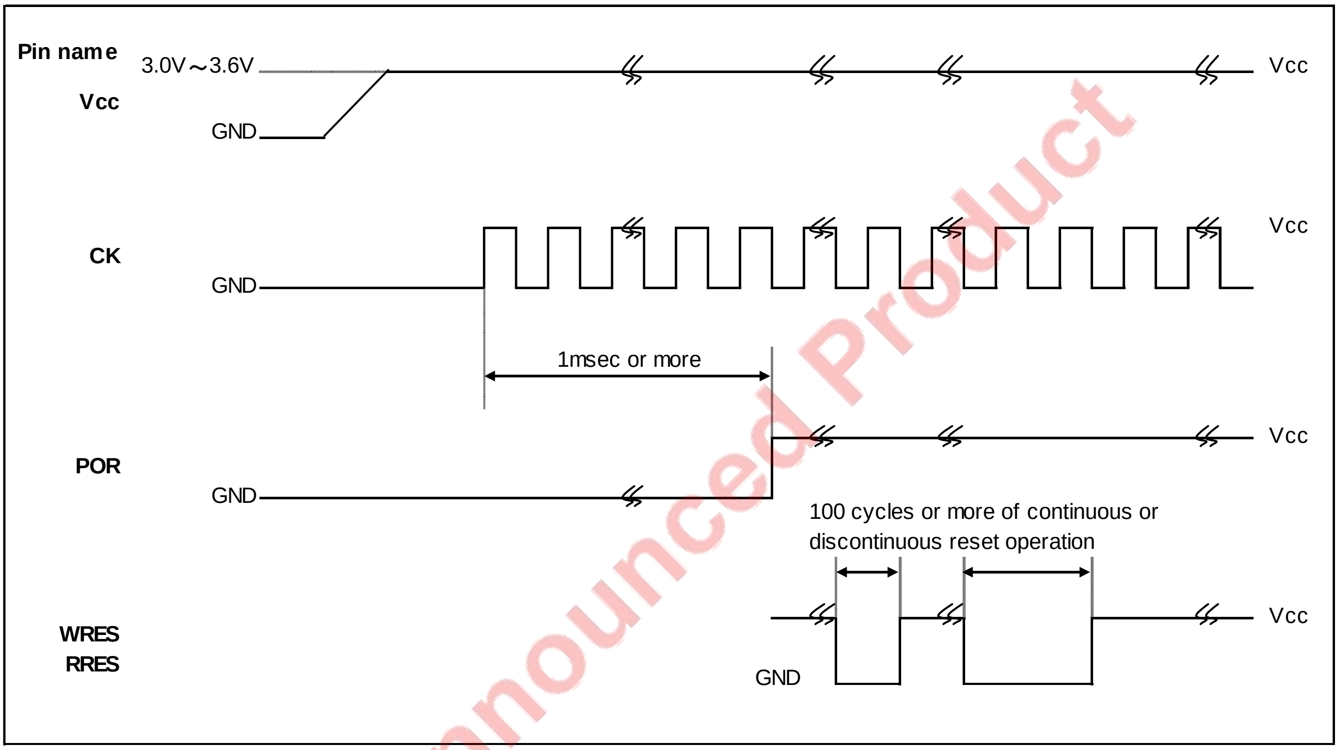
Power On

After power-on this IC, some circuits of internal FIFO should be initialized by the following procedures (1), (2).
Also, when the supply voltage (Vcc) drops below the operation voltage range(3.0 to 3.6V) during operating and so this is powered on again, they should be initialized by the same procedures.

(1)After 1msec or more has passed under the following conditions (i), (ii) and (iii), please input the signal of “L” to “H” to POR pin for power on reset. After of that, POR pin should be fixed at "H".

(i) :Vcc reaches to the operation voltage range.
(ii) :The clock signal is inputted to CK pin
(iii) :POR pin is fixed at "L".

(2)After POR pin is fixed at “H”, write reset and read reset operations should be provided with 100 cycles or more respectively. There is no problem in these reset operations, if total reset cycles reach to 100 or more even if those are discontinuous.



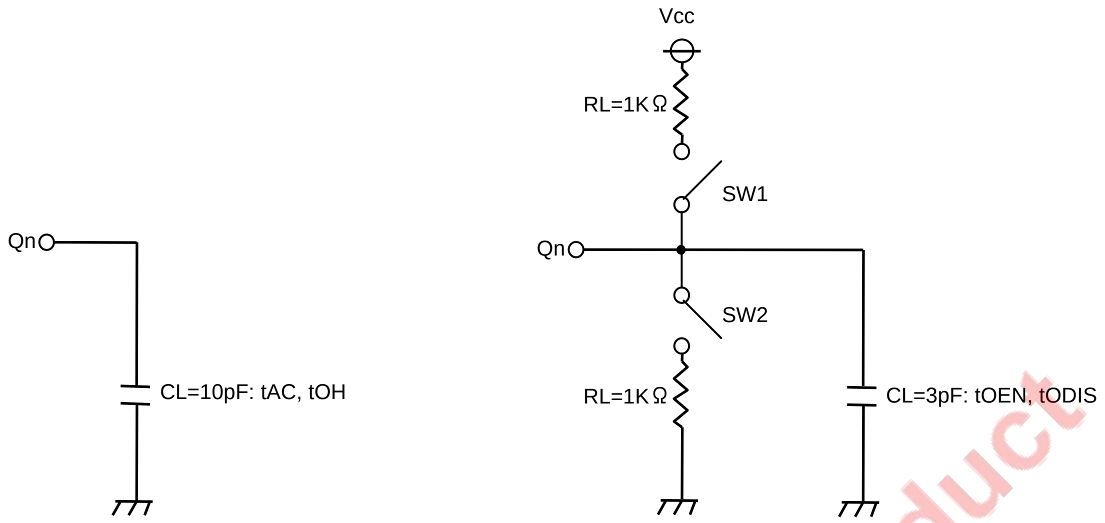
Timing Requirements (Ta = 0 ~ 70°C,Vcc = 3.3 ± 0.3V, GND = 0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tCK	Clock (CK) cycle	10		200	ns
tCKH	CK "H" pulse width	4			
tCKL	CK "L" pulse width	4			
tDS	Input data setup time to CK	4			
tDH	Input data hold time to CK	0			
tWRESS	Write reset setup time to CK	4			
tWRESH	Write reset hold time to CK	0			
tRRESS	Read reset setup time to CK	4			
tRRESH	Read reset hold time to CK	0			
tWES	Write enable setup time to CK	4			
tWEH	Write enable hold time to CK	0			
tRES	Read enable setup time to CK	4			
tREH	Read enable hold time to CK	0			
tr, tf	Input pulse rise / fall time			3	

Switching Characteristics (Ta = 0 ~ 70°C, Vcc = 3.3 ± 0.3V, GND = 0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tAC	Output access time to CK			6	ns
tOH	Output hold time to CK	1			
tOEN	Output enable time to CK	1		6	
tODIS	Output disable time to CK	1		6	

Switching Characteristics Measurement Circuit

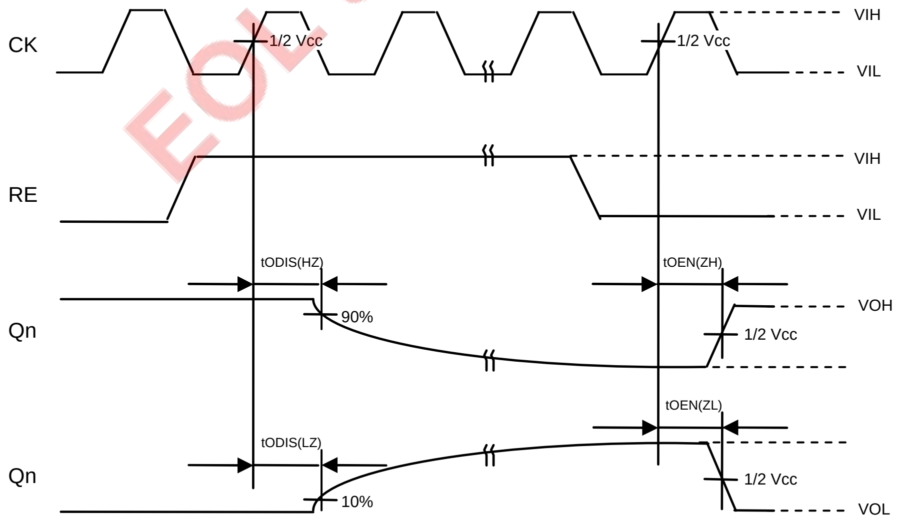


Parameter	SW1	SW2
tODIS(LZ)	Close	Open
tODIS(HZ)	Open	Close
tOEN(ZL)	Close	Open
tOEN(ZH)	Open	Close

Input pulse level	: 0 ~ Vcc
Input pulse rise/fall time	: 1 ns
Decision voltage input	: 1/2 Vcc
Decision voltage output	: 1/2 Vcc (However, tODIS(HZ) is judged with 90% of the output amplitude, while tODIS(LZ) is judged with 10% of the output amplitude.)

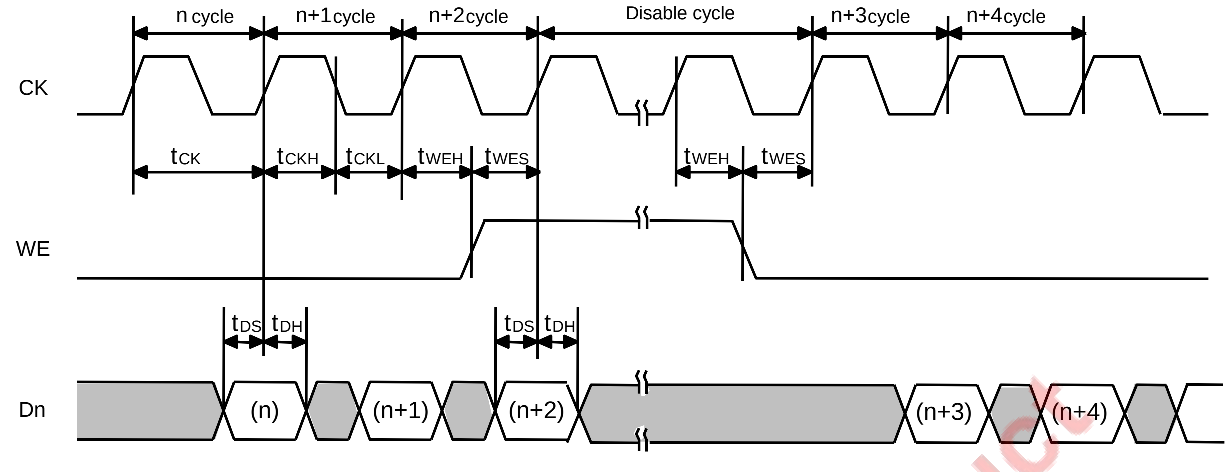
The load capacitance CL includes the floating capacitance of connections and a input capacitance of a probe.

tODIS and tOEN Measurement Conditions



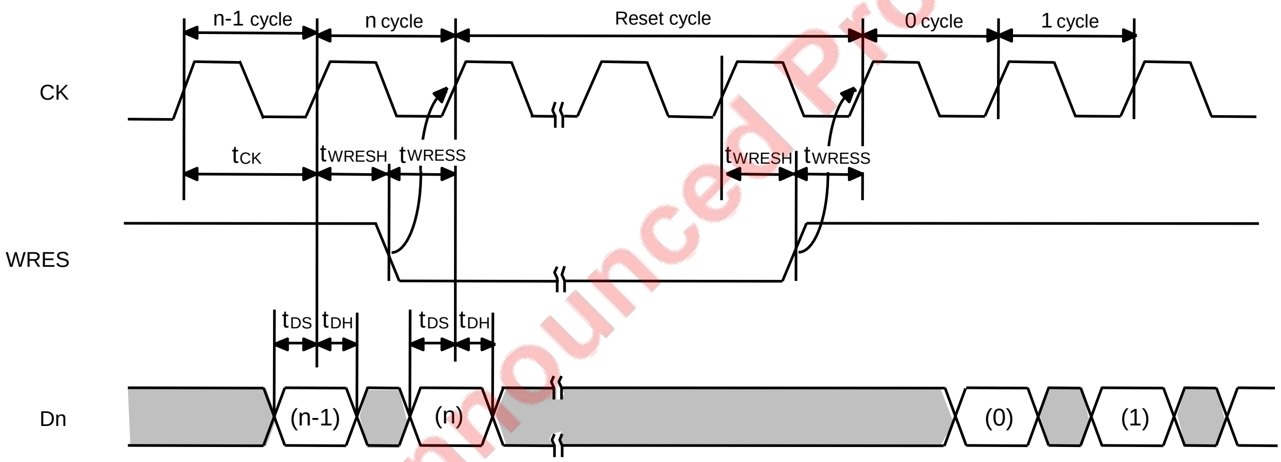
Operating Timing

Write Cycle



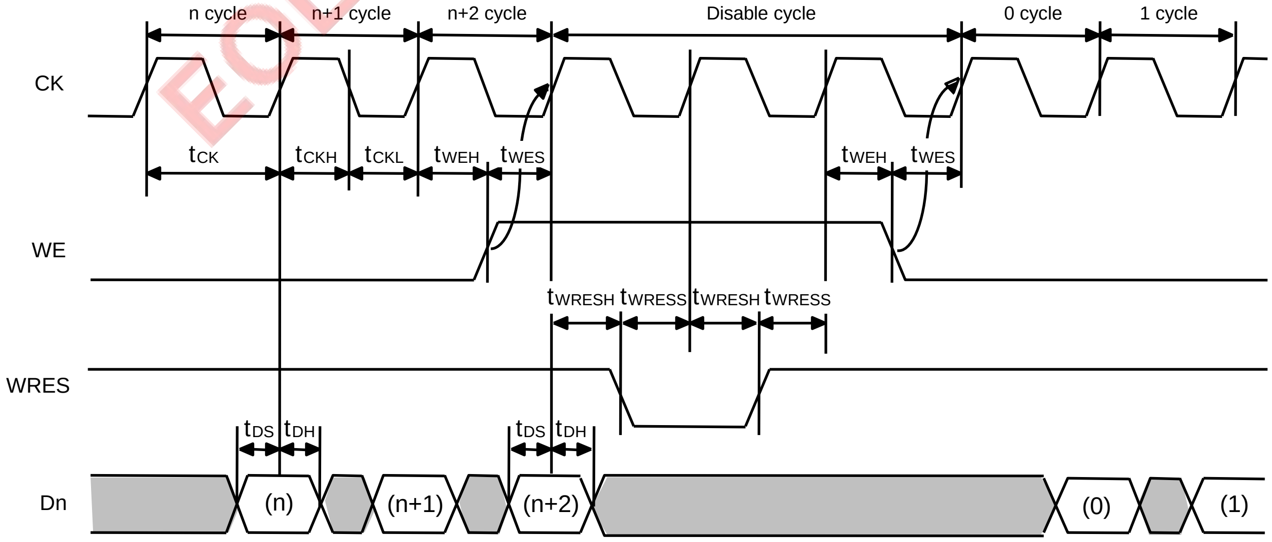
In case of WRES = “H”

Write Reset Cycle



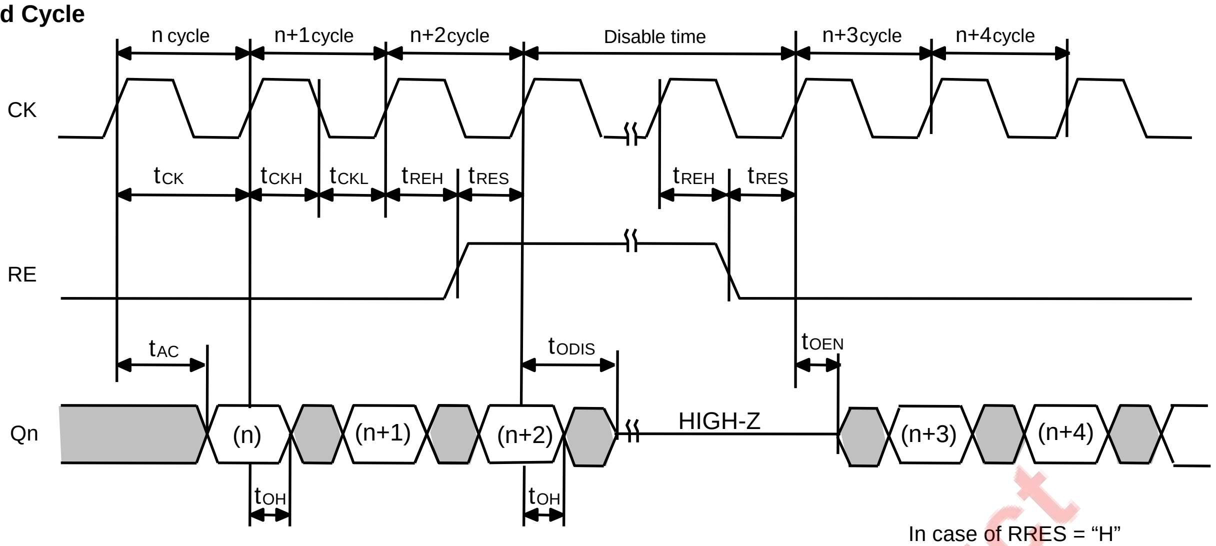
In case of WE = “L”

Write Reset and Write Enable Combination Cycle



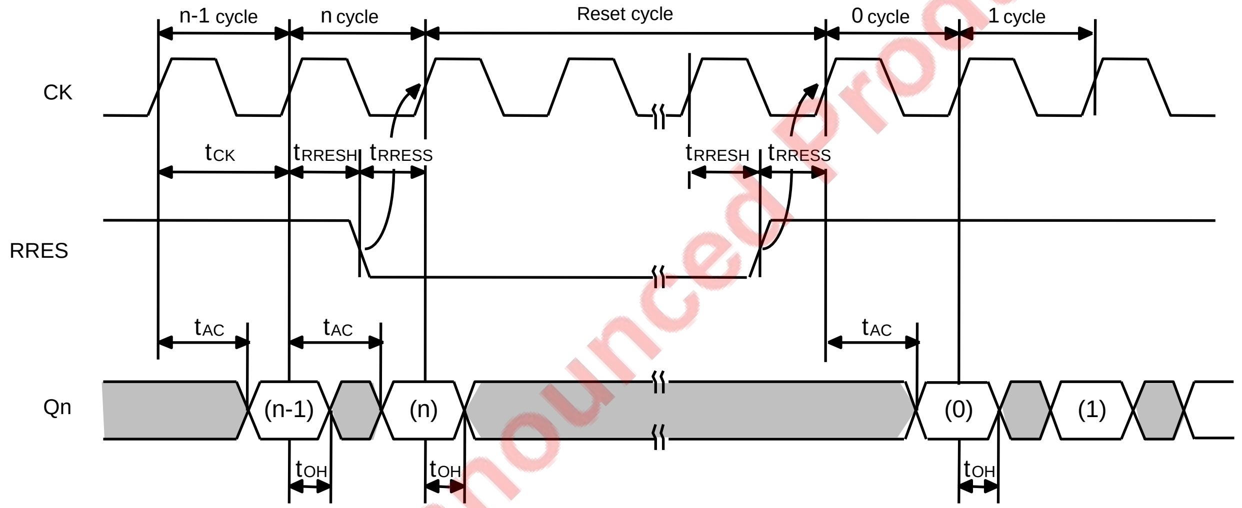
Note: There is no timing restriction of WE to WRES.

Read Cycle



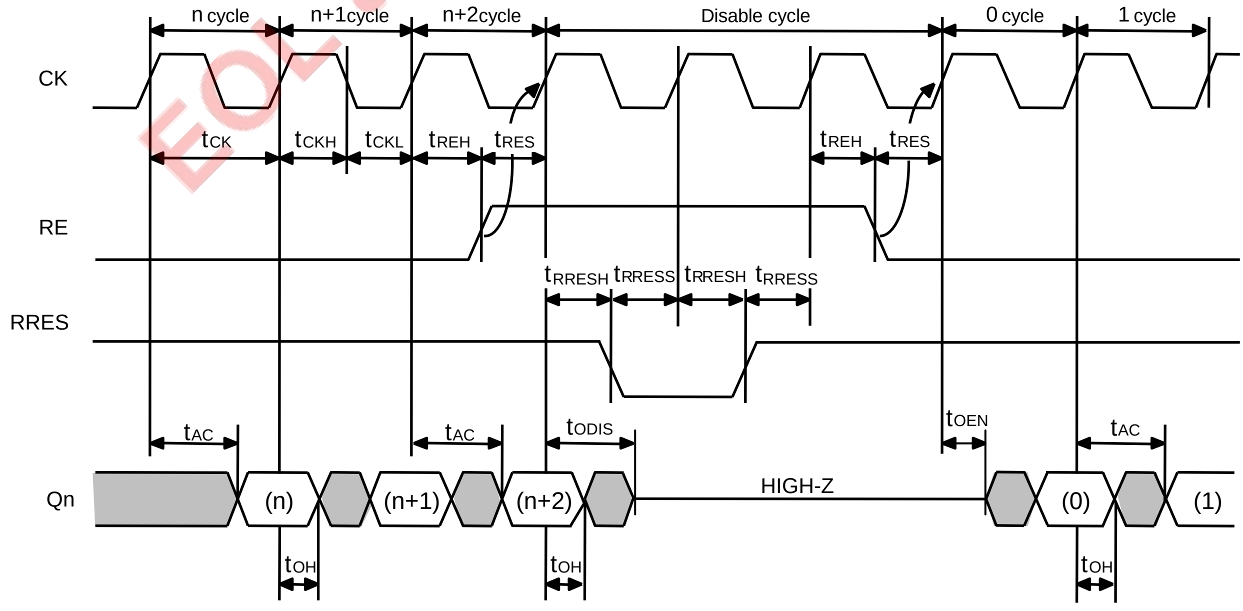
In case of RRES = “H”

Read Reset Cycle



In case of RE = “L”

Read Reset and Read Enable Combination Cycle



Note: There is no timing restriction of RE to RRES.

Caution When Write Cycle and Read Cycle Approach Each Other

The interval m between write cycle and a read cycle should be secured more than 256 cycles when the write cycle goes ahead of the read cycle on the following conditions, that is to say the interval less than 255 cycles is forbidden.

WRES, RRES="H"; WE, RE="L", and

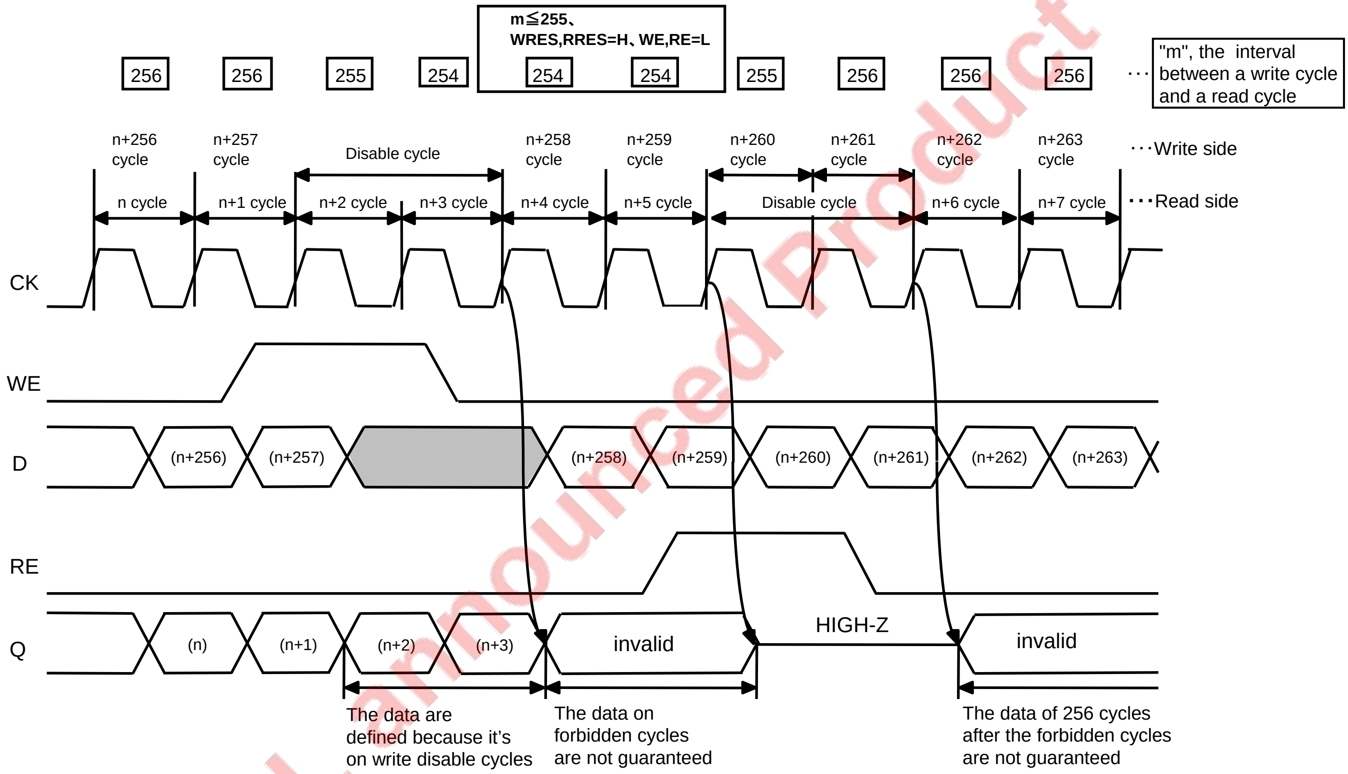
- Both write side and read side are activated continuously.

When once this restriction to the interval isn't fulfilled, writing data is guaranteed, but reading data isn't guaranteed not only for the cycles when it isn't fulfilled but also for the following 256 cycles after it is fulfilled again.
In this 256 cycles, read disable and read reset cycles are not counted.

But the following condition is an exception to the restriction to forbid the intervals less than 255 cycles.

- Either write side or read side is temporarily stopped owing to reset cycles (WRES or RRES="L") or disable cycles (WE or RE ="H").

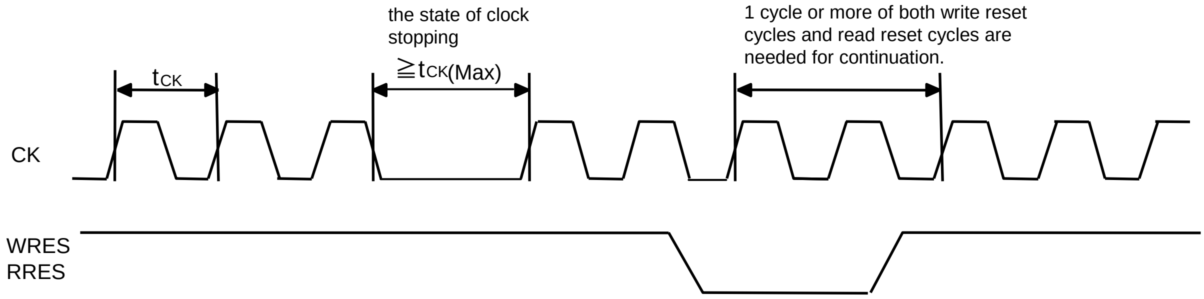
Note: Also, when the address counter is incremented up to the last cycle of 1-line and then returned to 0 cycle, the interval m between write and read cycles should be secured more than 256 cycles taking account that they are cyclic and serial lines.



In the case of read cycle goes ahead of the write cycle or write cycle and read cycle are accorded. It's exceptions of the restriction on forbid the intervals less than 255 cycles.

Caution of The State of Clock Stopping

Stopping of clock signal of this IC is forbidden during operating of it. "Stopping of clock signal" mean that CK is fixed at "L" or "H" for more than tck(Max)(=200ns).
When this restriction to tck isn't fulfilled, all writing data before stopping of clock signal isn't defined.
Once the clock signal stopped, 1 cycle or more of both write reset cycles and read reset cycles should be secured to operate again.

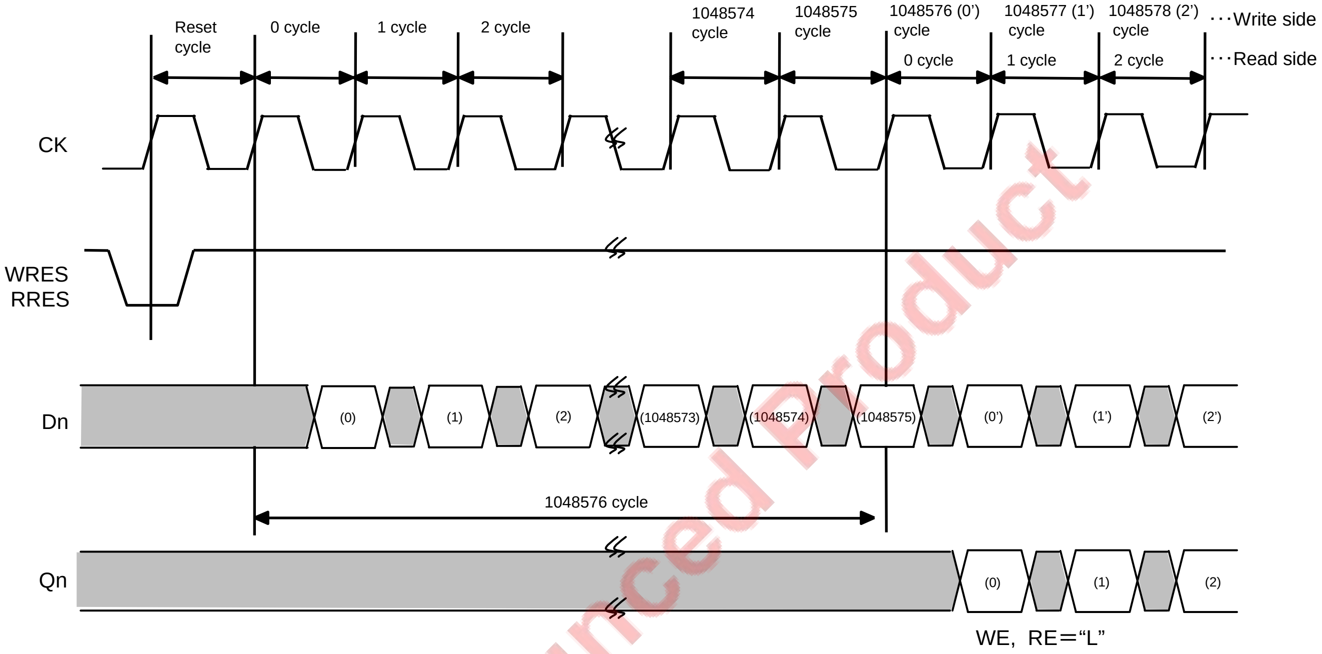


Variable Length Delay bits

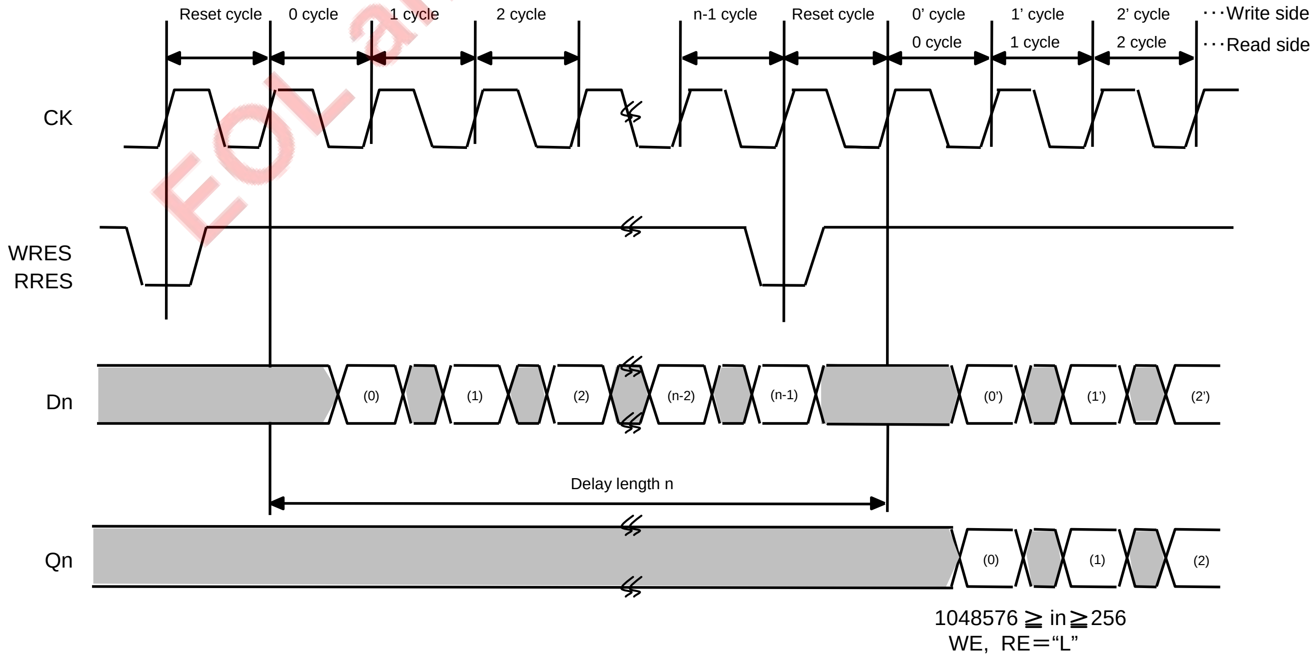
The 1-line length (cycle number) of R8A66120FFA is 1,048,576-cycle.

1-line Delay

In read cycles, an output data is read out at the (first) rising edge of CK (i.e. the start of the cycle) .
In write cycles, an input data is written at the (second) rising edge of CK (i.e. the end of the cycle) .
So 1-line delay can be made easily according to the control method of the following figure.

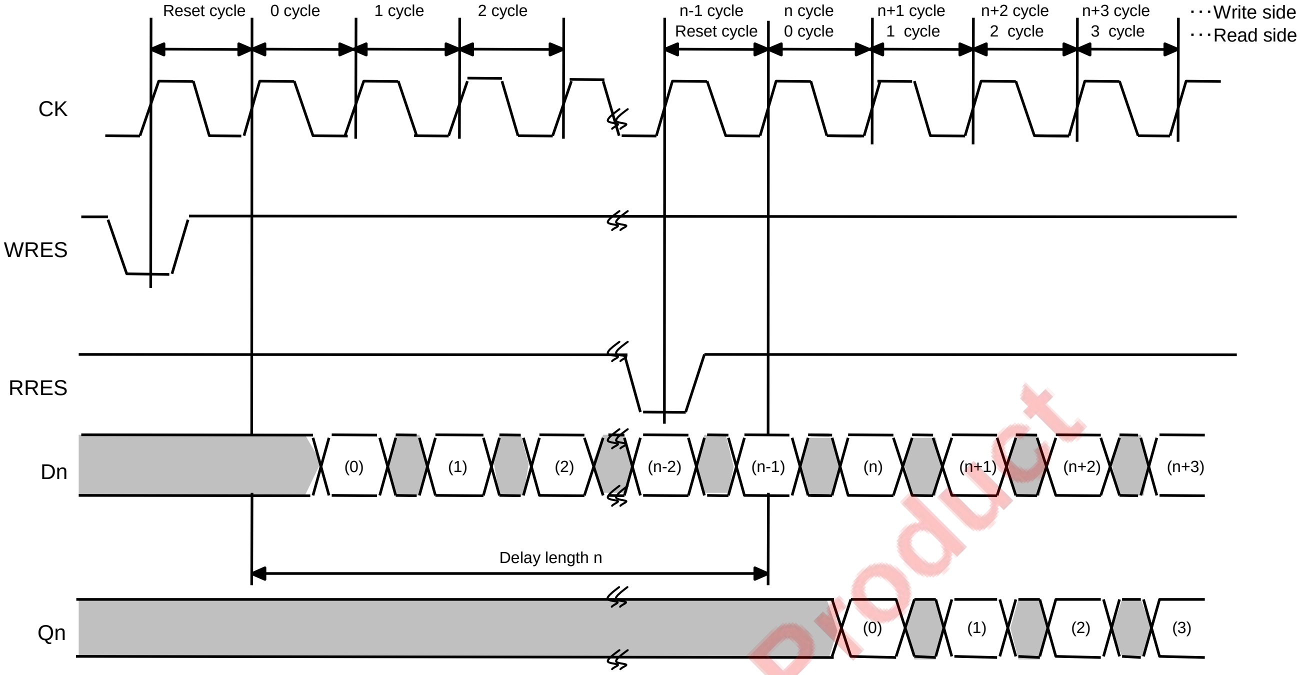


N-bit Delay 1
(Reset at cycles corresponding to delay length)



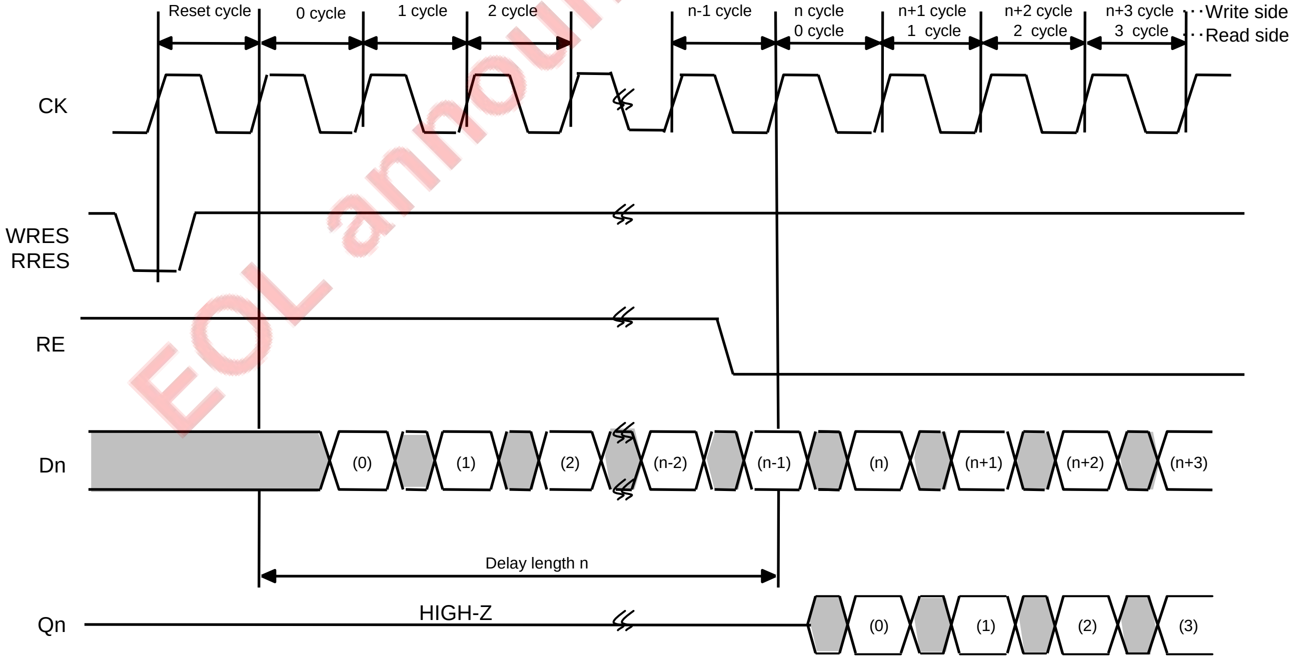
Note: Take care of the restriction to a interval between a write cycle and a read cycle (ref. page10).

N-bit Delay 2
(Sliding timings of WRES and RRES at cycles corresponding to delay length)



1048576 ≧n≧ 256
WE, RE=“L”

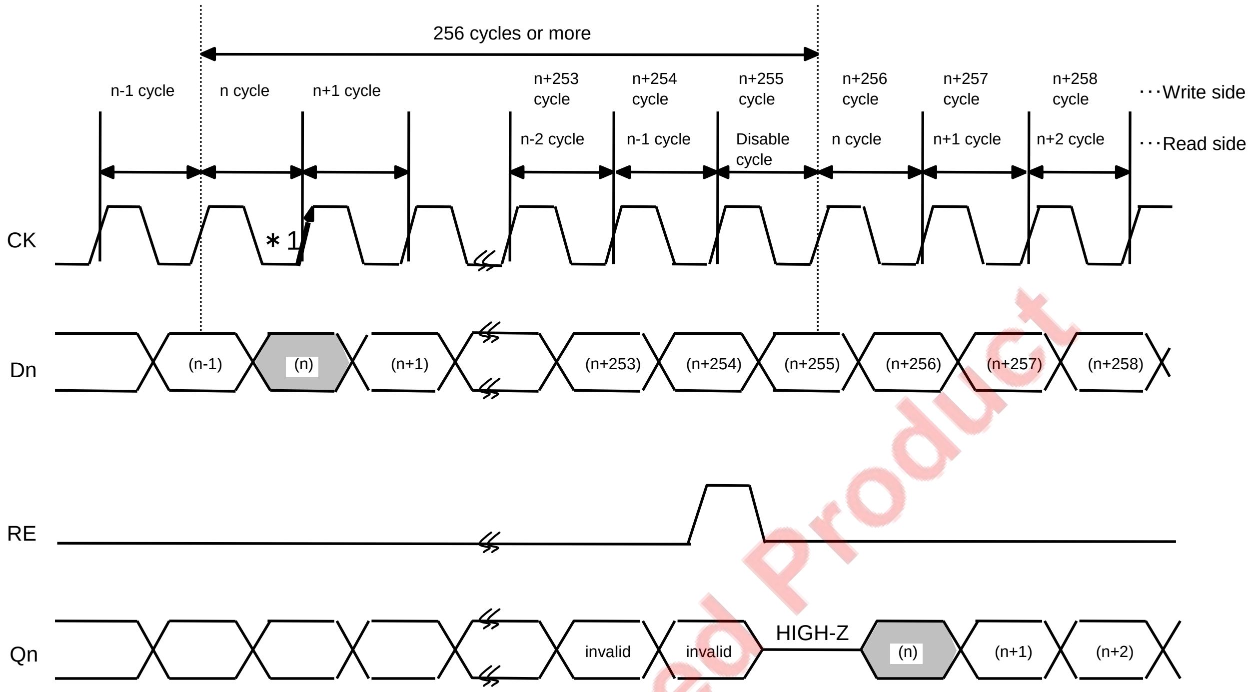
N-bit Delay 3
(Sliding address by disabling RE for cycles corresponding to delay length)



1048576 ≧n≧ 256
WE=“L”

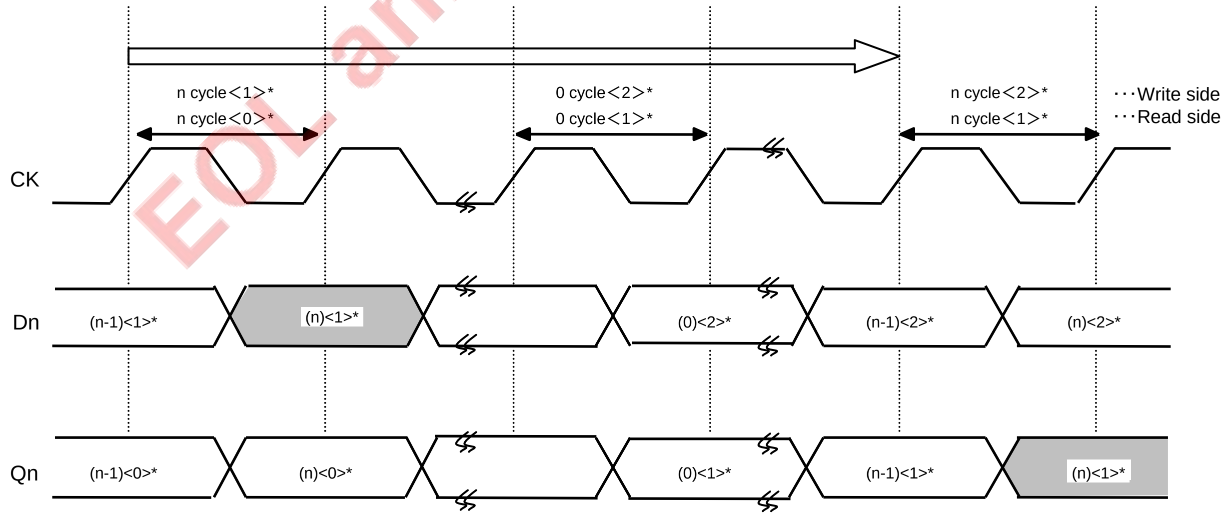
Reading shortest a data written at n cycle on write-side

In order to read out a written data, CK should be inputted for 256 cycles and more after the data is written.
In following figure, an example is shown of reading out the data written at the rising edge of CK (*1) at n cycle on write-side.
Output data becomes invalid when this restriction isn't fulfilled.
Also, take care of the restriction to the interval between a write cycle and a read cycle (ref. page10).



Reading longest a data written at n cycle on write-side : 1-line Delay

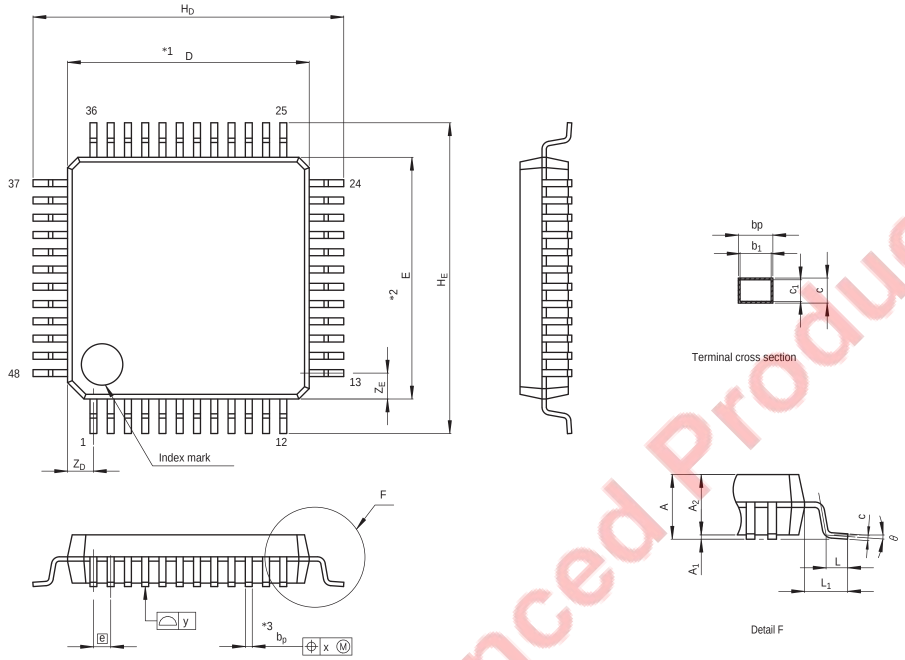
Output Q of n cycle<1>* can be read out until n cycle<1>* on read-side and n cycle<2>* on write-side overlap each other.



<0>* , <1>* and <2>* indicate a line number.

Package Outline

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

All trademarks and registered trademarks are the property of their respective owners.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2