

HAF2017(L), HAF2017(S)

Silicon N Channel Power MOS FET Power Switching

REJ03G0234-0200Z
(Previous ADE-208-1637 (Z))
Rev.2.00
Apr.13.2004

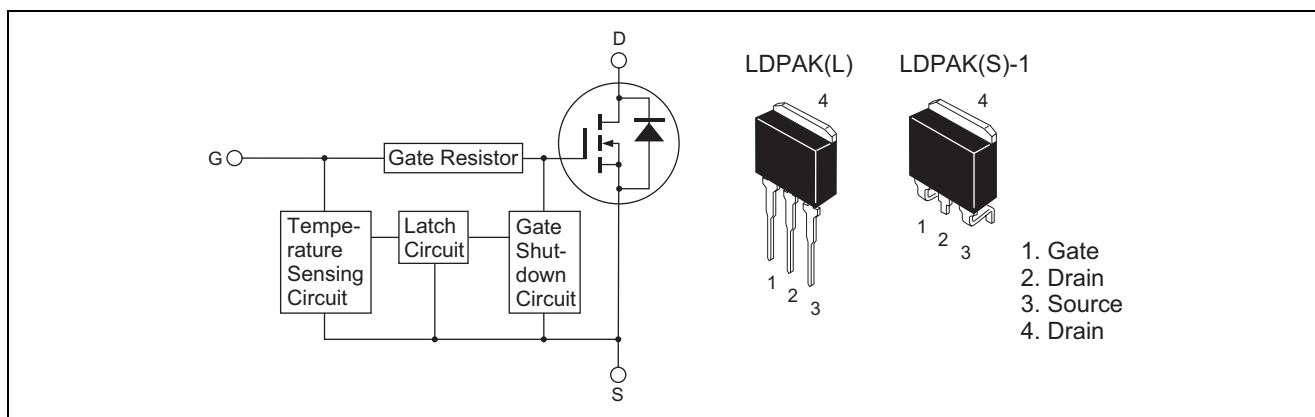
Descriptions

This FET has the over temperature shutdown capability sensing the junction temperature. This FET has the built-in over temperature shutdown circuit in the gate area. And this circuit operation to shutdown the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shutdown circuit
- Latch type shutdown operation (Need 0 voltage recovery)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	16	V
Gate to source voltage	V _{GSS}	-2.5	V
Drain current	I _D	20	A
Drain peak current	I _D (pulse) ^{Note1}	40	A
Body-drain diode reverse drain current	I _{DR}	20	A
Channel dissipation	P _{ch} ^{Note2}	50	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1%

2. Value at T_{ch} = 25°C

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	—	—	V	
Input voltage	V _{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	100	μA	V _i = 8V, V _{DS} = 0
Input current (Gate non shut down)	I _{IH2}	—	—	50	μA	V _i = 3.5V, V _{DS} = 0
Input current (Gate non shut down)	I _{IL}	—	—	1	μA	V _i = 1.2V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	0.8	—	mA	V _i = 8V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)2}	—	0.35	—	mA	V _i = 3.5V, V _{DS} = 0
Shutdown temperature	T _{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{OP}	3.5	—	12	V	

Electrical Characteristics

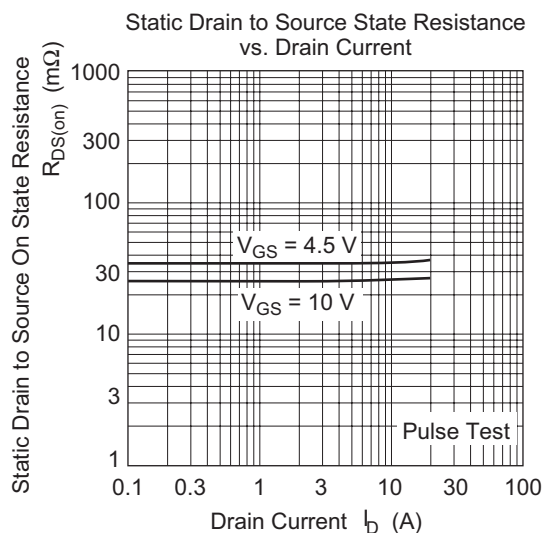
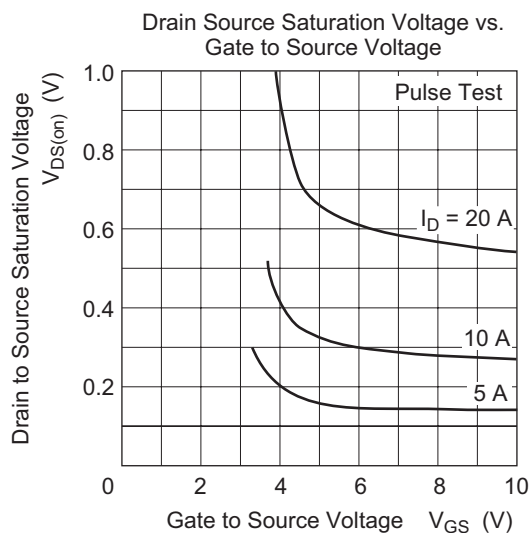
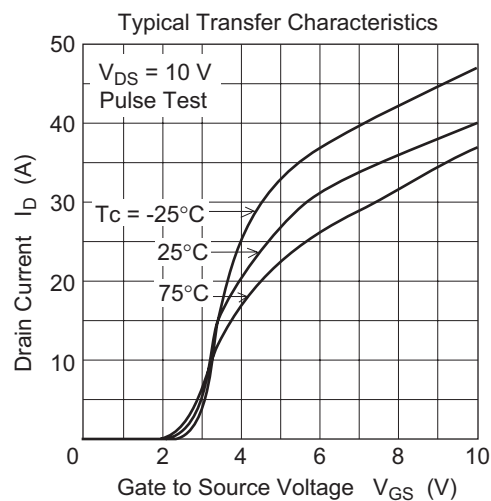
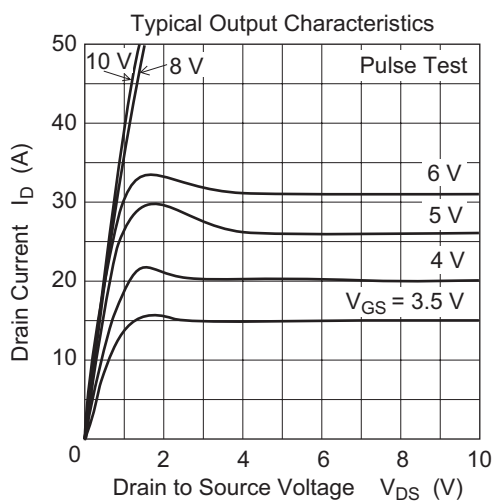
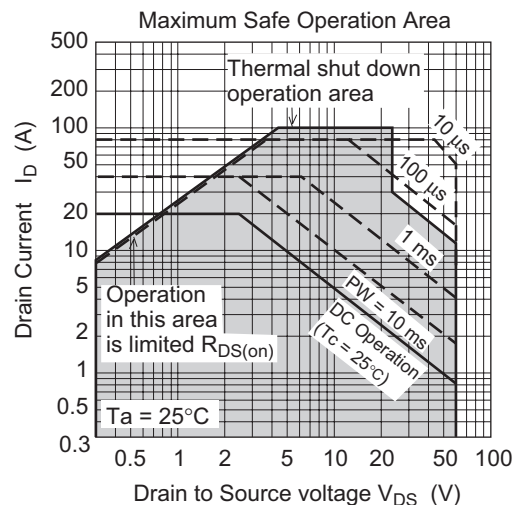
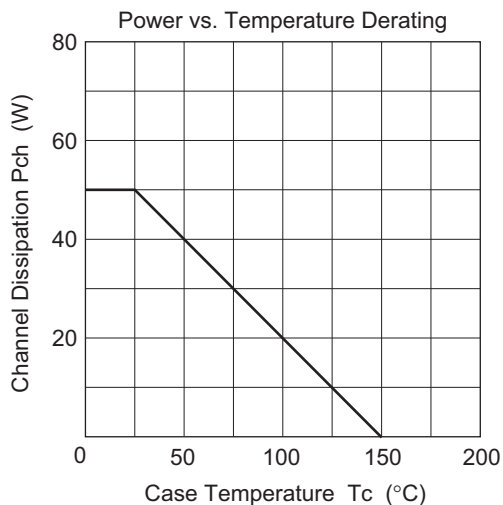
(Ta = 25°C)

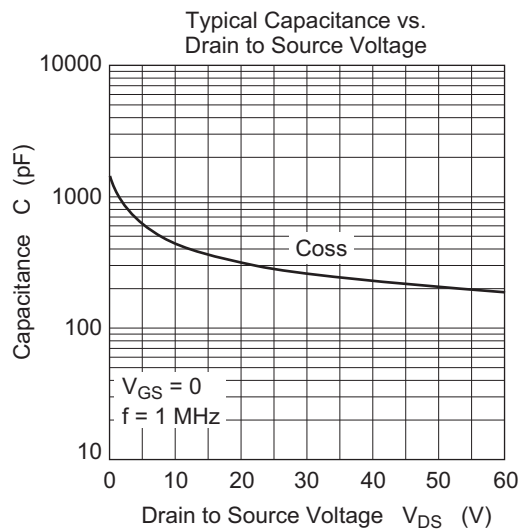
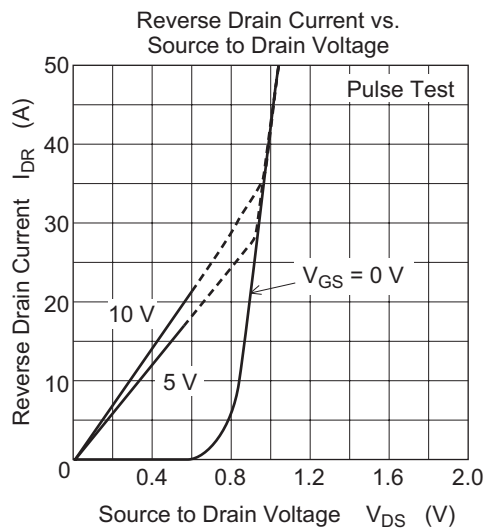
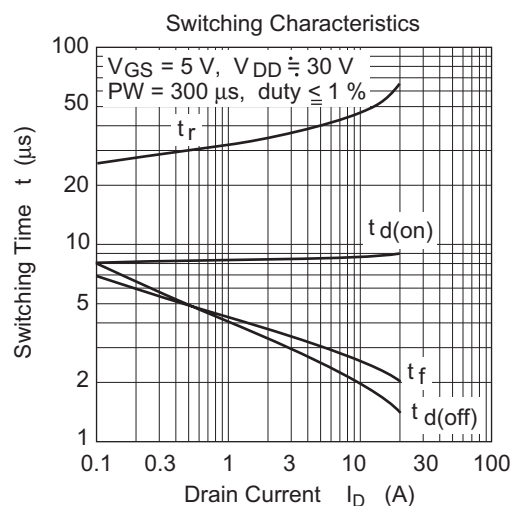
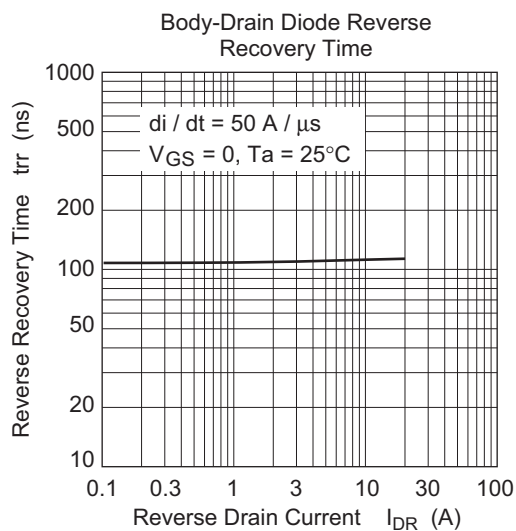
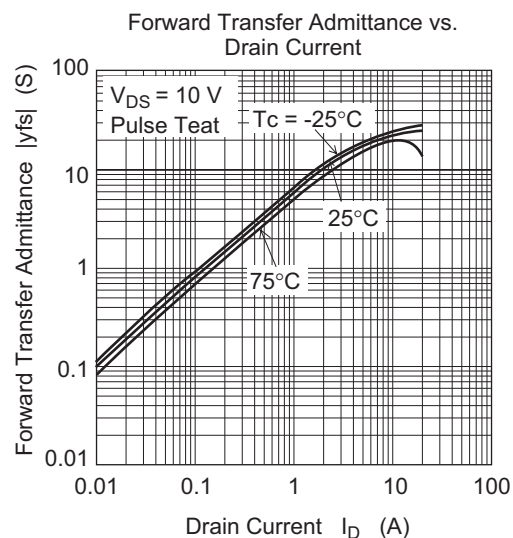
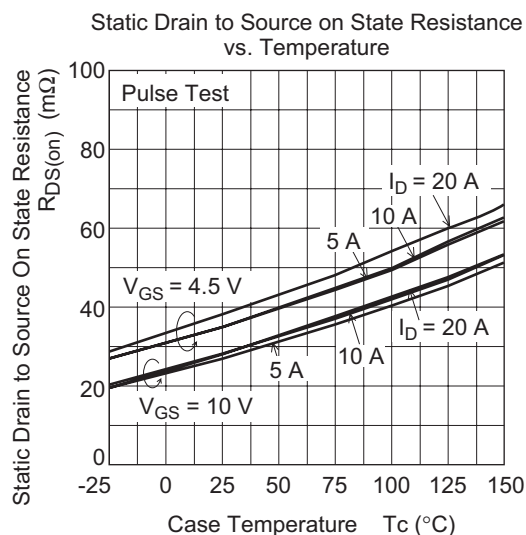
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Darin current	I_{D1}	1	—	—	A	$V_{GS} = 3.5 \text{ V}$, $V_{DS} = 2 \text{ V}$
Darin current	I_{D2}	—	—	10	mA	$V_{GS} = 1.2 \text{ V}$, $V_{DS} = 2 \text{ V}$
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	16	—	—	V	$I_G = 800 \mu\text{A}$, $V_{DS} = 0$
	$V_{(BR)GSS}$	-2.5	—	—	V	$I_G = -100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	100	μA	$V_{GS} = 8 \text{ V}$, $V_{DS} = 0$
	I_{GSS2}	—	—	50	μA	$V_{GS} = 3.5 \text{ V}$, $V_{DS} = 0$
	I_{GSS3}	—	—	1	μA	$V_{GS} = 1.2 \text{ V}$, $V_{DS} = 0$
	I_{GSS4}	—	—	-100	μA	$V_{GS} = -2.4 \text{ V}$, $V_{DS} = 0$
Input current (shut down)	$I_{GS(OP)1}$	—	0.8	—	mA	$V_{GS} = 8 \text{ V}$, $V_{DS} = 0$
	$I_{GS(OP)2}$	—	0.35	—	mA	$V_{GS} = 3.5 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.4	—	2.6	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	6	21	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Static drain to source on state resistance	$R_{DS(on)}$	—	35	53	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	27	43	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
Output capacitance	C_{oss}	—	460	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	8.7	—	μs	$V_{GS} = 5 \text{ V}$, $I_D = 10 \text{ A}$, $R_L = 3 \Omega$
Rise time	t_r	—	44.6	—	μs	
Turn-off delay time	$t_{d(off)}$	—	2	—	μs	
Fall time	t_f	—	2.6	—	μs	
Body-drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	120	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$, $diF/dt = 50 \text{ A}/\mu\text{s}$
Over load shut down operation time ^{Note4}	t_{os1}	—	0.97	—	ms	$V_{GS} = 5 \text{ V}$, $V_{DD} = 16 \text{ V}$
	t_{os2}	—	0.57	—	ms	$V_{GS} = 5 \text{ V}$, $V_{DD} = 24 \text{ V}$

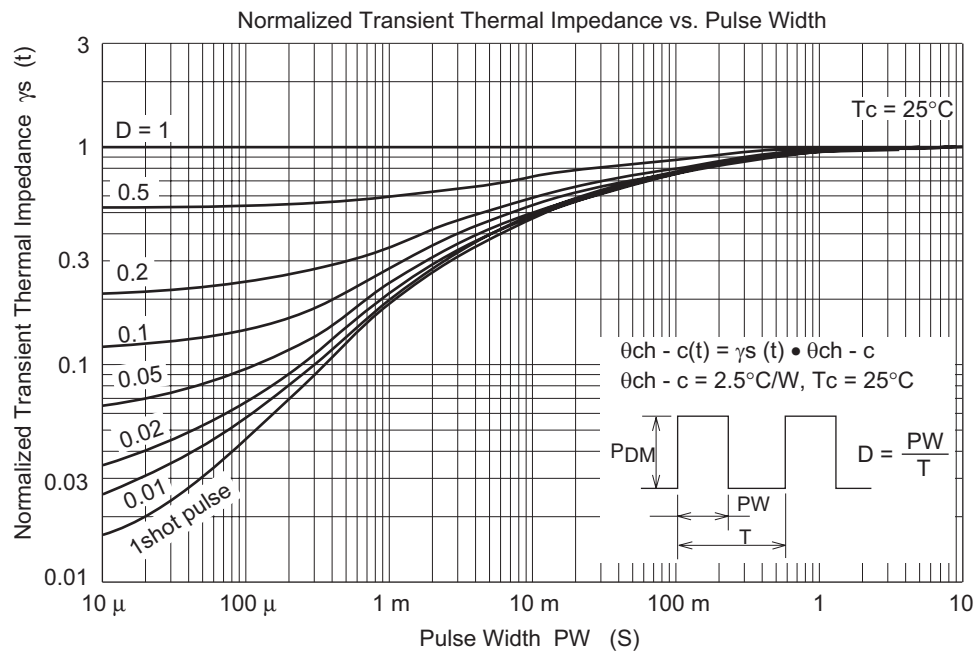
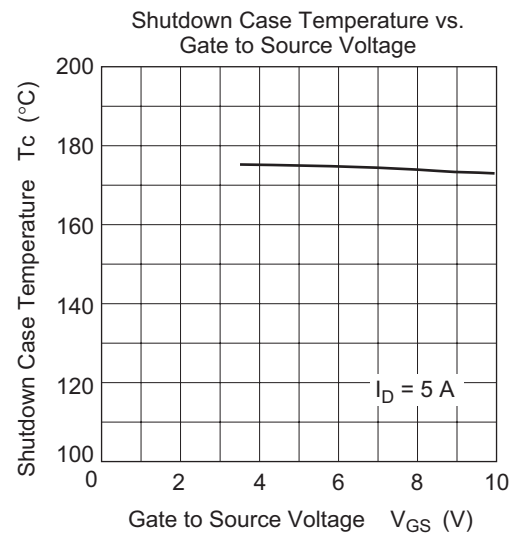
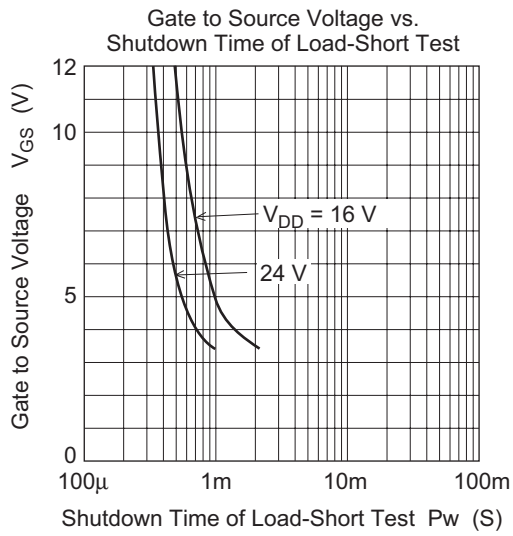
Notes: 3. Pulse test

4. Include the time shift based on increasing of channel temperature when operate under over load condition.

Main Characteristics

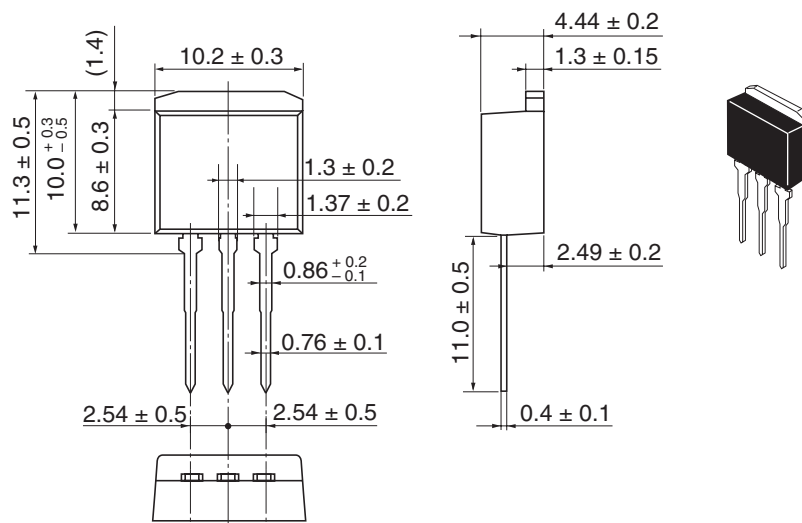






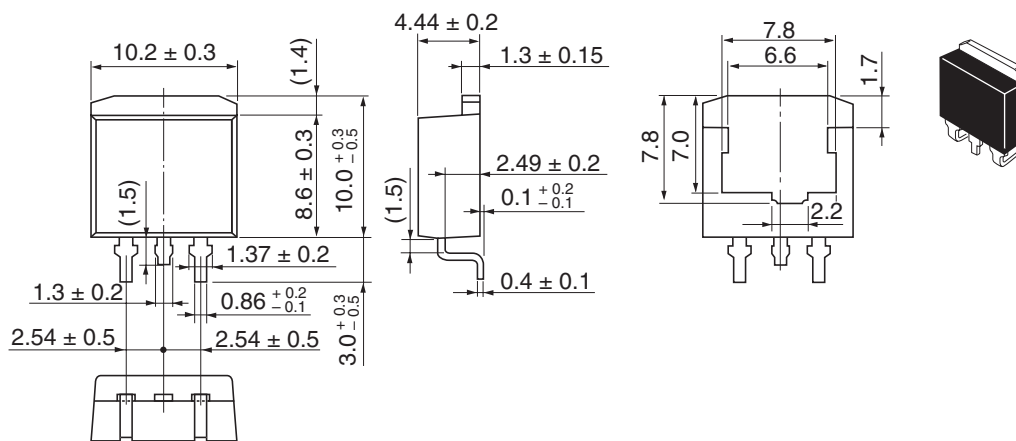
Package Dimensions

As of January, 2003
Unit: mm



Package Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.40 g

As of January, 2003
Unit: mm



Package Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.30 g

Ordering Information

Part Name	Quantity	Shipping Container
HAF2017-90L	Max: 50 pcs/ sack	Sack
HAF2017-90S	Max: 50 pcs/ sack	Sack
HAF2017-90STL	1000 pcs/ Reel	Embossed tape
HAF2017-90STR	1000 pcs/ Reel	Embossed tape

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