# HD74LS258

## Quadruple 2-line-to-1-line Data Selectors / Multiplexers (with three-state outputs)

REJ03D0470–0300
Rev.3.00
Jul.15.2005

This multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

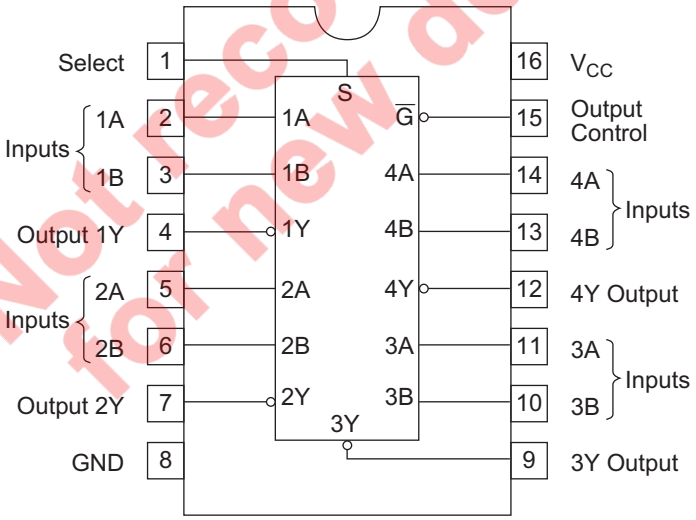
### Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74LS258FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |



### Pin Arrangement



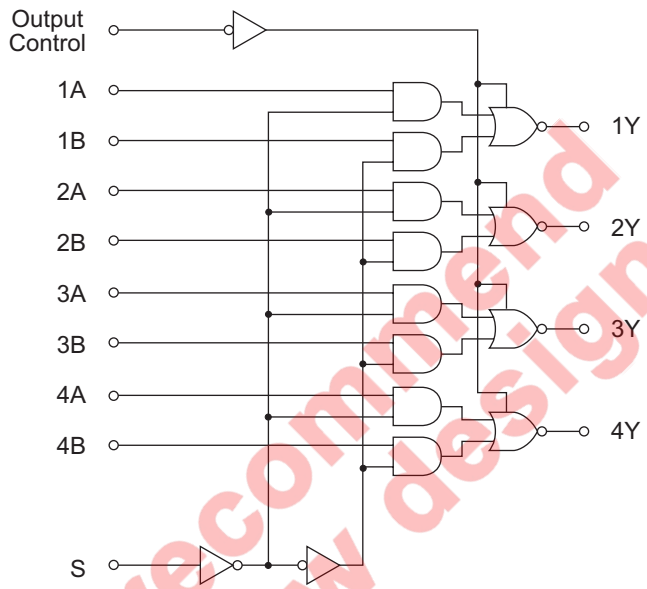

(Top view)

## Function Table

| Inputs | | | | Output |
|---|---|---|---|---|
| OC | S | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

Note: H; high level, L; low level, X; irrelevant, Z; off (high-impedance) state of a 3-state output

## Block Diagram






## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input voltage | $V_{IN}$ | 7 | V |
| Power dissipation | $P_T$ | 400 | mW |
| Storage temperature | Tstg | –65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | $I_{OH}$ | — | — | –2.6 | mA |
| | $I_{OL}$ | — | — | 8 | mA |
| Operating temperature | Topr | –20 | 25 | 75 | °C |

## Electrical Characteristics

(Ta = –20 to +75 °C)

| Item | | Symbol | min. | typ.* | max. | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Input voltage | | $V_{IH}$ | 2.0 | — | — | V | |
| | | $V_{IL}$ | — | — | 0.8 | V | |
| Output voltage | | $V_{OH}$ | 2.4 | — | — | V | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = –2.6 mA |
| | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 4 mA, $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V |
| | | | — | — | 0.5 | V | $I_{OL}$ = 8 mA |
| Output Current | | $I_{OZH}$ | — | — | 20 | µA | $V_{CC}$ = 5.25 V, $V_{IH}$ = 2 V, $V_O$ = 2.4 V |
| | | $I_{OZL}$ | — | — | –20 | µA | $V_{CC}$ = 5.25 V, $V_{IH}$ = 2 V, $V_O$ = 0.4 V |
| Input current | S | $I_{IH}$ | — | — | 40 | µA | $V_{CC}$ = 5.25 V, $V_I$ = 2.7 V |
| | except S | | — | — | 20 | µA | |
| | S | $I_{IL}$ | — | — | –0.8 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V |
| | except S | | — | — | –0.4 | mA | |
| | S | $I_I$ | — | — | 0.2 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 7 V |
| | except S | | — | — | 0.1 | mA | |
| Short-circuit output current | | $I_{OS}$ | –30 | — | –130 | mA | $V_{CC}$ = 5.25 V |
| Supply current** | All outputs high | $I_{CC}$ | — | — | 7 | mA | $V_{CC}$ = 5.25 V |
| | All outputs low | | — | — | 11 | mA | |
| | All outputs off | | — | — | 12 | mA | |
| Input clamp voltage | | $V_{IK}$ | — | — | –1.5 | V | $V_{CC}$ = 4.75 V, $I_{IN}$ = –18 mA |

Notes: * $V_{CC}$ = 5 V, Ta = 25°C

** $I_{CC}$ is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

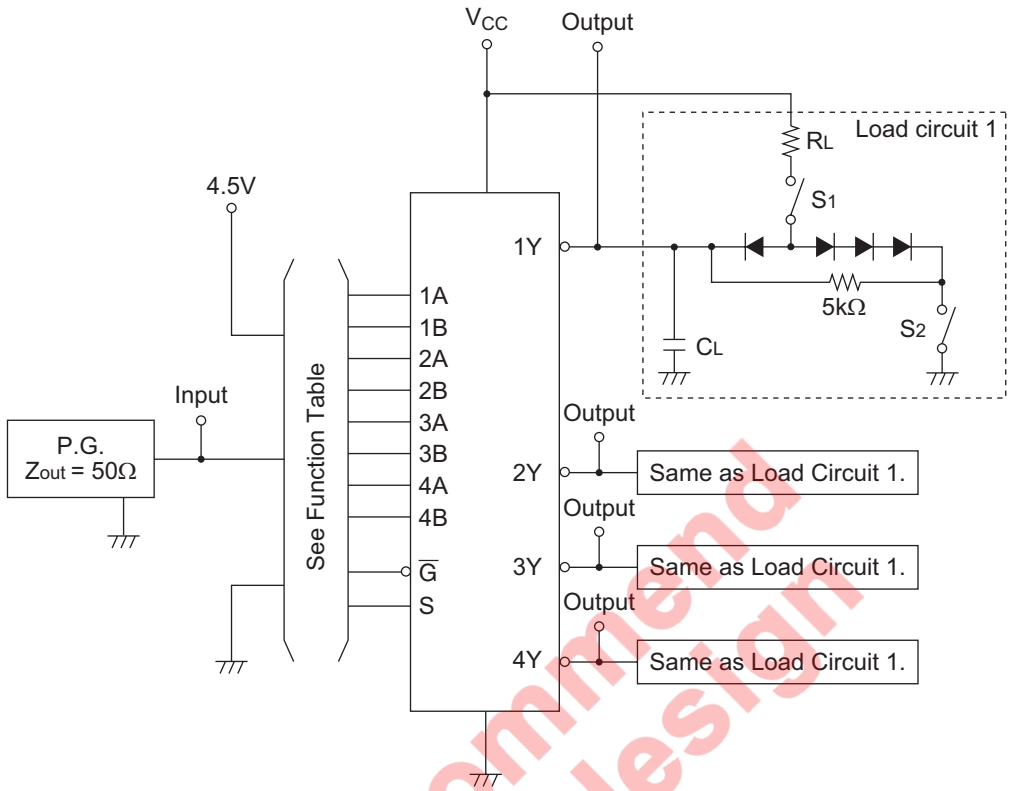
## Switching Characteristics

($V_{CC}$ = 5 V, Ta = 25°C)

| Item | Symbol | Inputs | Output | min. | typ. | max. | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | A, B | Y | — | 12 | 18 | ns | $C_L$ = 15 pF, $R_L$ = 2 kΩ |
| | $t_{PHL}$ | | | — | 12 | 18 | | |
| | $t_{PLH}$ | S | Y | — | 14 | 21 | ns | |
| | $t_{PHL}$ | | | — | 14 | 21 | | |
| Output enable time | $t_{ZH}$ | OC | Y | — | 20 | 30 | ns | |
| | $t_{ZL}$ | | | — | 20 | 30 | | |
| Output disable time | $t_{HZ}$ | OC | Y | — | 18 | 30 | ns | $C_L$ = 5 pF, $R_L$ = 2 kΩ |
| | $t_{LZ}$ | | | — | 16 | 25 | | |

## Testing Method

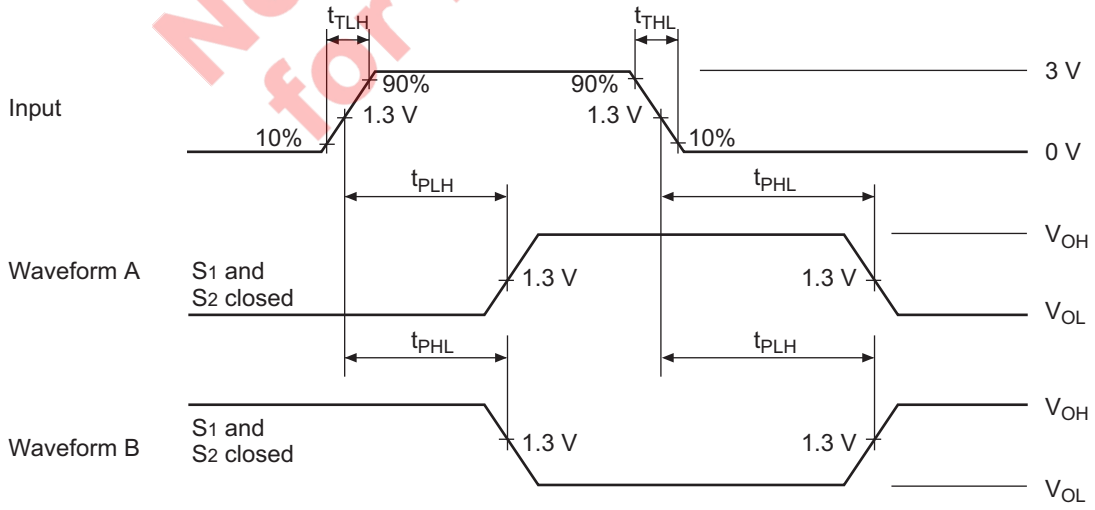
### Test Circuit




Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074(H).

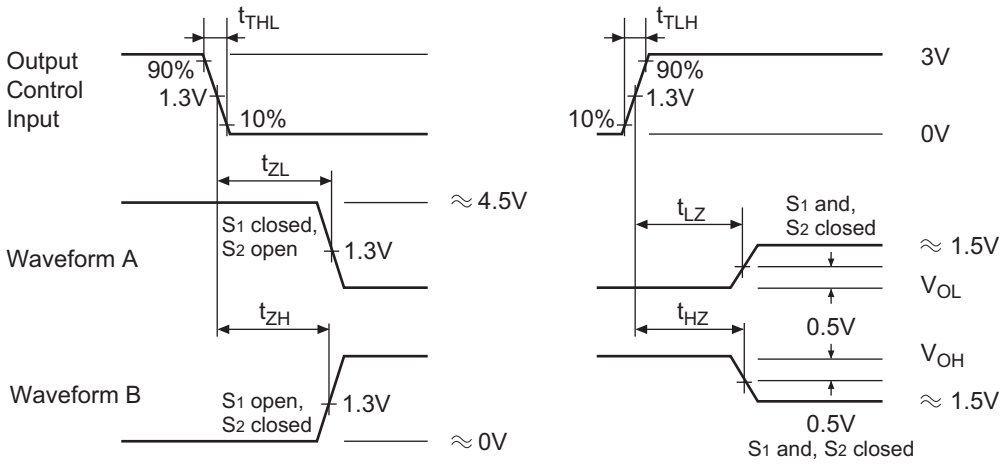


### Waveforms 1




Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%

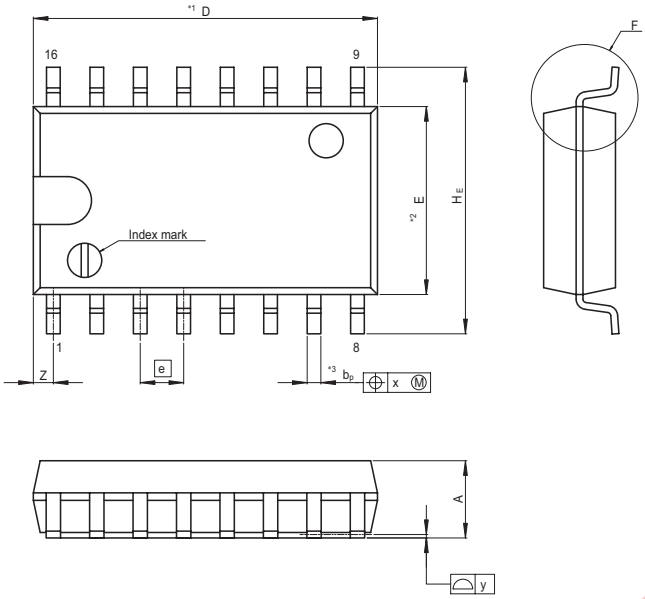
## Waveforms 2




Notes:
1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%
2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

## Package Dimensions

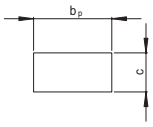
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-B | FP-16DAV | 0.24g |



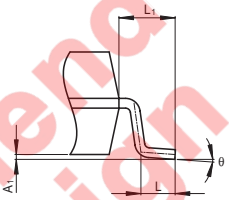




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.




Terminal cross section
( Ni/Pd/Au plating )




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.50 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| $L_1$ | — | 1.15 | — |

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