

HD74LV2G74A

Single D-type Flip Flops with Preset and Clear

REJ03D0097-0500
(Previous: ADE-205-346D)
Rev.5.00
Apr 07, 2006

Description

The HD74LV2G74A has independent data, preset, clear, and clock inputs Q and \bar{Q} outputs in an 8 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

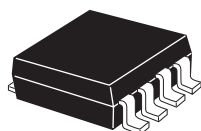
Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Electrical characteristics equivalent to the HD74LV74A
Supply voltage range : 1.65 to 5.5 V
Operating temperature range : -40 to +85°C
- All inputs V_{IH} (Max.) = 5.5 V (@ V_{CC} = 0 V to 5.5 V)
All outputs V_O (Max.) = 5.5 V (@ V_{CC} = 0 V)
- Output current ± 6 mA (@ V_{CC} = 3.0 V to 3.6 V), ± 12 mA (@ V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

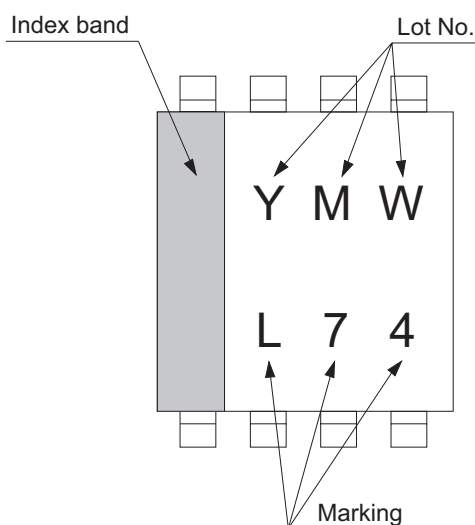
| Part Name | Package Type | Package Code (Previous code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|----------------|--------------|---------------------------------|-------------------------|-----------------------------------|
| HD74LV2G74AUSE | SSOP-8 pin | PVSP0008KA-A (TTP-8DBV) | US | E (3,000 pcs / Reel) |

Outline and Article Indication

• HD74LV2G74A



SSOP-8



Y : Year code
(the last digit of year)
M : Month code
W : Week code

Function Table

| Inputs | | | | Outputs | |
|-------------------------|-------------------------|--------------|---|-----------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H^{*1} | H^{*1} |
| H | H | \uparrow | H | H | L |
| H | H | \uparrow | L | L | H |
| H | H | \downarrow | X | Q_0 | $\overline{\text{Q}}_0$ |

H : High level

L : Low level

X : Immaterial

\uparrow : Low to high transition

\downarrow : High to low transition

Q_0 : The level of Q immediately before the input conditions shown in the above table are determined.

Note : 1. Q and $\overline{\text{Q}}$ will remain high as long as preset and clear are low, but Q and $\overline{\text{Q}}$ are unpredictable, if preset and clear go high simultaneously.

Pin Arrangement



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Test Conditions |
|---------------------------------------------------------------------------------------|-----------------------|------------------------|------------------|-----------------------------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V | |
| Input voltage range ^{*1} | V_I | -0.5 to 7.0 | V | |
| Output voltage range ^{*1, 2} | V_O | -0.5 to $V_{CC} + 0.5$ | V | Output : H or L |
| | | -0.5 to 7.0 | | V_{CC} : OFF |
| Input clamp current | I_{IK} | -20 | mA | $V_I < 0$ |
| Output clamp current | I_{OK} | ± 50 | mA | $V_O < 0$ or $V_O > V_{CC}$ |
| Continuous output current | I_O | ± 25 | mA | $V_O = 0$ to V_{CC} |
| Continuous current through V_{CC} or GND | I_{CC} or I_{GND} | ± 50 | mA | |
| Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3} | P_T | 200 | mW | |
| Storage temperature | T_{stg} | -65 to 150 | $^\circ\text{C}$ | |

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

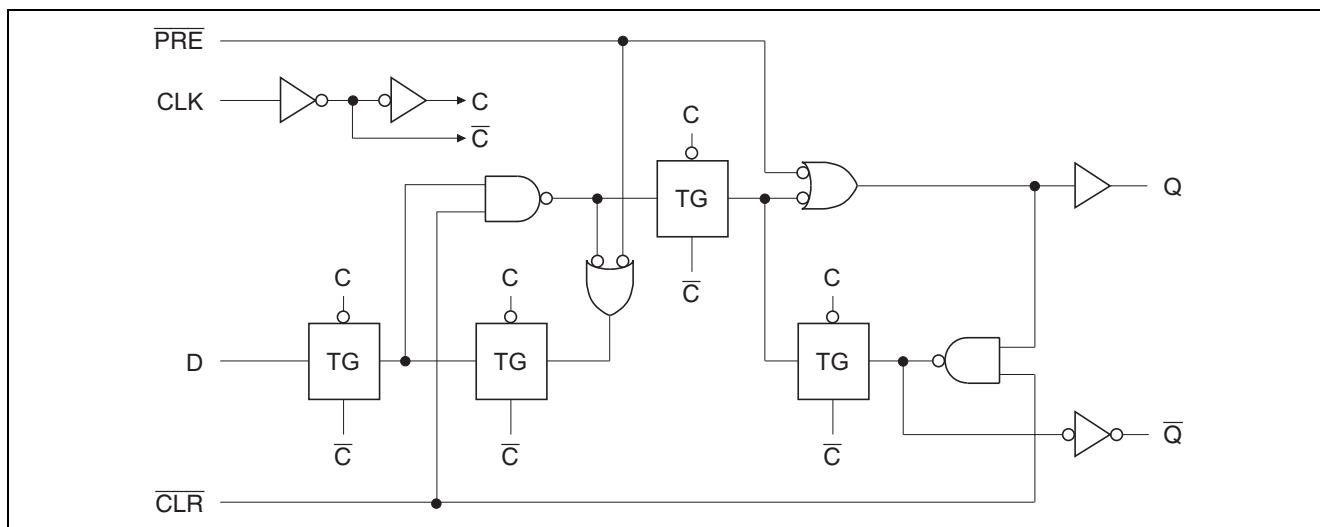
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

| Item | Symbol | Min | Max | Unit | Conditions |
|------------------------------------|-----------------------|------|----------|------------------|-----------------------------|
| Supply voltage range | V_{CC} | 1.65 | 5.5 | V | |
| Input voltage range | V_I | 0 | 5.5 | V | |
| Output voltage range | V_O | 0 | V_{CC} | V | |
| Output current | I_{OL} | — | 1 | mA | $V_{CC} = 1.65$ to 1.95 V |
| | | — | 2 | | $V_{CC} = 2.3$ to 2.7 V |
| | | — | 6 | | $V_{CC} = 3.0$ to 3.6 V |
| | | — | 12 | | $V_{CC} = 4.5$ to 5.5 V |
| | I_{OH} | — | -1 | | $V_{CC} = 1.65$ to 1.95 V |
| | | — | -2 | | $V_{CC} = 2.3$ to 2.7 V |
| | | — | -6 | | $V_{CC} = 3.0$ to 3.6 V |
| | | — | -12 | | $V_{CC} = 4.5$ to 5.5 V |
| Input transition rise or fall rate | $\Delta t / \Delta v$ | 0 | 300 | ns / V | $V_{CC} = 1.65$ to 1.95 V |
| | | 0 | 200 | | $V_{CC} = 2.3$ to 2.7 V |
| | | 0 | 100 | | $V_{CC} = 3.0$ to 3.6 V |
| | | 0 | 20 | | $V_{CC} = 4.5$ to 5.5 V |
| Operating free-air temperature | T_a | -40 | 85 | $^\circ\text{C}$ | |

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Electrical Characteristics

Ta = -40 to 85°C

| Item | Symbol | V _{CC} (V) * | Min | Typ | Max | Unit | Test condition |
|--------------------------|------------------|-----------------------|-----------------------|------|-----------------------|------|-----------------------------------------------------------------|
| Input voltage | V _{IH} | 1.65 to 1.95 | V _{CC} ×0.75 | — | — | V | |
| | | 2.3 to 2.7 | V _{CC} ×0.7 | — | — | | |
| | | 3.0 to 3.6 | V _{CC} ×0.7 | — | — | | |
| | | 4.5 to 5.5 | V _{CC} ×0.7 | — | — | | |
| | V _{IL} | 1.65 to 1.95 | — | — | V _{CC} ×0.25 | | |
| | | 2.3 to 2.7 | — | — | V _{CC} ×0.3 | | |
| | | 3.0 to 3.6 | — | — | V _{CC} ×0.3 | | |
| | | 4.5 to 5.5 | — | — | V _{CC} ×0.3 | | |
| Hysteresis voltage | V _H | 1.8 | — | 0.25 | — | V | V _I ⁺ – V _I [–] |
| | | 2.5 | — | 0.30 | — | | |
| | | 3.3 | — | 0.35 | — | | |
| | | 5.0 | — | 0.45 | — | | |
| Output voltage | V _{OH} | Min to Max | V _{CC} –0.1 | — | — | V | I _{OH} = –50 μA |
| | | 1.65 | 1.4 | — | — | | I _{OH} = –1 mA |
| | | 2.3 | 2.0 | — | — | | I _{OH} = –2 mA |
| | | 3.0 | 2.48 | — | — | | I _{OH} = –6 mA |
| | | 4.5 | 3.8 | — | — | | I _{OH} = –12 mA |
| | V _{OL} | Min to Max | — | — | 0.1 | | I _{OL} = 50 μA |
| | | 1.65 | — | — | 0.3 | | I _{OL} = 1 mA |
| | | 2.3 | — | — | 0.4 | | I _{OL} = 2 mA |
| | | 3.0 | — | — | 0.44 | | I _{OL} = 6 mA |
| | | 4.5 | — | — | 0.55 | | I _{OL} = 12 mA |
| Input current | I _{IN} | 0 to 5.5 | — | — | ±1 | μA | V _{IN} = 5.5 V or GND |
| Quiescent supply current | I _{CC} | 5.5 | — | — | 10 | μA | V _{IN} = V _{CC} or GND, I _O = 0 |
| Output leakage current | I _{OFF} | 0 | — | — | 5 | μA | V _{IN} or V _O = 0 to 5.5 V |
| Input capacitance | C _{IN} | 3.3 | — | 2.5 | — | pF | V _{IN} = V _{CC} or GND |

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$$V_{CC} = 1.8 \pm 0.15 \text{ V}$$

| Item | Symbol | T _a = 25°C | | | T _a = −40 to 85°C | | Unit | Test Conditions | FROM (Input) | TO (Output) |
|-------------------------|------------------|-----------------------|------|------|------------------------------|------|------|------------------------|---------------------|-------------|
| | | Min | Typ | Max | Min | Max | | | | |
| Maximum clock frequency | f _{max} | 30 | 60 | — | 20 | — | MHz | C _L = 15 pF | | |
| | | 20 | 40 | — | 15 | — | | C _L = 50 pF | | |
| Propagation delay time | t _{PLH} | — | 16.3 | 27.0 | 1.0 | 29.0 | ns | C _L = 15 pF | PRE/CLR | Q or Q̄ |
| | t _{PHL} | — | 17.9 | 29.0 | 1.0 | 32.0 | | | CLK | |
| | | — | 21.6 | 34.0 | 1.0 | 36.5 | | C _L = 50 pF | PRE/CLR | Q or Q̄ |
| | | — | 24.5 | 39.5 | 1.0 | 42.5 | | | CLK | |
| Setup time | t _{su} | 13.0 | — | — | 14.0 | — | ns | | D | |
| | | 9.0 | — | — | 9.0 | — | | | PRE or CLR inactive | |
| Hold time | t _h | 0.5 | — | — | 0.5 | — | ns | | | |
| Pulse width | t _w | 12.0 | — | — | 13.0 | — | ns | | PRE or CLR “L” | |
| | | 12.0 | — | — | 13.0 | — | | | CLK “H” or “L” | |

$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

| Item | Symbol | T _a = 25°C | | | T _a = −40 to 85°C | | Unit | Test Conditions | FROM (Input) | TO (Output) |
|-------------------------|------------------|-----------------------|------|------|------------------------------|------|------|------------------------|---------------------|-------------|
| | | Min | Typ | Max | Min | Max | | | | |
| Maximum clock frequency | f _{max} | 50 | 100 | — | 40 | — | MHz | C _L = 15 pF | | |
| | | 30 | 70 | — | 25 | — | | C _L = 50 pF | | |
| Propagation delay time | t _{PLH} | — | 9.8 | 14.8 | 1.0 | 17.0 | ns | C _L = 15 pF | PRE/CLR | Q or Q̄ |
| | t _{PHL} | — | 11.1 | 16.4 | 1.0 | 19.0 | | | CLK | |
| | | — | 13.0 | 17.4 | 1.0 | 20.0 | | C _L = 50 pF | PRE/CLR | Q or Q̄ |
| | | — | 14.2 | 20.0 | 1.0 | 23.0 | | | CLK | |
| Setup time | t _{su} | 8.0 | — | — | 9.0 | — | ns | | D | |
| | | 7.0 | — | — | 7.0 | — | | | PRE or CLR inactive | |
| Hold time | t _h | 0.5 | — | — | 0.5 | — | ns | | | |
| Pulse width | t _w | 8.0 | — | — | 9.0 | — | ns | | PRE or CLR “L” | |
| | | 8.0 | — | — | 9.0 | — | | | CLK “H” or “L” | |

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

| Item | Symbol | T _a = 25°C | | | T _a = −40 to 85°C | | Unit | Test Conditions | FROM (Input) | TO (Output) |
|-------------------------|------------------|-----------------------|------|------|------------------------------|------|------|------------------------|---------------------|-------------|
| | | Min | Typ | Max | Min | Max | | | | |
| Maximum clock frequency | f _{max} | 80 | 140 | — | 70 | — | MHz | C _L = 15 pF | | |
| | | 50 | 90 | — | 45 | — | | C _L = 50 pF | | |
| Propagation delay time | t _{PLH} | — | 6.9 | 12.3 | 1.0 | 14.5 | ns | C _L = 15 pF | PRE/CLR | Q or Q̄ |
| | t _{PHL} | — | 7.9 | 11.9 | 1.0 | 14.0 | | | CLK | |
| | | — | 9.2 | 15.8 | 1.0 | 18.0 | | C _L = 50 pF | PRE/CLR | Q or Q̄ |
| | | — | 10.2 | 15.4 | 1.0 | 17.5 | | | CLK | |
| Setup time | t _{su} | 6.0 | — | — | 7.0 | — | ns | | D | |
| | | 5.0 | — | — | 5.0 | — | | | PRE or CLR inactive | |
| Hold time | t _h | 0.5 | — | — | 0.5 | — | ns | | | |
| Pulse width | t _w | 6.0 | — | — | 7.0 | — | ns | | PRE or CLR “L” | |
| | | 6.0 | — | — | 7.0 | — | | | CLK “H” or “L” | |

$$V_{CC} = 5.0 \pm 0.5 \text{ V}$$

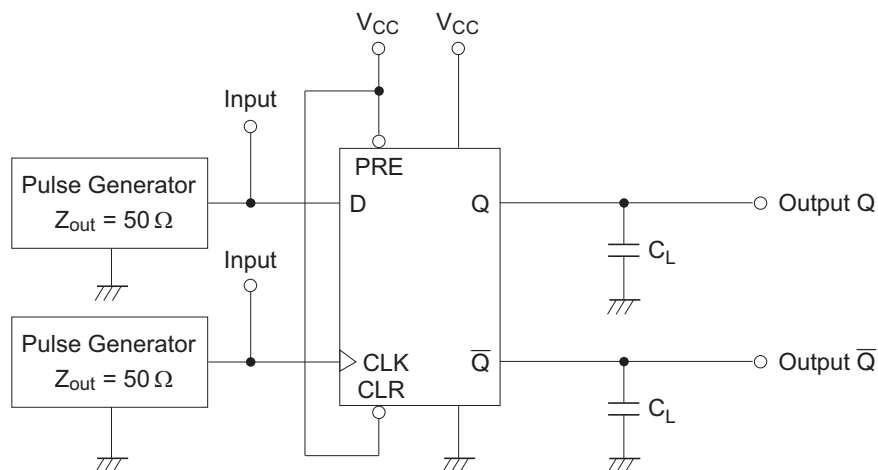
| Item | Symbol | T _a = 25°C | | | T _a = −40 to 85°C | | Unit | Test Conditions | FROM (Input) | TO (Output) |
|-------------------------|------------------|-----------------------|-----|-----|------------------------------|------|------|------------------------|---------------------|-------------|
| | | Min | Typ | Max | Min | Max | | | | |
| Maximum clock frequency | f _{max} | 130 | 180 | — | 110 | — | MHz | C _L = 15 pF | | |
| | | 90 | 140 | — | 75 | — | | C _L = 50 pF | | |
| Propagation delay time | t _{PLH} | — | 5.0 | 7.7 | 1.0 | 9.0 | ns | C _L = 15 pF | PRE/CLR | Q or Q̄ |
| | t _{PHL} | — | 5.6 | 7.3 | 1.0 | 8.5 | | | CLK | |
| | | — | 6.6 | 9.7 | 1.0 | 11.0 | | C _L = 50 pF | PRE/CLR | Q or Q̄ |
| | | — | 7.2 | 9.3 | 1.0 | 10.5 | | | CLK | |
| Setup time | t _{su} | 5.0 | — | — | 5.0 | — | ns | | D | |
| | | 3.0 | — | — | 3.0 | — | | | PRE or CLR inactive | |
| Hold time | t _h | 0.5 | — | — | 0.5 | — | ns | | | |
| Pulse width | t _w | 5.0 | — | — | 5.0 | — | ns | | PRE or CLR “L” | |
| | | 5.0 | — | — | 5.0 | — | | | CLK “H” or “L” | |

Operating Characteristics

$$C_L = 50 \text{ pF}$$

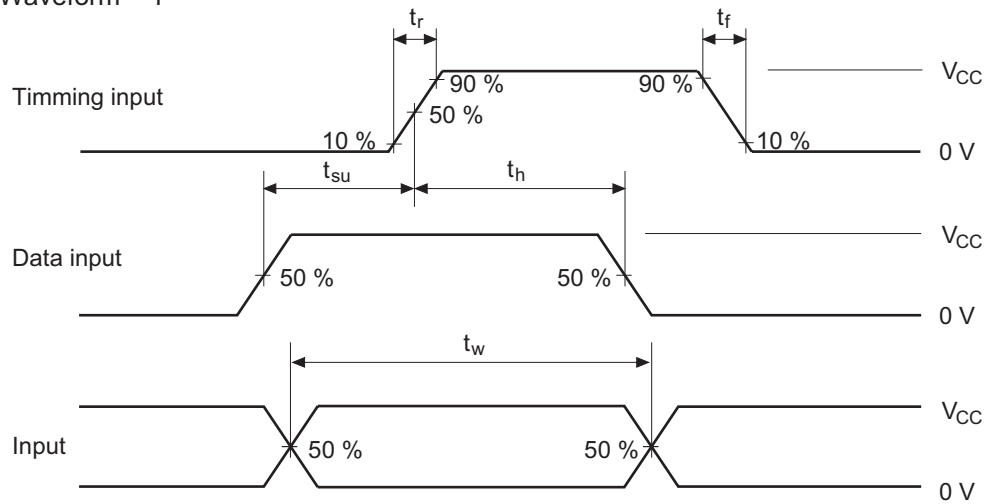
| Item | Symbol | $V_{CC} \text{ (V)}$ | $T_a = 25^\circ\text{C}$ | | | Unit | Test Conditions |
|-------------------------------|----------|----------------------|--------------------------|------|-----|------|----------------------|
| | | | Min | Typ | Max | | |
| Power dissipation capacitance | C_{PD} | 3.3 | — | 13.0 | — | pF | $f = 10 \text{ MHz}$ |
| | | 5.0 | — | 14.0 | — | | |

Test Circuit

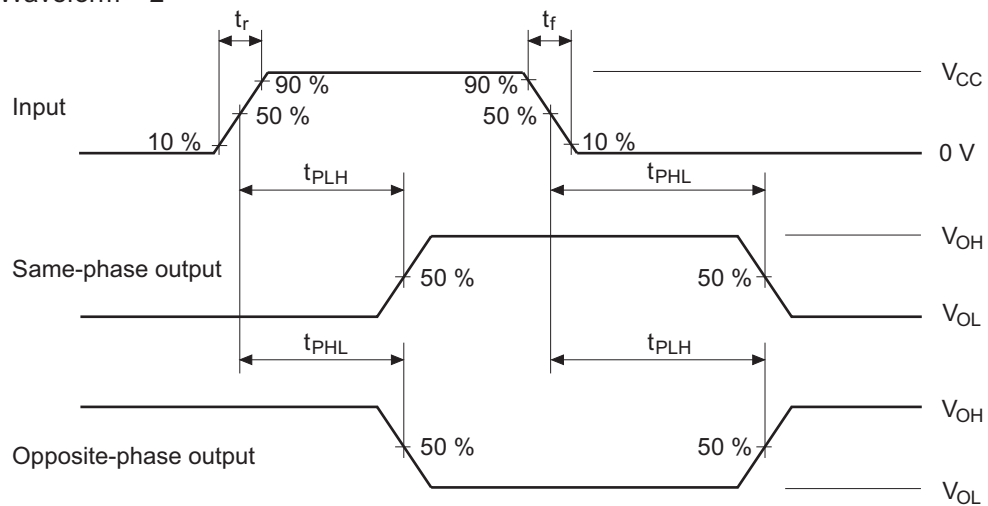


- Notes: 1. C_L includes probe and jig capacitance.
2. Test is put into the each flip flops.

• Waveform – 1

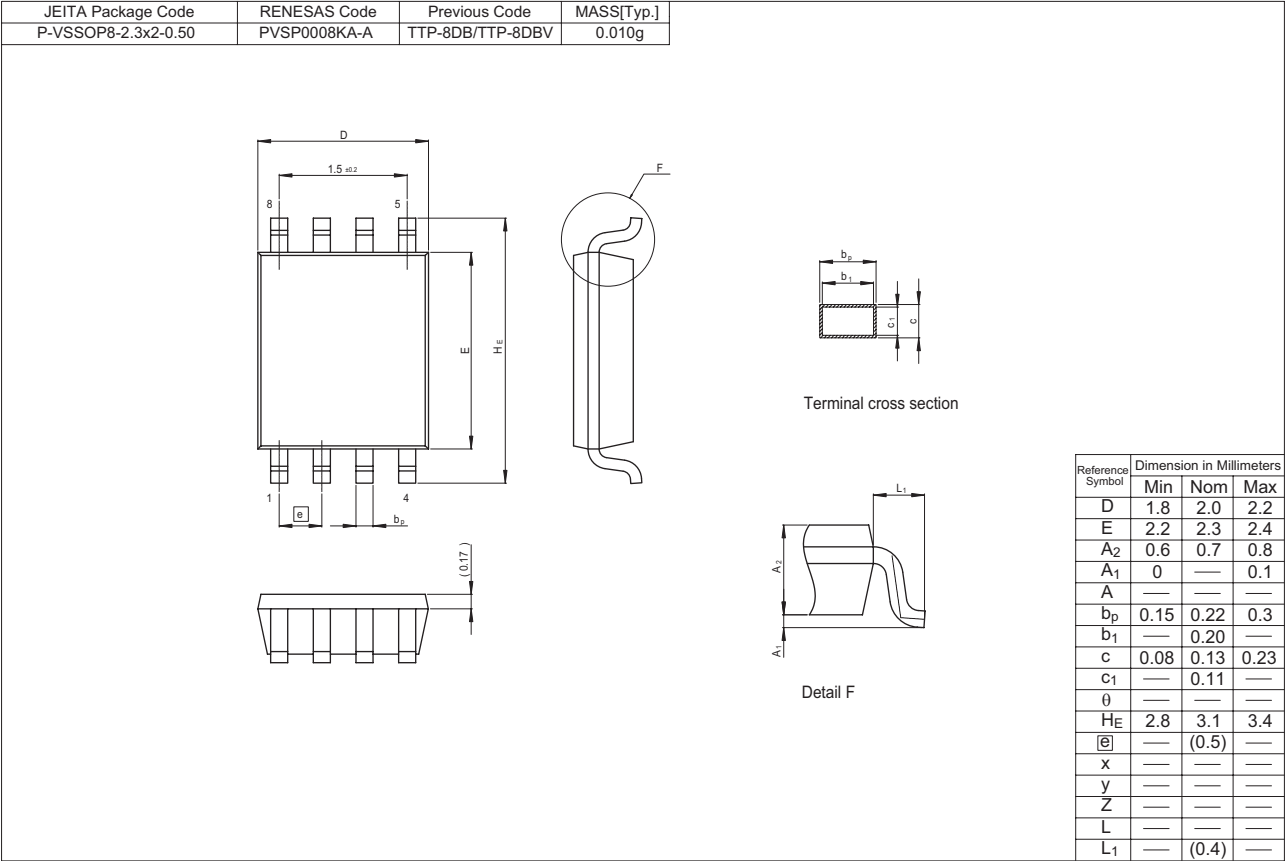


• Waveform – 2



- Notes: 1. Input waveform : $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions



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