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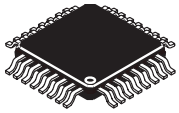
RoHS

LIN System Basis Chip with 2x60mA High Side Drivers

33910

SYSTEM BASIS CHIP WITH LIN 2ND GENERATION



AC SUFFIX (Pb-FREE)
98ASH70029A
32-PIN LQFP

The 33910 is a Serial Peripheral Interface (SPI)-controlled System Basis Chip (SBC), that combines many frequently used functions in an MCU-based system, plus a Local Interconnect Network (LIN) transceiver. It has a 5.0V, 60mA low dropout regulator with full protection and reporting features. The device provides full SPI-readable diagnostic and a selectable timing watchdog for detecting errant operation. The LIN Protocol Specification, version 2.0 compliant LIN transceiver has waveshaping circuitry that can be disabled for higher data rates.

Two 60mA high side switches with optional pulse-width modulation (PWM) are implemented to drive small loads. One high voltage input is available for use in contact monitoring or as external wake-up input. This input can be used as high voltage Analog Input as well. The voltage on this pin is divided by a selectable ratio and available via an analog multiplexer.

The 33910 has three main operating modes: Normal (all functions available); Sleep (V_{DD} off, wake-up via LIN, wake-up input (L1), cyclic sense and forced wake-up) and Stop (V_{DD} on with limited current capability, wake-up via $\overline{CS}$, LIN bus, wake-up input, cyclic sense, forced wake-up and external reset).

The 33910 is compatible with LIN Protocol Specification 2.0.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33910BAC/R2	-40°C to 125°C	32-LQFP
MC34910BAC/R2	-40°C to 85°C	

Features

- Two 60mA high side switches
- One high voltage analog/logic input
- Full-duplex SPI at frequencies up to 4MHz
- LIN transceiver capable of up to 100kbps with wave shaping
- Configurable window watchdog
- 5.0V low drop regulator with fault detection and low voltage reset (LVR) circuitry
- Switched/protected 5.0V output (used for Hall sensors)
- Pb-free packaging designated by suffix code AC

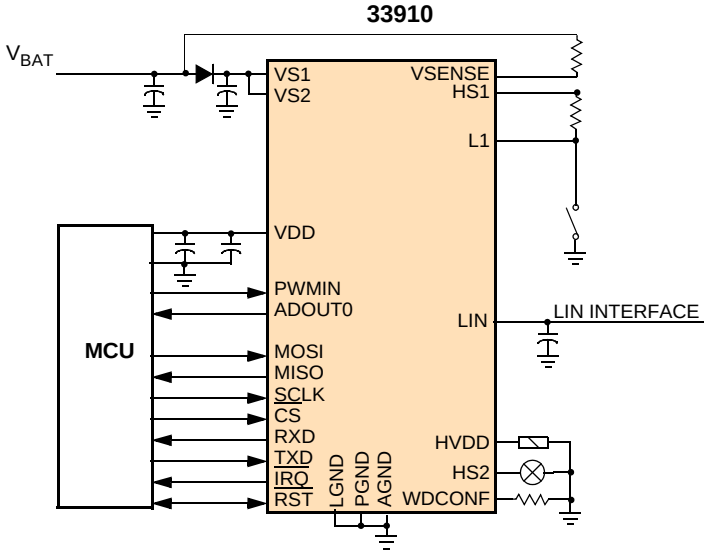


Figure 1. 33910 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

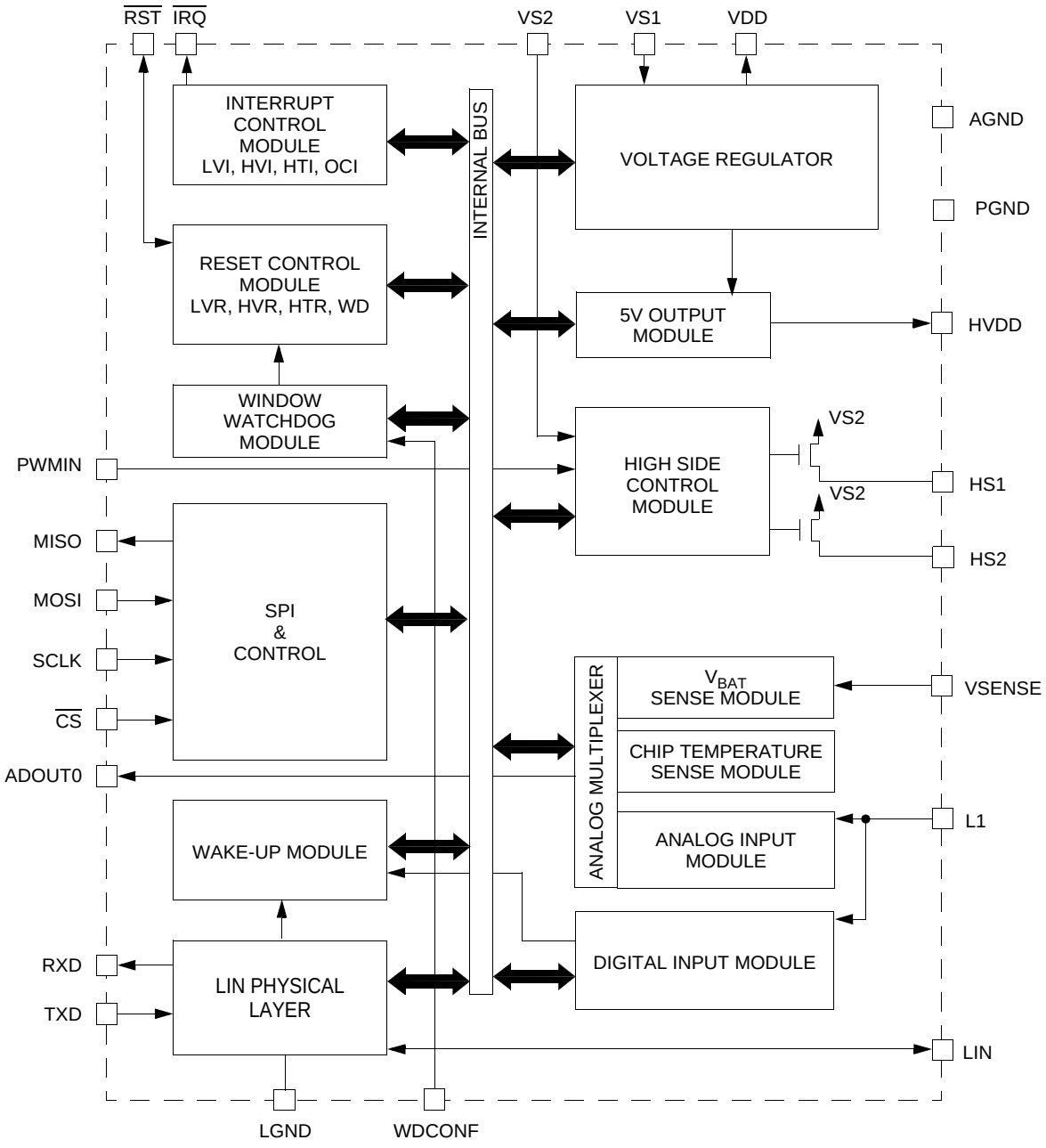


Figure 2. 33910 Simplified Internal Block Diagram

PIN CONNECTIONS

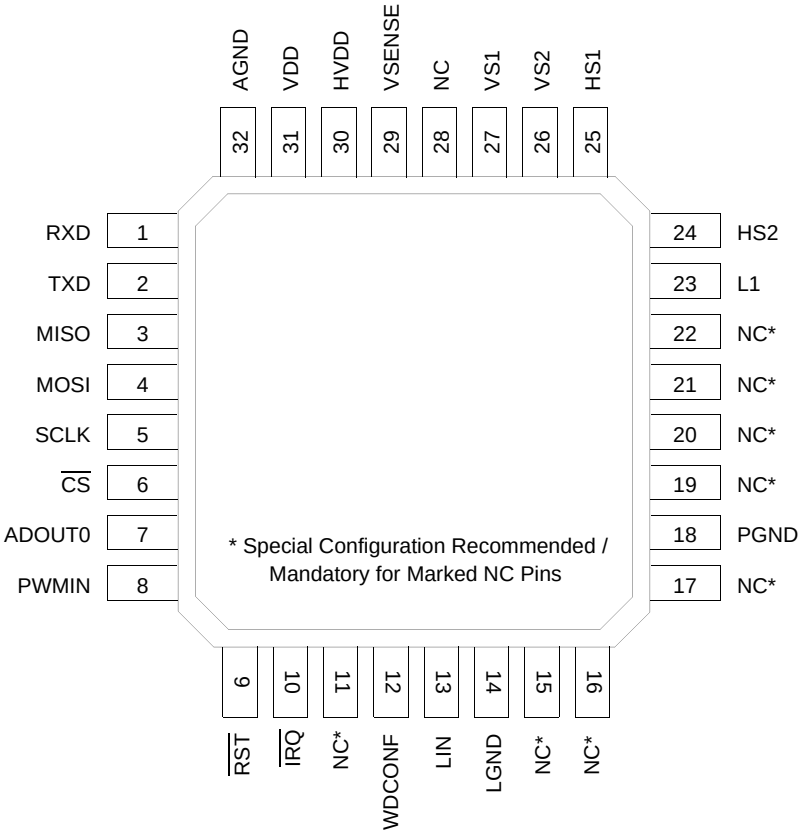


Figure 3. 33910 Pin Connections

Table 1. 33910 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin	Pin Name	Formal Name	Definition
1	RXD	Receiver Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	TXD	Transmitter Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
3	MISO	SPI Output	SPI data output. When $\overline{CS}$ is high, the pin is in the high-impedance state.
4	MOSI	SPI Input	SPI data input.
5	SCLK	SPI Clock	SPI clock Input.
6	$\overline{CS}$	SPI Chip Select	SPI chip select input pin. $\overline{CS}$ is active low.
7	ADOUT0	Analog Output Pin 0	Analog multiplexer output.
8	PWMIN	PWM Input	High side pulse width modulation input.
9	$\overline{RST}$	Internal Reset I/O	Bidirectional reset I/O pin - driven low when any internal reset source is asserted. $\overline{RST}$ is active low.
10	$\overline{IRQ}$	Internal Interrupt Output	Interrupt output pin, indicating wake-up events from Stop Mode or events from Normal and Normal Request Modes. $\overline{IRQ}$ is active low.
11, 15-17, 19-22, 28	NC		No connect

Table 1. 33910 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin	Pin Name	Formal Name	Definition
12	WDCONF	Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
13	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
14	LGND	LIN Ground Pin	This pin is the device LIN ground connection. It is internally connected to the PGND pin.
18	PGND	Power Ground Pin	This pin is the device power ground connection. It is internally connected to the LGND pin.
23	L1	Wake-up Input	This pin is a wake-up capable digital input(1). In addition, L1 can be sensed analog via the analog multiplexer.
24, 25	HS2, HS1	High Side Outputs	High side switch outputs.
26, 27	VS2, VS1	Power Supply Pin	These pins are device battery level power supply pins. VS2 is supplying the HS1 driver while VS1 supplies the remaining blocks.(2)
29	VSENSE	Voltage Sense Pin	Battery voltage sense input.(3)
30	HVDD	Hall Sensor Supply Output	+5.0V switchable supply output pin.(4)
31	VDD	Voltage Regulator Output	+5.0V main voltage regulator output pin.(5)
32	AGND	Analog Ground Pin	This pin is the device analog ground connection.

Notes

1. When used as digital input, a series 33kΩ resistor must be used to protect against automotive transients.
2. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
3. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10kΩ resistor in series with this pin for protection purposes.
4. External capacitor (1µF < C < 10µF; 0.1Ω < ESR < 5Ω) required.
5. External capacitor (2µF < C < 100µF; 0.1Ω < ESR < 10Ω) required.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage at VS1 and VS2 Normal Operation (DC) Transient Conditions (load dump)	 $V_{SUP(SS)}$ $V_{SUP(PK)}$	 -0.3 to 27 -0.3 to 40	V
Supply Voltage at VDD	V_{DD}	-0.3 to 5.5	V
Input / Output Pins Voltage[6] $\overline{CS}$, $\overline{RST}$, SCLK, PWMIN, ADOUT0, MOSI, MISO, TXD, RXD Interrupt Pin ($\overline{IRQ}$)[7]	 V_{IN} $V_{IN(IRQ)}$	 -0.3 to V_{DD}+0.3 -0.3 to 11	V
HS1 Pin Voltage (DC)	V_{HS1}	-0.3 to V_{SUP}+0.3	V
HS2 Pin Voltage (DC)	V_{HS2}	-0.3 to V_{SUP}+0.3	V
L1 Pin Voltage Normal Operation with a series 33kΩ resistor (DC) Transient input voltage with external component (according to ISO7637-2) (See Figure 5, page 16)	 V_{L1DC} V_{L1TR}	 -18 to 40 ±100	V
VSENSE Pin Voltage (DC)	V_{VSENSE}	-27 to 40	V
LIN Pin Voltage Normal Operation (DC) Transient input voltage with external component (according to ISO7637-2) (See Figure 4, page 16)	 V_{BUSDC} V_{BUSTR}	 -18 to 40 -150 to 100	V
VDD output current	I_{VDD}	Internally Limited	A
ESD Voltage[8] Human Body Model - LIN Pin Human Body Model - all other Pins Machine Model Charge Device Model Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25 and 32) All other Pins (Pins 2-7, 10-15, 18-23, 26-31)	 V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3-1} V_{ESD3-2}	 ±8000 ±2000 ±200 ±750 ±500	V
NC Pin Voltage (NC pins 11, 15, 16, 17, 19, 20, 21, 22, and 28)[9]	V_{NC}	Note 9	

Notes

6. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
7. Extended voltage range for programming purpose only.
8. Testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0Ω), and the Charge Device Model, Robotic (C_{ZAP} = 4.0pF).
9. Special configuration recommended / mandatory for marked NC pins. Please refer to the typical application shown on page 40.

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Operating Ambient Temperature[10] 33910 34910	T_A	 -40 to 125 -40 to 85	°C
Operating Junction Temperature[10]	T_J	-40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance, Junction to Ambient Natural Convection, Single Layer board (1s)[11, 12] Natural Convection, Four Layer board (2s2p)[11, 13]	$R_{\theta JA}$	 85 56	°C/W
Thermal Resistance, Junction to Case[14]	$R_{\theta JC}$	23	°C/W
Peak Package Reflow Temperature During Reflow[15, 16]	T_{PPRT}	Note 16	°C

Notes

10. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
11. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
12. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
13. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
14. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
15. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
16. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE (VS1, VS2)					
Nominal Operating Voltage	V_{SUP}	5.5	–	18	V
Functional Operating Voltage[17]	V_{SUPOP}	–	–	27	V
Load Dump	V_{SUPLD}	–	–	40	V
SUPPLY CURRENT RANGE (V_{SUP} = 13.5V)					
Normal Mode (I_{OUT} at V_{DD} = 10mA), LIN Recessive State[18]	I_{RUN}	–	4.5	10	mA
Stop Mode, VDD ON with I_{OUT} = 100µA, LIN Recessive State[18], [19], [20]	I_{STOP}				µA
5.5V < V_{SUP} < 12V		–	48	80	
V_{SUP} = 13.5V		–	58	90	
Sleep Mode, VDD OFF, LIN Recessive State[18], [20]	I_{SLEEP}				µA
5.5V < V_{SUP} < 12V		–	27	35	
12V ≤ V_{SUP} < 13.5V		–	37	48	
Cyclic Sense Supply Current Adder[21]	I_{CYCLIC}	–	10	–	µA
SUPPLY UNDER/OVER-VOLTAGE DETECTIONS					
Power-On Reset (BATFAIL)[22]					V
Threshold (measured on VS1)[21]	$V_{BATFAIL}$	1.5	3.0	3.9	
Hysteresis (measured on VS1)[21]	$V_{BATFAIL\_HYS}$	–	0.9	–	
V_{SUP} under-voltage detection (VSUV Flag) (Normal and Normal Request Modes, Interrupt Generated)					V
Threshold (measured on VS1)	V_{SUV}	5.55	6.0	6.6	
Hysteresis (measured on VS1)	V_{SUV_HYS}	–	1.0	–	
V_{SUP} over-voltage detection (VSOV Flag) (Normal and Normal Request Modes, Interrupt Generated)					V
Threshold (measured on VS1)	V_{SOV}	18	19.25	20.5	
Hysteresis (measured on VS1)	V_{SOV_HYS}	–	1.0	–	

Notes

17. Device is fully functional. All features are operating.
18. Total current (I_{VS1} + I_{VS2}) measured at GND pins excluding all loads, Cyclic Sense disabled.
19. Total I_{DD} current (including loads) below 100µA.
20. Stop and Sleep Mode currents will increase if V_{SUP} exceeds13.5V.
21. This parameter is guaranteed by process monitoring but, not production tested.
22. The flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR[23] (VDD)					
Normal Mode Output Voltage 1.0mA < I_{VDD} < 50mA; 5.5V < V_{SUP} < 27V	V_{DDRUN}	4.75	5.00	5.25	V
Normal Mode Output Current Limitation	I_{VDDRUN}	60	110	200	mA
Dropout Voltage[24] I_{VDD} = 50mA	V_{DDDROP}	–	0.1	0.25	V
Stop Mode Output Voltage I_{VDD} < 5mA	V_{DDSTOP}	4.75	5.0	5.25	V
Stop Mode Output Current Limitation	$I_{VDDSTOP}$	6.0	12	36	mA
Line Regulation Normal Mode, 5.5V < V_{SUP} < 18V; I_{VDD} = 10mA Stop Mode, 5.5V < V_{SUP} < 18V; I_{VDD} = 1.0mA	 LR_{RUN} LR_{STOP}	 – –	 20 5.0	 25 25	mV
Load Regulation Normal Mode, 1.0mA < I_{VDD} < 50mA Stop Mode, 0.1mA < I_{VDD} < 5mA	 LD_{RUN} LD_{STOP}	 – –	 15 10	 80 50	mV
Over-temperature Prewarning (Junction)[25] Interrupt generated, Bit VDDOT Set	T_{PRE}	110	125	140	°C
Over-temperature Pre-Warning hysteresis[25]	T_{PRE_HYS}	–	10	–	°C
Over-temperature Shutdown Temperature (Junction)[25]	T_{SD}	155	170	185	°C
Over-temperature Shutdown hysteresis[25]	T_{SD_HYS}	–	10	–	°C
HALL SENSOR SUPPLY OUTPUT[26] (HVDD)					
V_{DD} Voltage matching H_{VDDACC} = (HVDD-VDD) / VDD * 100% I_{HVDD} = 15mA	H_{VDDACC}	-2.0	–	2.0	%
Current Limitation	I_{HVDD}	20	30	50	mA
Dropout Voltage I_{HVDD} = 15mA; I_{VDD} = 5mA	$H_{VDDDROP}$	–	160	300	mV
Line Regulation I_{HVDD} = 5mA; I_{VDD} = 5mA	LR_{HVDD}	–	25	40	mV
Load Regulation 1mA > I_{HVDD} > 15mA; I_{VDD} = 5mA	LD_{HVDD}	–	10	20	mV

Notes

23. Specification with external capacitor 2µF < C < 100µF and 100mΩ ≤ ESR ≤ 10Ω.
24. Measured when voltage has dropped 250mV below its nominal Value (5V).
25. This parameter is guaranteed by process monitoring but, not production tested.
26. Specification with external capacitor 1µF < C < 10µF and 100mΩ ≤ ESR ≤ 10Ω.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ INPUT/OUTPUT PIN ($\overline{RST}$)					
VDD Low Voltage Reset Threshold	$V_{\overline{RSTTH}}$	4.3	4.5	4.7	V
Low-State Output Voltage I_{OUT} = 1.5mA; 3.5V ≤ V_{SUP} ≤ 27V	V_{OL}	0.0	–	0.9	V
High-State Output Current (0 < V_{OUT} < 3.5V)	I_{OH}	-150	-250	-350	µA
Pull-down Current Limitation (internally limited) V_{OUT} = V_{DD}	I_{PD_MAX}	1.5	–	8.0	mA
Low-State Input Voltage	V_{IL}	-0.3	–	0.3 x V_{DD}	V
High-State Input Voltage	V_{IH}	0.7 x V_{DD}	–	V_{DD} + 0.3	V
MISO SPI OUTPUT PIN (MISO)					
Low-State Output Voltage I_{OUT} = 1.5mA	V_{OL}	0.0	–	1.0	V
High-State Output Voltage I_{OUT} = -250µA	V_{OH}	V_{DD} - 0.9	–	V_{DD}	V
Tri-state Leakage Current 0 V ≤ V_{MISO} ≤ V_{DD}	$I_{TriMISO}$	-10	–	10	µA
SPI INPUT PINS (MOSI, SCLK, $\overline{CS}$)					
Low-state Input Voltage	V_{IL}	-0.3	–	0.3 x V_{DD}	V
High-state Input Voltage	V_{IH}	0.7 x V_{DD}	–	V_{DD} + 0.3	V
MOSI, SCLK Input Current 0 ≤ V_{IN} ≤ V_{DD}	I_{IN}	-10	–	10	µA
$\overline{CS}$ Pull-up current 0 < V_{IN} < 3.5V	$I_{PU\overline{CS}}$	10	20	30	µA
INTERRUPT OUTPUT PIN ($\overline{IRQ}$)					
Low-state Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	–	0.8	V
High-state Output Voltage I_{OUT} = -250µA	V_{OH}	V_{DD} - 0.8	–	V_{DD}	V
Leakage current V_{DD} ≤ V_{OUT} ≤ 10V	V_{OH}	–	–	2.0	mA
PULSE WIDTH MODULATION INPUT PIN (PWMIN)					
Low-state Input Voltage	V_{IL}	-0.3	–	0.3 x V_{DD}	V
High-state Input Voltage	V_{IH}	0.7 x V_{DD}	–	V_{DD} + 0.3	V
Pull-up current 0 < V_{IN} < 3.5V	$I_{PUPWMIN}$	10	20	30	µA

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUT HS1 AND HS2 PINS (HS1, HS2)					
Output Drain-to-Source On Resistance	$R_{DS(ON)}$				Ω
T_J = 25°C, I_{LOAD} = 50mA; V_{SUP} > 9.0V		–	–	7.0	
T_J = 150°C, I_{LOAD} = 50mA; V_{SUP} > 9.0V[27]		–	–	10	
T_J = 150°C, I_{LOAD} = 30mA; 5.5V < V_{SUP} < 9.0V[27]		–	–	14	
Output Current Limitation[28]	I_{LIMHS1}				mA
0V < V_{OUT} < V_{SUP} - 2.0V		60	120	250	
Open Load Current Detection[29]	I_{OLHSx}	–	5.0	7.5	mA
Leakage Current (-0.2V < V_{HSx} < V_{S2} + 0.2V)	I_{LEAK}	–	–	10	µA
Short Circuit Detection Threshold[30]	V_{THSC}				V
5.5V < V_{SUP} < 27V		V_{SUP} - 2	–	–	
Over-temperature Shutdown[31], [32]	T_{HSSD}	150	165	180	°C
Over-temperature Shutdown Hysteresis[32]	T_{HSSD_HYS}	–	10	–	°C
L1 INPUT PIN (L1)					
Low Detection Threshold	V_{THL}				V
5.5V < V_{SUP} < 27V		2.0	2.5	3.0	
High Detection Threshold	V_{THH}				V
5.5V < V_{SUP} < 27V		3.0	3.5	4.0	
Hysteresis	V_{HYS}				V
5.5V < V_{SUP} < 27V		0.5	1.0	1.5	
Input Current[33]	I_{IN}				µA
-0.2V < V_{IN} < VS1		-10	–	10	
Analog Input Impedance[34]	R_{L1IN}	800	1550	–	kΩ
Analog Input Divider Ratio ($RATIO_{L1}$ = V_{L1} / V_{ADOUT0})	$RATIO_{L1}$				
L1DS (L1 Divider Select) = 0		0.95	1.0	1.05	
L1DS (L1 Divider Select) = 1		3.42	3.6	3.78	
Analog Output Offset Ratio	$V_{RATIOL1-OFFSET}$				mV
L1DS (L1 Divider Select) = 0		-80	0.0	80	
L1DS (L1 Divider Select) = 1		-22	0.0	22	
Analog Inputs Matching	$L1_{MATCHING}$				%
L1DS (L1 Divider Select) = 0		96	100	104	
L1DS (L1 Divider Select) = 1		96	100	104	

Notes

27. This parameter is production tested up to T_A = 125°C and guaranteed by process monitoring up to T_J = 150°C.
28. When over-current occurs, the high side stays ON with limited current capability and the HS1CL flag is set in the HSSR.
29. When open-load occurs, the flag (HS1OP) is set in the HSSR.
30. When short circuit occurs and if HVSE flag is enabled, HS1 automatic shutdown.
31. When over-temperature shutdown occurs, both High Sides are turned off. All flags in HSSR are set.
32. Guaranteed by characterization but, not production tested
33. Analog multiplexer input disconnected from L1 input pin.
34. Analog multiplexer input connected to L1 input pin.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
External Resistor Range	R_{EXT}	20	–	200	kΩ
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy)(35)	WD_{ACC}	-15	–	15	%
ANALOG MULTIPLEXER					
Internal Chip Temperature Sense Gain	S_{TTOV}	–	10.5	–	mV/K
VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / V_{ADOUT0}) 5.5V < V_{SUP} < 27V	$RATIO_{VSENSE}$	5.0	5.25	5.5	
VSENSE Output Related Offset -40°C < T_A < -20°C	$OFFSET_{VSENSE}$	-30 -45	– –	30 45	mV
ANALOG OUTPUT (ADOUT0)					
Maximum Output Voltage -5mA < I_O < 5mA	V_{OUT_MAX}	V_{DD} - 0.35	–	V_{DD}	V
Minimum Output Voltage -5mA < I_O < 5mA	V_{OUT_MIN}	0.0	–	0.35	V
RXD OUTPUT PIN (LIN PHYSICAL LAYER) (RXD)					
Low-state Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	–	0.8	V
High-state Output Voltage I_{OUT} = -250µA	V_{OH}	V_{DD}-0.8	–	V_{DD}	V
TXD INPUT PIN (LIN PHYSICAL LAYER) (TXD)					
Low-state Input Voltage	V_{IL}	-0.3	–	0.3 x nV_{DD}	V
High-state Input Voltage	V_{IH}	0.7 x V_{DD}	–	V_{DD} + 0.3	V
Pin Pull-up Current, 0 < V_{IN} < 3.5V	I_{PUIN}	10	20	30	µA

Notes

35. Watchdog timing period calculation formula: t_{PWD} [ms] = 0.466 * (R_{EXT} - 20) + 10 (R_{EXT} in kΩ)

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER, TRANSCEIVER (LIN)(36)					
Output Current Limitation Dominant State, V_{BUS} = 18V	I_{BUSLIM}	 40	 120	 200	mA
Leakage Output Current to GND Dominant State; V_{BUS} = 0V; V_{BAT} = 12V Recessive State; 8V < V_{BAT} < 18V; 8V < V_{BUS} < 18V; $V_{BUS} \geq V_{BAT}$ GND Disconnected; GND_{DEVICE} = V_{SUP}; V_{BAT} = 12V; 0 < V_{BUS} < 18V V_{BAT} disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18V	 $I_{BUS\_PAS\_DOM}$ $I_{BUS\_PAS\_REC}$ $I_{BUS\_NO\_GND}$ I_{BUS}	 -1.0 – -1.0 –	 – – – –	 – 20 1.0 100	 mA µA mA µA
Receiver Input Voltages Receiver Dominant State Receiver Recessive State Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2 Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	 V_{BUSDOM} V_{BUSREC} V_{BUS_CNT} V_{HYS}	 – 0.6 0.475 –	 – – 0.5 –	 0.4 – 0.525 0.175	V_{SUP}
LIN Transceiver Output Voltage Recessive State, TXD HIGH, I_{OUT} = 1.0 µA Dominant State, TXD LOW, 500Ω External Pull-up Resistor, LDVS = 0 Dominant State, TXD LOW, 500Ω External Pull-up Resistor, LDVS = 1	 V_{LIN_REC} $V_{LIN\_DOM\_0}$ $V_{LIN\_DOM\_1}$	 V_{SUP}-1 – –	 – 1.1 1.7	 – 1.4 2	V
LIN Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Over-temperature Shutdown(37)	T_{LINSD}	150	165	180	°C
Over-temperature Shutdown Hysteresis	T_{LINSD_HYS}	–	10	–	°C

Notes

36. Parameters guaranteed for 7.0V ≤ V_{SUP} ≤ 18V.
37. When Over-temperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING (Figure 13)					
SPI Operating Frequency	f_{SPIOP}	–	–	4.0	MHz
SCLK Clock Period	t_{PSCLK}	250	–	N/A	ns
SCLK Clock High Time(38)	t_{WSCLKH}	110	–	N/A	ns
SCLK Clock Low Time(38)	t_{WSCLKL}	110	–	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK(38)	t_{LEAD}	100	–	N/A	ns
Falling Edge of SCLK to $\overline{CS}$ Rising Edge(38)	t_{LAG}	100	–	N/A	ns
MOSI to Falling Edge of SCLK(38)	t_{SISU}	40	–	N/A	ns
Falling Edge of SCLK to MOSI(38)	t_{SIH}	40	–	N/A	ns
MISO Rise Time(38) C_L = 220pF	t_{RSO}	–	40	–	ns
MISO Fall Time(38) C_L = 220pF	t_{FSO}	–	40	–	ns
Time from Falling or Rising Edges of $\overline{CS}$ to:(38) - MISO Low-impedance - MISO High-impedance	 t_{SOEN} t_{SODIS}	 0.0 0.0	 – –	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid(38) 0.2 x V_{DD} ≤ MISO ≥ 0.8 x V_{DD}, C_L = 100pF	t_{VALID}	0.0	–	75	ns
$\overline{RST}$ OUTPUT PIN					
Reset Low-level Duration after V_{DD} High (See Figure 12, page 19)	$t_{\overline{RST}}$	0.65	1.0	1.35	ms
Reset Deglitch Filter Time	$t_{\overline{RSTDF}}$	350	600	900	ns
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
Watchdog Time Period(39) External Resistor R_{EXT} = 20kΩ (1%) External Resistor R_{EXT} = 200kΩ (1%) Without External Resistor R_{EXT} (WDCONF Pin Open)	t_{PWD}	 8.5 79 110	 10 94 150	 11.5 108 205	ms

Notes
38. This parameter is guaranteed by process monitoring but, not production tested.
39. Watchdog timing period calculation formula: t_{PWD} [ms] = 0.466 * (R_{EXT} - 20) + 10 (R_{EXT} in kΩ)

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
L1 INPUT					
Wake-up Filter Time	t_{WUF}	8.0	20	38	µs
STATE MACHINE TIMING					
Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation(40)	t_{STOP}	–	–	5.0	µs
Normal Request Mode Timeout (see Figure 12, page 19)	t_{NRTOUT}	110	150	205	ms
Delay Between SPI Command and HS Turn On(41) 9V < V_{SUP} < 27V	t_{S-ON}	–	–	10	µs
Delay Between SPI Command and HS Turn Off(41) 9V < V_{SUP} < 27V	t_{S-OFF}	–	–	10	µs
Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request Mode)(40)	t_{SNR2N}	–	–	10	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) in Stop Mode and: Normal Request Mode, VDD ON and $\overline{RST}$ HIGH First Accepted SPI Command	 $t_{WU\overline{CS}}$ t_{WUSPI}	 9.0 90	 15 —	 80 N/A	µs
Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	$t_{2\overline{CS}}$	4.0	—	—	µs
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0KBIT/SEC(42), (43)					
Duty Cycle 1: D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50µs 7.0V ≤ V_{SUP} ≤ 18V	D1	0.396	—	—	
Duty Cycle 2: D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50µs 7.6V ≤ V_{SUP} ≤ 18V	D2	—	—	0.581	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4KBIT/SEC(42),(44)					
Duty Cycle 3: D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96µs 7.0V ≤ V_{SUP} ≤ 18V	D3	0.417	—	—	µs
Duty Cycle 4: D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96µs 7.6V ≤ V_{SUP} ≤ 18V	D4	—	—	0.590	µs

Notes
40. This parameter is guaranteed by process monitoring but, not production tested.
41. Delay between turn on or off command (rising edge on $\overline{CS}$) and HS ON or OFF, excluding rise or fall time due to external load.
42. Bus load R_{BUS} and C_{BUS} 1.0nF / 1.0kΩ, 6.8nF / 660Ω, 10nF / 500Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6, page 17.
43. See Figure 7, page 17.
44. See Figure 8, page 17.

Table 4. Dynamic Electrical Characteristics (continued)

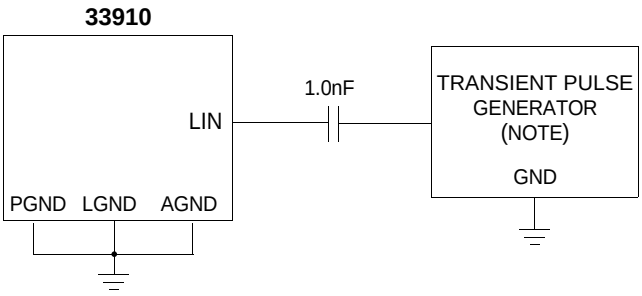
Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C for the 33910 and -40°C ≤ T_A ≤ 85°C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR FAST SLEW RATE					
LIN Fast Slew Rate (Programming Mode)	SR_{FAST}	—	20	—	V/µs
LIN PHYSICAL LAYER: CHARACTERISTICS AND WAKE-UP TIMINGS(45)					
Propagation Delay and Symmetry(46)					µs
Propagation Delay Receiver, t_{REC_PD}=max (t_{REC_PDR}, t_{REC_PDF})	t_{REC_PD}	—	3.0	6.0	
Symmetry of Receiver Propagation Delay t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	—	2.0	
Bus Wake-up Deglitcher (Sleep and Stop Modes)(47)	t_{PROPWL}	42	70	95	µs
Bus Wake-up Event Reported					µs
From Sleep Mode(48)	t_{WAKE}	—	—	1500	
From Stop Mode(49)	t_{WAKE}	9.0	13	17	
TXD Permanent Dominant State Delay	t_{TXDDOM}	0.65	1.0	1.35	s
PULSE WIDTH MODULATION INPUT PIN (PWMIN)					
PWMIN pin(50)	f_{PWMIN}				kHz
Max. frequency to drive HS output pins			10		

Notes

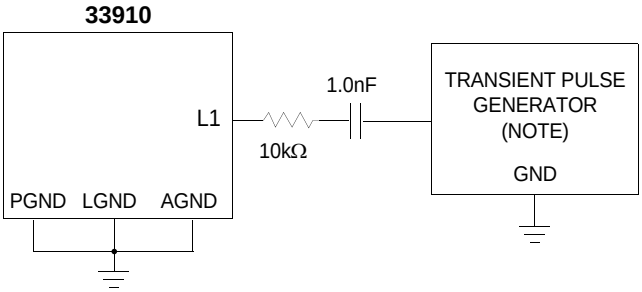
45. V_{SUP} from 7.0V to 18V, bus load R_{BUS} and C_{BUS} 1.0nF / 1.0kΩ, 6.8nF / 660Ω, 10 nF / 500Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6, page 17.
46. See Figure 9, page 18
47. See Figure 10, page 18 for Sleep and Figure 11, page 19 for Stop Mode.
48. The measurement is done with 1µF capacitor and 0mA current load on V_{DD}. The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See Figure 10, page 18. The delay depends of the load and capacitor on V_{DD}.
49. In Stop Mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{IRQ}$ pin. See Figure 11, page 18.
50. This parameter is guaranteed by process monitoring but, not production tested.

TIMING DIAGRAMS



NOTE: Waveform Per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 4. Test Circuit for Transient Test Pulses (LIN)



NOTE: Waveform Per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 5. Test Circuit for Transient Test Pulses (L1)

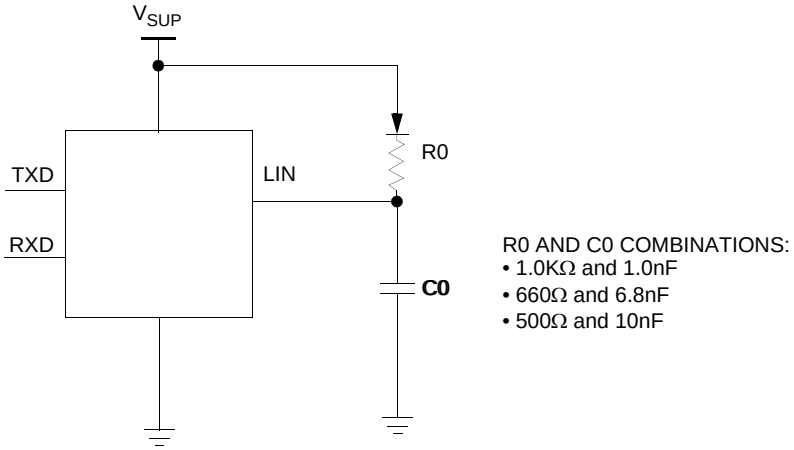


Figure 6. Test Circuit for LIN Timing Measurements

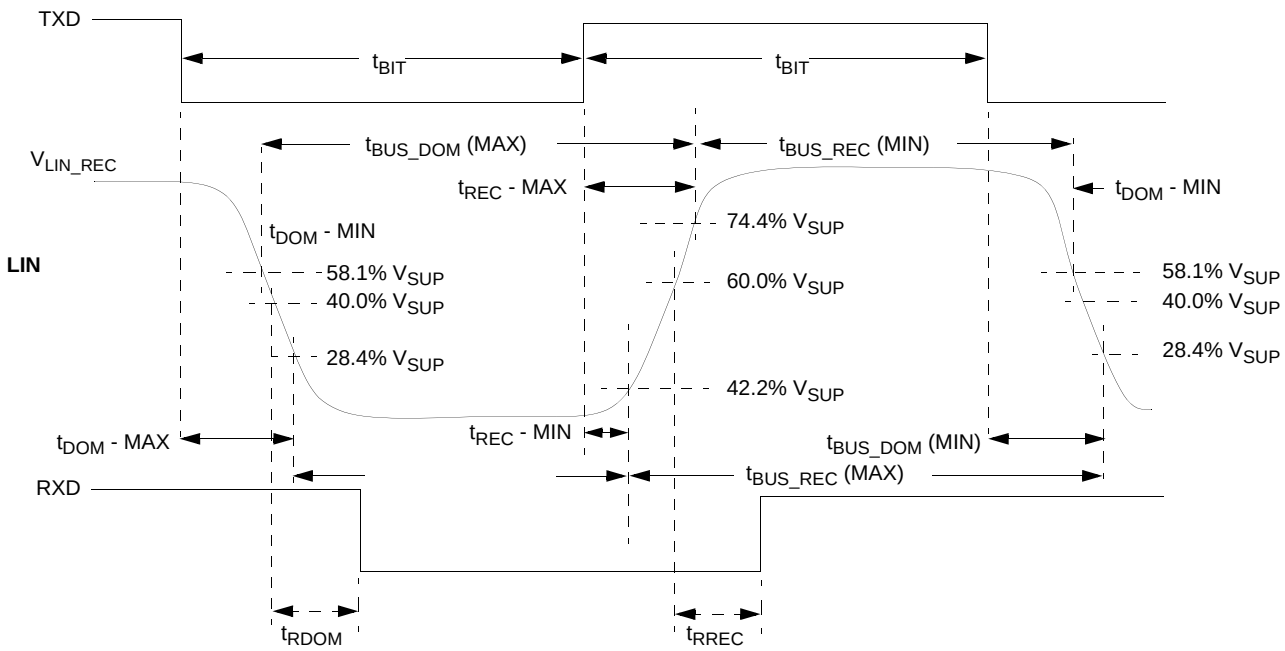


Figure 7. LIN Timing Measurements for Normal Slew Rate

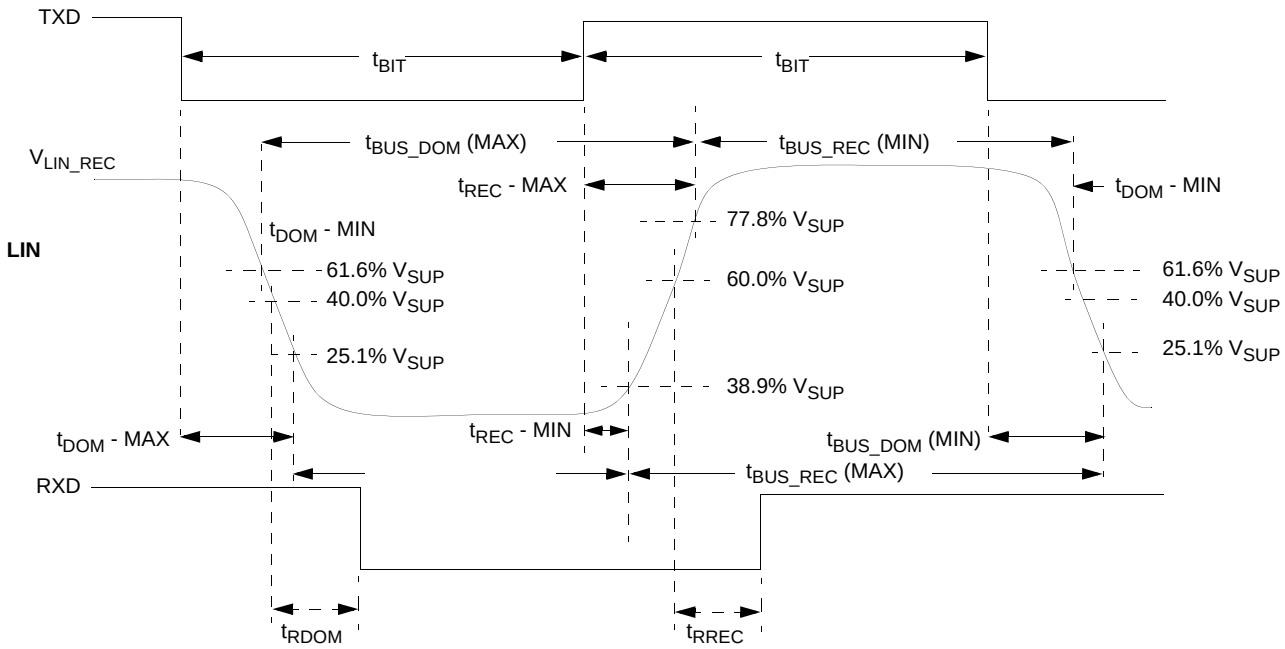


Figure 8. LIN Timing Measurements for Slow Slew Rate

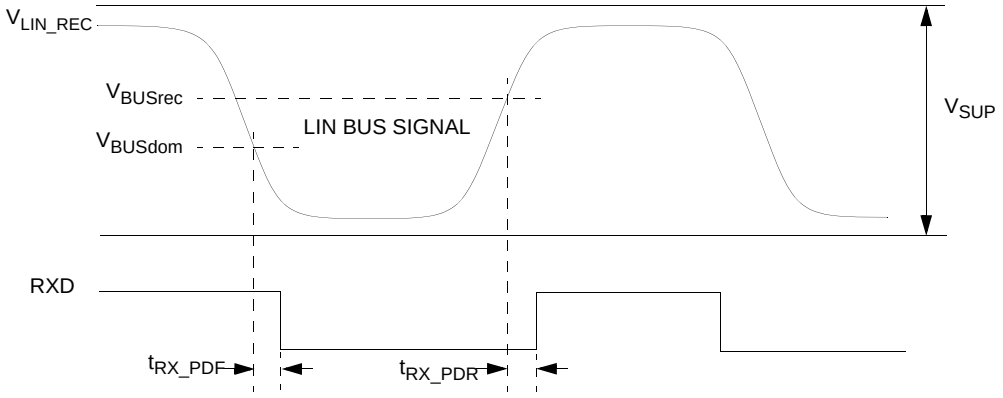


Figure 9. LIN Receiver Timing

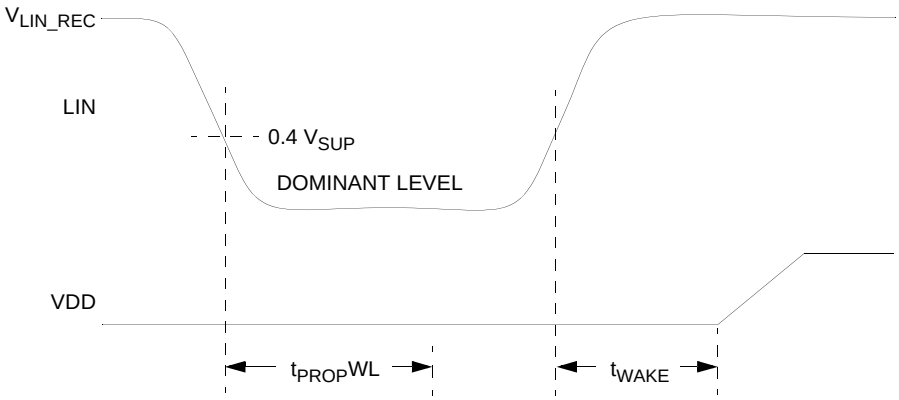


Figure 10. LIN Wake-up Sleep Mode Timing

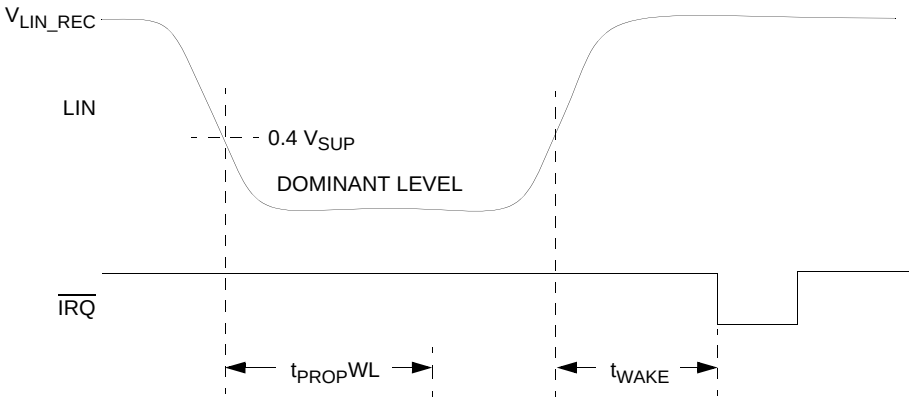


Figure 11. LIN Wake-up Stop Mode Timing

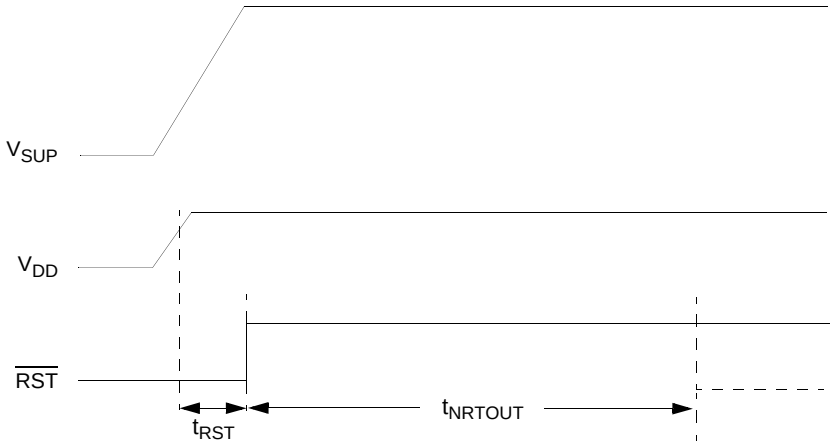


Figure 12. Power On Reset and Normal Request Time-Out Timing

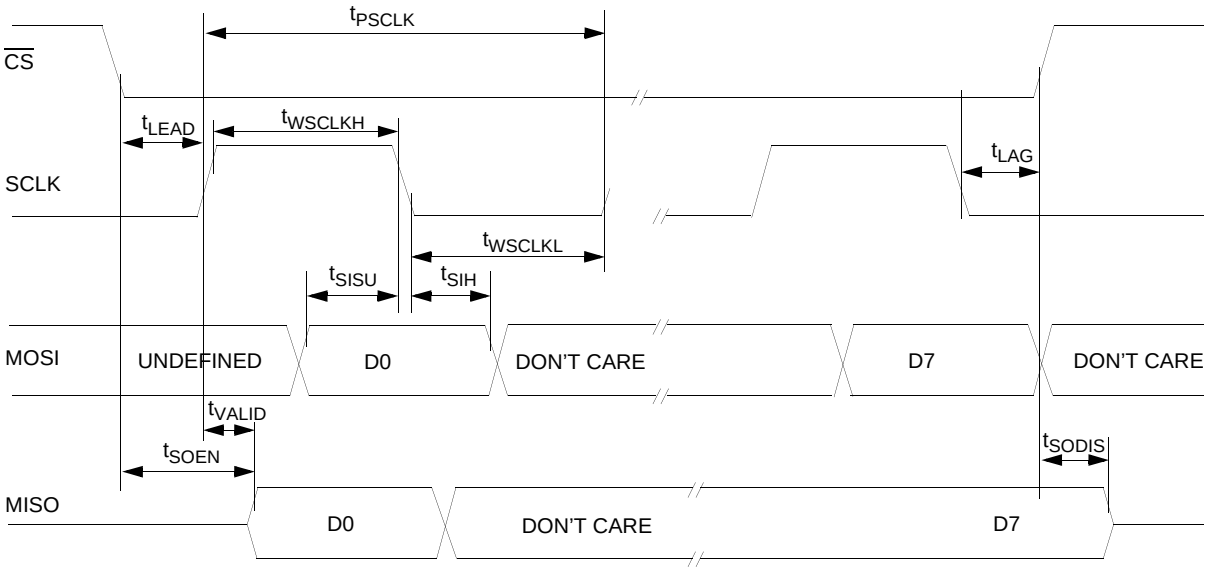


Figure 13. SPI Timing Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33910 is designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33910 is well suited to perform keypad applications via the LIN bus.

Two power switches are provided on the device configured as high side outputs. Other ports are also provided, which include a wake-up capable pin amd a Hall Sensor port supply. An internal voltage regulator provides power to a MCU device.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See Table 1, 33910 Simplified Application Diagram, page 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 3 for a description of the pin locations in the package.

RECEIVER OUTPUT (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD low when LIN bus is dominant, RXD high when LIN bus is recessive.

TRANSMITTER INPUT (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High).

This pin has an internal pull-up to force recessive state in case the input is left floating.

LIN BUS (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0.

The LIN interface is only active during Normal and Normal Request Modes.

SERIAL DATA CLOCK (SCLK)

The SCLK pin is the SPI clock input pin. MISO data changes on the negative transition of the SCLK. MOSI is sampled on the positive edge of the SCLK.

MASTER OUT SLAVE IN (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the positive edge of SCLK.

MASTER IN SLAVE OUT (MISO)

The MISO pin sends data to an SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the negative edge of the SCLK. When $\overline{CS}$ is High, this pin will remain in high-impedance state.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ is a active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{CS}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only.

While in STOP Mode a low-to-high level transition on this pin will generate a wake-up condition for the 33910.

ANALOG MULTIPLEXER (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the L1 input voltage and the internal junction temperature.

PWM INPUT CONTROL (PWMIN)

This digital input can control the high sides in Normal Request and Normal Mode.

To enable PWM control, the MCU must perform a write operation to the high side control register (HSCR).

This pin has an internal 20uA current pull-up.

RESET ($\overline{RST}$)

This bidirectional pin is used to reset the MCU in case the 33910 detects a reset condition or to inform the 33910 that the MCU has just been reset. After release of the $\overline{RST}$ pin Normal Request Mode is entered.

The $\overline{RST}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development without the risk of destroying the driver.

INTERRUPT ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request Mode or to signal a wake-up from Stop Mode. This active low output will transition to high, only after the interrupt is acknowledged by a SPI read of the respective status bits.

WATCHDOG CONFIGURATION (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog will be disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150ms typical).

GROUND CONNECTION (AGND, PGND, LGND)

The AGND, PGND and LGND pins are the Analog and Power ground pins.

The AGND pin is the ground reference of the voltage regulator.

The PGND and LGND pins are used for high current load return as in the LIN interface pin.

Note: PGND, AGND and LGND pins must be connected together.

DIGITAL/ANALOG (L1)

The L1 pin is a multi purpose input. It can be used as a digital input, which can be sampled by reading the SPI and used for wake-up when 33910 is in Low Power Mode or used as analog inputs for the analog multiplexer. When used to sense voltage outside the module, a 33kohm series resistor must be used on each input.

When used as a wake-up input L1 can be configured to operate in Cyclic-Sense Mode. In this mode, one of the high side switches is configured to be periodically turned on and sample the wake-up input. If a state change is detected between two cycles a wake-up is initiated. The 33910 can also wake-up from Stop or Sleep by a simple state change on L1.

When used as analog input, the voltage present on the L1 pins is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer.

Note: If L1 input is selected in the analog multiplexer, it will be disabled as digital input and remains disabled in low Power Mode. No wake-up feature is available in that condition.

When the L1 input is not selected in the analog multiplexer, the voltage divider is disconnected from that input.

HIGH SIDE OUTPUTS (HS1 AND HS2)

These high side switches are able to drive loads such as relays or lamps. Their structure is connected to the VS2 supply pin. The pins are short-circuit protected and also protected against overheating.

HS1and HS2 are controlled by SPI and can respond to a signal applied to the PWMIN input pin.

The HS1 and HS2 outputs can also be used during Low Power Mode for the cyclic-sense of the wake input.

POWER SUPPLY (VS1 AND VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages, with external components. These pins sustain standard automotive voltage conditions such as load dump at 40V.

The high side switches (HS1 and HS2) are supplied by the VS2 pin, all other internal blocks are supplied by VS1 pin.

VOLTAGE SENSE PIN (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage.

The ESD structure on this pin allows for excursion up to +40V and down to -27V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10kohm resistor in series with this pin for protection purposes.

HALL SENSOR SWITCHABLE SUPPLY PIN (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal Mode, this current limited output can be controlled through the SPI.

The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

+5V MAIN REGULATOR OUTPUT (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and over-temperature protected.

During Stop Mode the voltage regulator does not operate with its full drive capabilities and the output current is limited.

During Sleep Mode the regulator output is completely shut down.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

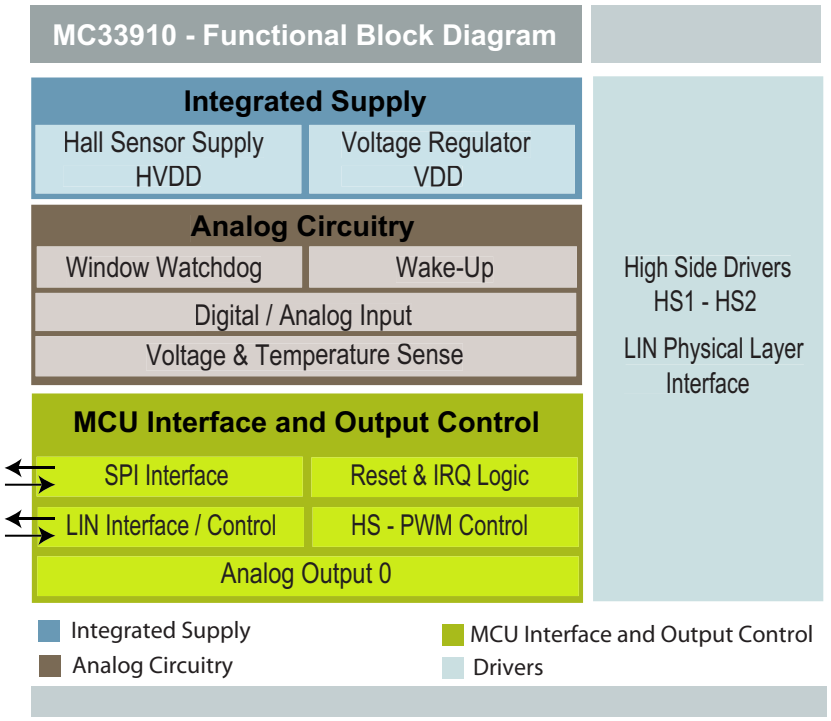


Figure 14. Functional Internal Block Diagram

ANALOG CIRCUITRY

The 33910 is designed to operate under automotive operating conditions. A fully configurable window watchdog circuit will reset the connected MCU in case of an overflow. Two low power modes are available with several different wake-up sources to reactivate the device. One analog / digital input can be sensed or used as the wake-up source. The device is capable of sensing the supply voltage (VSENSE) and the internal chip temperature (CTEMP).

HIGH SIDE DRIVERS

Two current and temperature protected High Side drivers with PWM capability are provided to drive small loads such as Status LED's or small lamps. Both Drivers can be configured for periodic sense during low power modes.

MCU INTERFACE

The 33910 is providing its control and status information through a standard 8-Bit SPI interface. Critical system events such as Low- or High-voltage/Temperature conditions as well as over-current conditions in any of the driver stages can be reported to the connected MCU via IRQ or RST. The High Side driver outputs can be controlled via the SPI register as well as the PWMIN input. The integrated LIN physical layer interface can be configured via SPI register and its communication is driven through the RXD and TXD device pins. All internal analog sources are multiplexed to the ADOUT0 pin.

VOLTAGE REGULATOR OUTPUTS

Two independent voltage regulators are implemented on the 33910. The VDD main regulator output is designed to supply a MCU with a precise 5V. The switchable HVDD output is dedicated to supply small peripherals as hall sensors.

LIN PHYSICAL LAYER INTERFACE

The 33910 provides a LIN 2.0 compatible LIN physical layer interface with selectable slew rate and various diagnostic features.

FUNCTIONAL DEVICE OPERATIONS

OPERATIONAL MODES

INTRODUCTION

The 33910 offers three main operating modes: Normal (Run), Stop, and Sleep (Low Power). In Normal Mode the device is active and is operating under normal application conditions. The Stop and Sleep Modes are low power modes with wake-up capabilities.

In Stop Mode the voltage regulator still supplies the MCU with V_{DD} (limited current capability) and in Sleep Mode the voltage regulator is turned off (V_{DD} = 0 V).

Wake-up from Stop Mode is initiated by a wake-up interrupt. Wake-up from Sleep Mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MOD1:2 bits in the mode control register (MCR).

Figure 15 describes how transitions are done between the different operating modes and Table 5, 25, gives an overview of the Operating Mode.

RESET MODE

The 33910 enters the Reset Mode after a power up. In this mode, the $\overline{RST}$ pin is low for 1ms (typical value). After this delay, the 33910 enters the Normal Request Mode and the $\overline{RST}$ pin is driven high.

The Reset Mode is entered if a reset condition occurs (V_{DD} low, watchdog trigger fail, after a wake-up from Sleep Mode, Normal Request Mode time-out occurs).

NORMAL REQUEST MODE

This is a temporary mode automatically accessed by the device after the Reset Mode or after a wake-up from Stop Mode.

In Normal Request Mode, the VDD regulator is ON, the Reset pin is high and the LIN is operating in Rx Only Mode.

As soon as the device enters the Normal Request Mode an internal timer is started for 150ms (typical value). During these 150ms, the MCU must configure the timing control register (TIMCR) and the MCR with MOD2 and MOD1 bits ste = 0 to enter in Normal Mode. If within the 150ms timeout the MCU does not command the 33910 to Normal Mode, it will enter in Reset Mode. If the WDCONF pin is grounded in order to disable the watchdog function, the 33910 goes directly in Normal Mode after the Reset Mode. If the WDCONF pin is open, the 33910 stays typically for 150ms in Normal Request before entering in Normal Mode.

NORMAL MODE

In Normal Mode, all 33910 functions are active and can be controlled by the SPI and the PWMIN pin.

The VDD regulator is ON and delivers its full current capability.

If an external resistor is connected between the WDCONF pin and the Ground, the window watchdog function will be enabled.

The wake-up input (L1) can be read as a digital input or have its voltage routed through the analog-multiplexer.

The LIN interface has slew rate and timing compatible with the LIN protocol specification 2.0. The LIN bus can transmit and receive information.

The high side switches are active and have PWM capability according to the SPI configuration.

The interrupts are generated to report failures 5 for V_{SUP} over/under-voltage, thermal shutdown or thermal shutdown prewarning on the main regulator.

SLEEP MODE

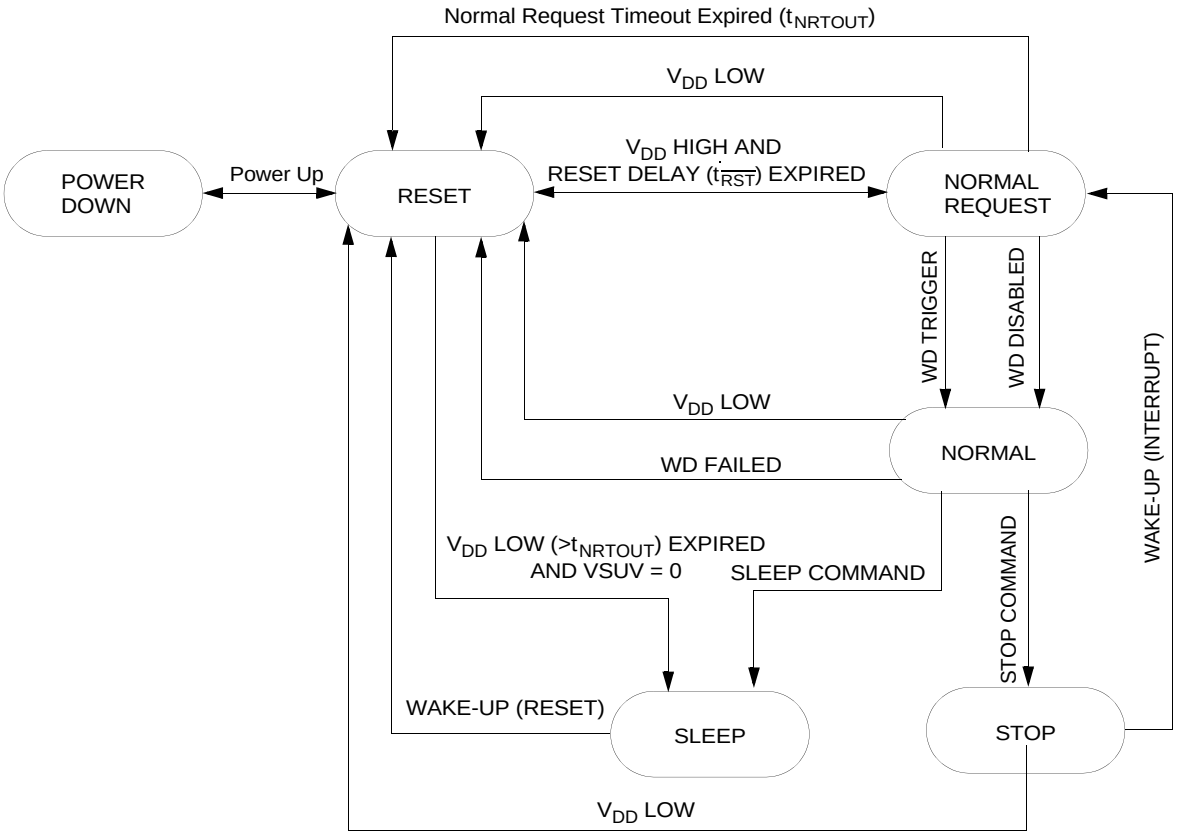
The Sleep Mode is a low power mode. From Normal Mode, the device enters the Sleep Mode by sending one SPI command through the MCR. All blocks are in their lowest power consumption condition. Only some wake-up sources (wake-up input with or without cyclic sense, forced wake-up and LIN receiver) are active. The 5V regulator is OFF. The internal low-power oscillator may be active if the IC is configured for cyclic-sense. In this condition, one of the high side switches is turned on periodically and the wake-up inputs are sampled.

Wake-up from Sleep Mode is similar to a power-up. The device goes in Reset Mode except that the SPI will report the wake-up source and the BATFAIL flag is not set.

STOP MODE

The Stop Mode is the second low power mode, but in this case the 5V regulator is ON with limited current drive capability. The application MCU is always supplied while the 33910 is operating in Stop Mode.

The device can enter in Stop Mode only by sending the SPI command. When the application is in this mode, it can wake-up from the 33910 side (for example: cyclic sense, force wake-up, LIN bus, wake inputs) or the MCU side ($\overline{CS}$, $\overline{RST}$ pins). Wake-up from Stop Mode will transition the 33910 to Normal Request Mode and generates an interrupt except if the wake-up event is a low to high transition on the $\overline{CS}$ pin or comes from the $\overline{RST}$ pin.



Legend
WD: Watchdog
WD Disabled: Watchdog disabled (WDCONF pin connected to GND)
WD Trigger: Watchdog is triggered by SPI command
WD Failed: No watchdog trigger or trigger occurs in closed window
Stop Command: Stop command sent via the SPI
Sleep Command: Sleep command sent via the SPI
Wake-up from Stop Mode: L1 state change, LIN bus wake-up, Periodic wake-up, $\overline{CS}$ rising edge wake-up or $\overline{RST}$ wake-up.
Wake-up from Sleep Mode: L1 state change, LIN bus wake-up, Periodic wake-up.

Figure 15. Operating Modes and Transitions

Table 5. Operating Modes Overview

Function	Reset Mode	Normal Request Mode	Normal Mode	Stop Mode	Sleep Mode
VDD	full	full	full	stop	-
HVDD	-	SPI(51)	SPI	-	-
HSx	-	SPI/PWM(52)	SPI/PWM	Note(53)	Note(54)
Analog Mux	-	SPI	SPI	-	-
L1	-	Input	Input	Wake-up	Wake-up
LIN	-	Rx-Only	full/Rx-Only	Rx-Only/Wake-up	Wake-up
Watchdog	-	150ms (typ.) timeout	On(55)/Off	-	-
VSENSE	On	On	On	VDD	-

Notes
51. Operation can be enabled/controlled by the SPI.
52. Operation can be controlled by the PWMIN input.
53. HSx switches can be configured for cyclic sense operation in Stop Mode.
54. HSx switches can be configured for cyclic sense operation in Sleep Mode.
55. Windowing operation when enabled by an external resistor.

INTERRUPTS

Interrupts are used to signal a microcontroller that a peripheral needs to be serviced. The interrupts which can be generated change according to the Operating Mode. While in Normal and Normal Request modes the 33910 signals through interrupts special conditions which may require a MCU software action. Interrupts are not generated until all pending wake-up sources are read in the interrupt source register (ISR).

While in Stop Mode, interrupts are used to signal wake-up events. Sleep Mode does not use interrupts, wake-up is performed by powering-up the MCU. In Normal and Normal Request Mode the wake-up source can be read by SPI.

The interrupts are signaled to the MCU by a low logic level of the $\overline{IRQ}$ pin, which will remain low until the interrupt is acknowledged by a SPI read. The $\overline{IRQ}$ pin will then be driven high.

Interrupts are only asserted while in Normal-, Normal Request and Stop Mode. Interrupts are not generated while the $\overline{RST}$ pin is low.

Following is a list of the interrupt sources in Normal and Normal Request Modes, some of those can be masked by writing to the SPI-interrupt mask register (IMR).

Low Voltage Interrupt

Signals when the supply line (VS1) voltage drops below the VSUV threshold (V_{SUV}).

High Voltage Interrupt

Signals when the supply line (VS1) voltage increases above the VSOV threshold (V_{SOV}).

Over-Temperature Prewarning

Signals when the 33910 temperature has reached the pre-shutdown warning threshold. It is used to warn the MCU that an over-temperature shutdown in the main 5V regulator is imminent.

LIN Over-Current Shutdown / Over-Temperature Shutdown / TXD Stuck At Dominant / RXD Short-Circuit

These signal faulty conditions in the LIN interface (except the LIN over-current) that had led to disable the LIN driver. In order to restart operation, the fault must be removed and must be acknowledged by reading the SPI.

The LINOC bit functionality in the LIN status register (LINSR) is to indicate that an LIN over-current occurred and the driver stays enabled.

High Side Over-Temperature Shutdown

Signals a shutdown of the high side outputs.

RESET

To reset an MCU, the 33910 drives the $\overline{RST}$ pin low for the time the reset condition lasts.

After the reset source has been removed the state machine will drive the $\overline{RST}$ output low for at least 1ms typical value before driving it high.

In the 33910 four main reset sources exist:

5V Regulator Low-Voltage-Reset ($V_{\overline{RSTTH}}$)

The 5V regulator output V_{DD} is continuously monitored against brown outs. If the supply monitor detects that the voltage at the VDD pin has dropped below the reset threshold $V_{\overline{RSTTH}}$ the 33910 will issue a reset. In case of over-

temperature, the voltage regulator will be disabled and the voltage monitoring will issue a VDDOT Flag independently of the V_{DD} voltage.

Window Watchdog Overflow

If the watchdog counter is not properly serviced while its window is open, the 33910 will detect a MCU software runaway and will reset the microcontroller.

Wake-up From Sleep Mode

During Sleep Mode, the 5V regulator is not active, hence all wake-up requests from Sleep Mode require a power-up/ reset sequence.

External Reset

The 33910 has a bidirectional reset pin which drives the device to a safe state (same as Reset Mode) for as long as this pin is held low. The $\overline{RST}$ pin must be held low long enough to pass the internal glitch filter and get recognized by the internal reset circuit. This functionality is also active in Stop Mode.

After the $\overline{RST}$ pin is released, there is no extra $t_{\overline{RST}}$ to be considered.

WAKE-UP CAPABILITIES

Once entered in to one of the low-power modes (Sleep or Stop) only wake-up sources can bring the device into Normal Mode operation.

In Stop Mode, a wake-up is signaled to the MCU as an interrupt, while in Sleep Mode the wake-up is performed by activating the 5V regulator and resetting the MCU. In both cases the MCU can detect the wake-up source by accessing the SPI registers. There is no specific SPI register bit to signal a $\overline{CS}$ wake-up or external reset. If necessary this condition is detected by excluding all other possible wake-up sources.

Wake-up From Wake-up Input (L1) With Cyclic Sense Disabled

The wake-up line is dedicated to sense state changes of external switches and wake-up the MCU (in Sleep or Stop Mode).

In order to select and activate direct wake-up from the L1 input, the wake-up control register (WUCR) must be configured with L1WE input enabled. The wake-up input state is read through the wake-up status register (WUSR).

L1 input is also used to perform cyclic-sense wake-up.

Note: Selecting the L1 input in the analog multiplexer before entering Low Power Mode will disable the wake-up capability of the L1 input.

Wake-up From Wake-up Input (L1) With Cyclic Sense Timer Enabled

The SBCLIN can wake-up at the end of a cyclic sense period if on the wake-up input lines (L1) a state change occurs. The HSx switch is activated in Sleep or Stop Modes from an internal timer. Cyclic sense and force wake-up are exclusive. If cyclic sense is enabled, the force wake-up can not be enabled.

In order to select and activate the cyclic sense wake-up from the L1 input, before entering in low power modes (Stop or Sleep Modes), the following SPI set-up has to be performed:

- In WUCR: select the L1 input to WU-enable.
- In HSCR: enable HSx.
- In TIMCR: select the CS/$\overline{WD}$ bit and determine the cyclic sense period with CYSTx bits.
- Perform Goto Sleep/Stop command.

Forced Wake-up

The 33910 can wake-up automatically after a predetermined time spent in Sleep or Stop Mode. Cyclic sense and forced wake-up are exclusive. If forced wake-up is enabled, the cyclic sense can not be enabled.

To determine the wake-up period, the following SPI set-up has to be sent before entering in Low Power Modes:

- In TIMCR: select the CS/$\overline{WD}$ bit and determine the Low Power Mode period with CYSTx bits.
- In HSCR: the HSx bit must be disabled.

$\overline{CS}$ Wake-up

While in Stop Mode, a rising edge on the $\overline{CS}$ will cause a wake-up. The $\overline{CS}$ wake-up does not generate an interrupt and is not reported on SPI.

LIN Wake-up

While in the low power modes the 33910 monitors the activity on the LIN bus. A dominant pulse larger than t_{PROPWL} followed by a dominant to recessive transition will cause a LIN wake-up. This behavior protects the system from a short-to-ground bus condition.

$\overline{RST}$ Wake-up

While in Stop Mode, the 33910 can wake-up when the $\overline{RST}$ pin is held low long enough to pass the internal glitch filter. Then, the 33910 will change to Normal Request or Normal modes depending on the WDCONF pin configuration. The $\overline{RST}$ wake-up does not generate an interrupt and is not reported via SPI.

From Stop Mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- $\overline{CS}$ wake-up
- LIN wake-up
- $\overline{RST}$ wake-up

From Sleep Mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense

- Cyclic sense wake-up inputs
- Force wake-up
- LIN wake-up

WINDOW WATCHDOG

The 33910 includes a configurable window watchdog which is active in Normal Mode. The watchdog can be configured by an external resistor connected to the WDCONF pin. The resistor is used to achieve higher precision in the timebase used for the watchdog.

SPI clears are performed by writing through the SPI in the MOD bits of the MCR.

During the first half of the SPI timeout watchdog clears are not allowed; but after the first half of the PSPI-timeout window the clear operation opens. If a clear operation is performed outside the window, the 33910 will reset the MCU, in the same way as when the watchdog overflows.

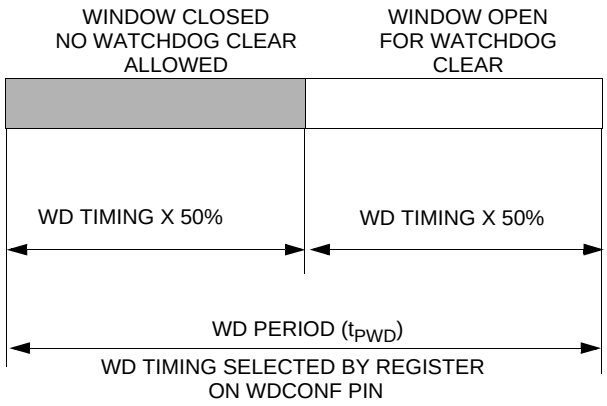


Figure 16. Window Watchdog Operation

To disable the watchdog function in Normal Mode the user must connect the WDCONF pin to ground. This measure effectively disables Normal Request Mode. The WDOFF bit in the WDSR will be set. This condition is only detected during Reset Mode.

If neither a resistor nor a connection to ground is detected, the watchdog falls back to the internal lower precision timebase of 150ms (typ.) and signals the faulty condition through the WDSR.

The watchdog timebase can be further divided by a prescaler which can be configured by the TIMCR. During Normal Request Mode, the window watchdog is not active but there is a 150ms (typ.) timeout for leaving the Normal Request Mode. In case of a timeout, the 33910 will enter into Reset Mode, resetting the microcontroller before entering again into Normal Request Mode.

HIGH SIDE OUTPUT PINS HS1 AND HS2

These outputs are two high side drivers intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Over-temperature shutdown (with maskable interrupt)
- High-voltage shutdown (software maskable)
- Cyclic sense

The high side switches are controlled by the bits HS1:2 in the High Side Control Register (HSCR).

PWM Capability (direct access)

Each high side driver offers additional (to the SPI control) direct control via the PWMIN pin.

If both the bits HS1 and PWMHS1 are set in the High Side Control Register (HSCR), then the HS1 driver is turned on if the PWMIN pin is high and turned of if the PWMIN pin is low. This applies to HS2 configuring HS2 and PWMHS2 bits.

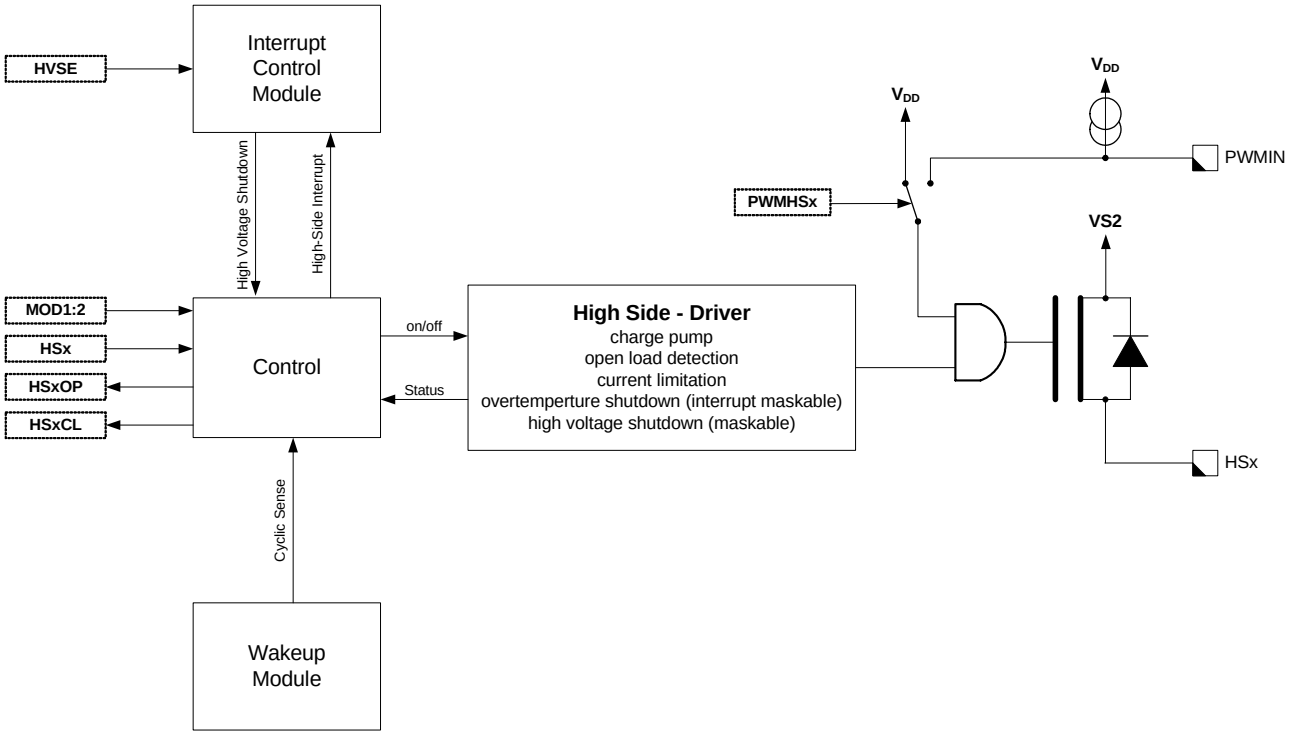


Figure 17. High Side Drivers HS1 and HS2

Open Load Detection

Each high side driver signals an open load condition if the current through the high side is below the open load current threshold.

The open load condition is indicated with the bits HS1OP and HS2OP in the High Side Status Register (HSSR).

Current Limitation

Each high side driver has an output current limitation. In combination with the over-temperature shutdown the high-side drivers are protected against over-current and short-circuit failures.

When the driver operates in the current limitation area, it is indicated with the bits HS1CL and HS2CL in the HSSR.

Note: If the driver is operating in current limitation mode, excessive power might be dissipated.

Over-temperature Protection (HS Interrupt)

Both high side drivers are protected against over-temperature. In case of an over-temperature condition both high side drivers are shut down and the event is latched in the Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source Register (ISR).

A thermal shutdown of the high side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

If the bit HSM is set in the Interrupt Mask Register (IMR), then an interrupt ($\overline{IRQ}$) is generated.

A write to the High Side Control Register (HSCR), when the over-temperature condition is gone, will re-enable the high side drivers.

High-voltage Shutdown

In case of a high voltage condition and if the high voltage shutdown is enabled (bit HVSE in the Mode Control Register (MCR) is set) both high side drivers are shut down.

A write to the High Side Control Register (HSCR), when the high voltage condition is gone, will re-enable the high side drivers.

Sleep And Stop Mode

The high side driver can be enabled to operate in Sleep and Stop Mode for cyclic sensing. Also see Table 5, Operating Modes Overview.

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification and has the following features:

- LIN physical layer 2.0 compliant
- Slew rate selection
- Over-current shutdown
- Over-temperature shutdown
- LIN pull-up disable in Stop and Sleep Modes
- Advanced diagnostics
- LIN dominant voltage level selection

The LIN driver is a low side MOSFET with over-current and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a Slave Mode. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

LIN Pin

The LIN pin offers a high susceptibility immunity level from external disturbance, guaranteeing communication.

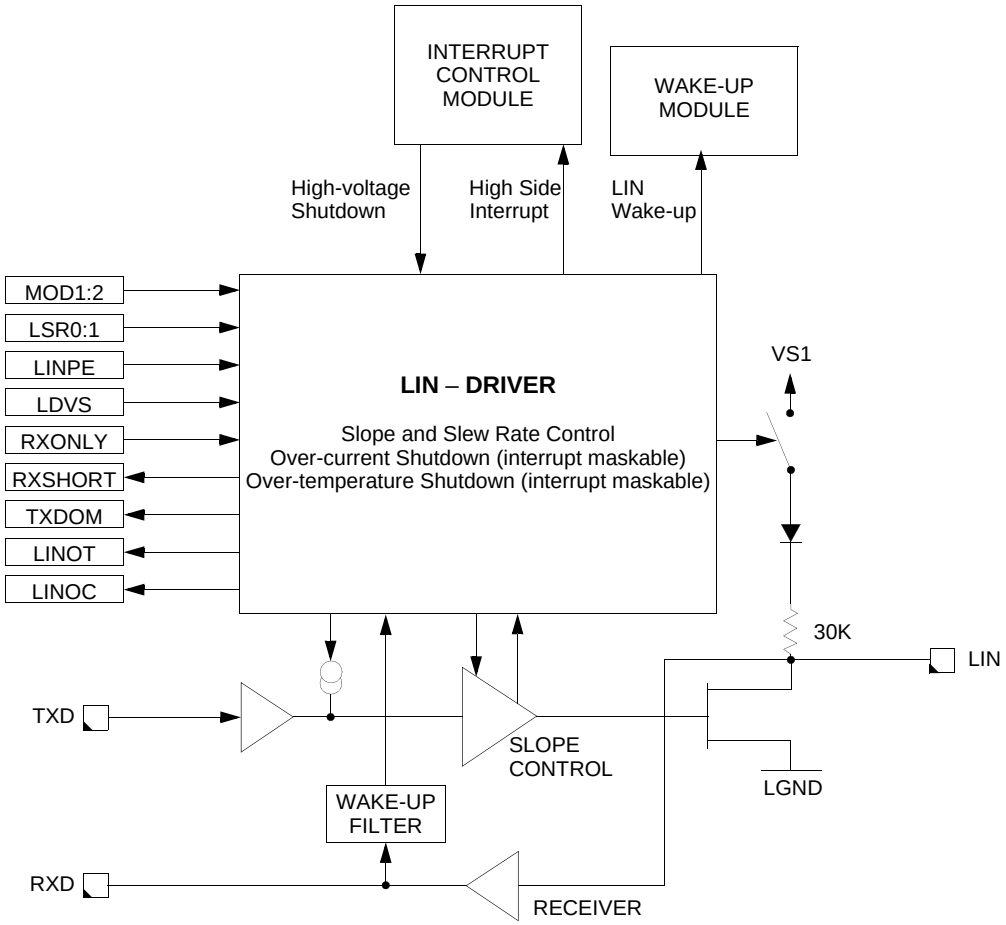


Figure 18. LIN Interface

Slew Rate Selection

The slew rate can be selected for optimized operation at 10.4 and 20kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LSR1:0 in the LIN control register (LINCR). The initial slew rate is optimized for 20kBit/s.

LIN Pull-up Disable In Stop and Sleep Mode

To improve performance and for safe behavior in case of LIN bus short to ground or LIN bus leakage during Low Power Mode the internal pull-up resistor on the LIN pin can be disconnected by clearing the LINPE bit in the MCR. The bit LINPE also changes the bus wake-up threshold (V_{BUSWU}).

In case of a LIN bus short to GND, this feature will reduce the current consumption in Stop and Sleep modes.

Over-Current Shutdown (LIN Interrupt)

The output low side FET is protected against over-current conditions. In case of an over-current condition (e.g. LIN bus

short to V_{BAT}), the transmitter will not be shut down. The bit LINOC in the LIN status register (LINSR) is set.

If the bit LINM is set in the interrupt mask register (IMR) an Interrupt $\overline{IRQ}$ will be generated.

Over-Temperature Shutdown (LIN Interrupt)

The output low side FET is protected against over-temperature conditions. In case of an over-temperature condition, the transmitter will be shut down and the bit LINOT in the LIN status register (LINSR) is set.

If the bit LINM is set in the interrupt mask register (IMR) an Interrupt $\overline{IRQ}$ will be generated.

The transmitter is automatically re-enabled once the condition is gone and TXD is high.

A read of the LIN status register (LINSR) with the TXD pin will re-enable the transmitter.

RXD Short Circuit Detection (LIN Interrupt)

The LIN transceiver has a short-circuit detection for the RXD output pin. In case of an short-circuit condition, either 5V or ground, the bit RXSHORT in the LIN status register (LINSR) is set and the transmitter is shutdown.

If the bit LINM is set in the interrupt mask register (IMR) an interrupt $\overline{IRQ}$ will be generated.

The transmitter is automatically re-enabled once the condition is gone (transition on RXD) and TXD is high.

A read of the LIN status register (LINSR) without the RXD pin short circuit condition will clear the bit RXSHORT.

TXD Dominant Detection (LIN Interrupt)

The LIN transceiver monitors the TXD input pin to detect stuck in dominant (0V) condition. In case of a stuck condition (TXD pin 0V for more than 1 second (typ.)) the transmitter is shut down and the bit TXDOM in the LIN status register (LINSR) is set.

If the bit LINM is set in the interrupt mask register (IMR) an interrupt $\overline{IRQ}$ will be generated.

The transmitter is automatically re-enabled once TXD is high.

A read of the LIN status register (LINSR) with the TXD pin is high will clear the bit TXDOM.

LIN Dominant Voltage Level Selection

The LIN dominant voltage level can be selected by the bit LDVS in the LIN control register (LINCR).

LIN Receiver Operation Only

While in Normal Mode the activation of the RXONLY bit disables the LIN TX driver. In the case of a LIN error condition this bit is automatically set. In case a Low Power Mode is selected with this bit set, the LIN wake-up functionality is disabled, then, in Stop Mode, the RXD pin will reflect the state of the LIN bus.

STOP Mode And Wake-up Feature

During Stop Mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop Mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in the recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by a rising edge will generate a wake-up interrupt and will be reported in the ISR. Also see Figure 11, page 19.

SLEEP Mode And Wake-up Feature

During Sleep Mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep Mode sequence the internal pull-up resistor is disconnected from V_{SUP} and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by a rising edge will generate a system wake-up (Reset) and will be reported in the ISR. Also see Figure 10, page 18.

LOGIC COMMANDS AND REGISTERS

SPI AND CONFIGURATION

The SPI creates the communication link between a microcontroller (master) and the 33910.

The interface consists of four pins (see Figure 19):

- $\overline{CS}$—Chip Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SCLK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 4 bits of address (A3:A0) + 4 bits of control information (C3:C0) and the slave replies with 3 system status bits and one not defined bit (VMS,LINS,HSS,n.d.) + 4 bits of status information (S3:S0).

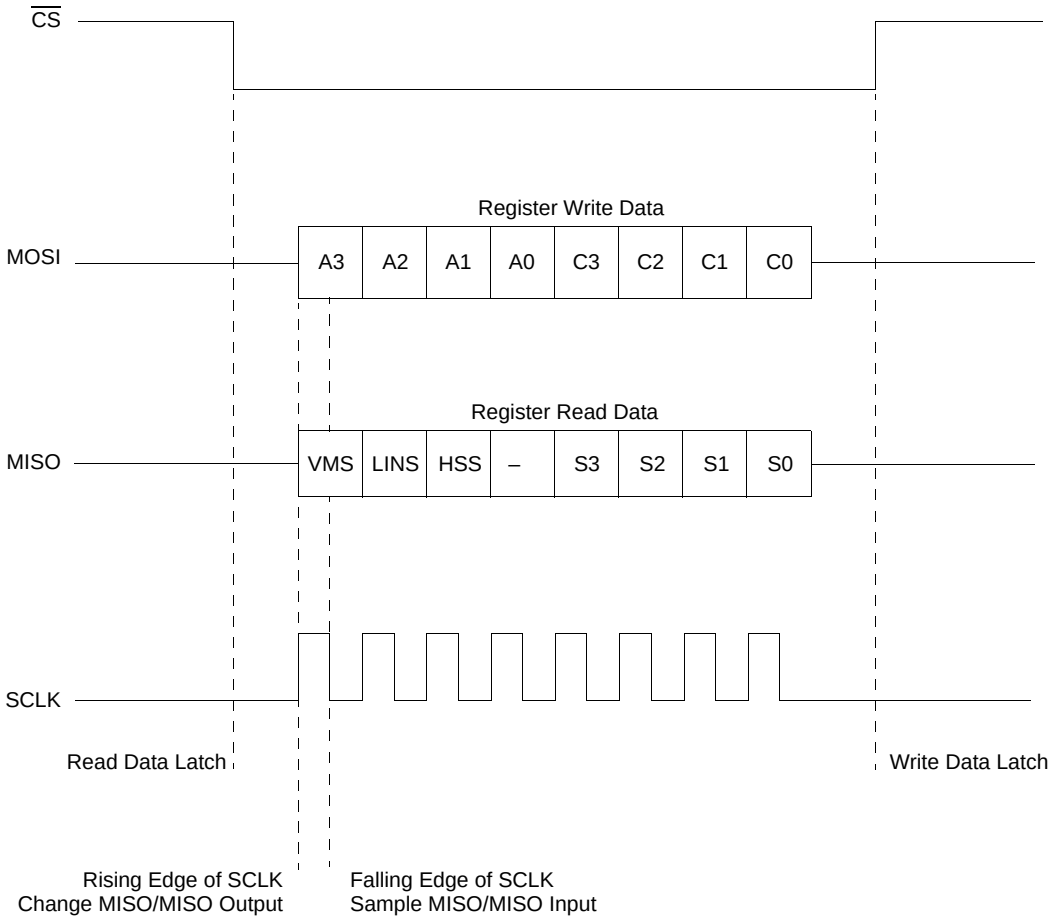


Figure 19. SPI Protocol

During the inactive phase of the $\overline{CS}$ (HIGH), the new data transfer is prepared.

The falling edge of the $\overline{CS}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data).

With the rising edge of the SPI clock (SCLK), the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock (SCLK) the data is sampled by the receiver.

The data transfer is only valid if exactly 8 sample clock edges are present during the active (low) phase of $\overline{CS}$.

The rising edge of the chip select $\overline{CS}$ indicates the end of the transfer and latches the write data (MOSI) into the register. The $\overline{CS}$ high forces MISO to the high-impedance state.

Register reset values are described along with the reset condition. Reset condition is the condition causing the bit to be set to its reset value. The main reset conditions are:

- Power-On Reset (POR): level at which the logic is reset and BATFAIL flag sets.

- Reset Mode

- Reset done by the $\overline{RST}$ pin (ext_reset)

SPI REGISTER OVERVIEW

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Table 6. System Status Register

Adress(A3:A0)	Register Name / Read/Write Information		BIT			
			7	6	5	4
$0 - $F	SYSSR - System Status Register	R	VMS	LINS	HSS	-

Table 7 summarizes the SPI Register content for Control Information (C3:C0)=W and status information (S3:S0) = R.

Table 7. SPI Register Overview

Adress(A3:A0)	Register Name / Read/Write Information		BIT			
			3	2	1	0
$0	MCR - Mode Control Register	W	HVSE	LINPE	MOD2	MOD1
	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$1	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$2	WUCR - Wake-up Control Register	W	-	-	-	L1WE
	WUSR - Wake-up Status Register	R	-	-	-	L1
$3	WUSR - Wake-up Status Register	R	-	-	-	L1
$4	LINCR - LIN Control Register	W	LDVS	RXONLY	LSR1	LSR0
	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	LINOC
$5	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	LINOC
$6	HSCR - High Side Control Register	W	PWMHS2	PWMHS1	HS2	HS1
	HSSR - High Side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$7	HSSR - High Side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$A	TIMCR - Timing Control Register	W	CS/$\overline{WD}$	WD2	WD1	WD0
				CYST2	CYST1	CYST0
	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$B	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$C	AMUXCR - Analog Multiplexer Control Register	W	L1DS	MX2	MX1	MX0
$D	CFR - Configuration Register	W	HVDD	CYSX8	-	-
$E	IMR - Interrupt Mask Register	W	HSM	-	LINM	VMM
	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0
$F	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0

Note: Address $8 and $9 are reserved and must not be used.

REGISTER DEFINITIONS

System Status Register - SYSSR

The system status register (SYSSR) is always transferred with every SPI transmission and gives a quick system status overview. It summarizes the status of the voltage status register (VSR), LIN status register (LINSR) and the HSSR.

Table 8. System Status Register

	S7	S6	S5	S4
Read	VMS	LINS	HSS	–.

VMS - Voltage Monitor Status

This read-only bit indicates that one or more bits in the voltage status register (VSR) are set.

1 = Voltage Monitor bit set

0 = None

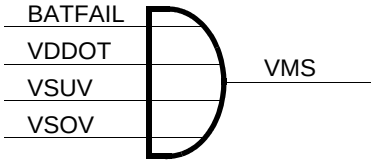


Figure 20. Voltage Monitor Status

LINS - LIN Status

This read-only bit indicates that one or more bits in the LIN status register (LINSR) are set.

1 = LIN Status bit set

0 = None

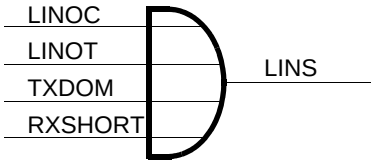


Figure 21. LIN Status

HSS - High Side Switch Status

This read-only bit indicates that one or more bits in the HSSR are set.

1 = High Side Status bit set

0 = None

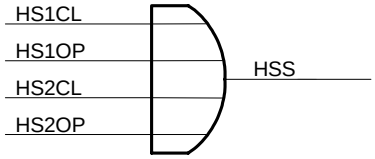


Figure 22. High Side Status

Mode Control Register - MCR

The MCR allows to switch between the operation modes and to configure the 33910. Writing the MCR will return the voltage status register (VSR).

Table 9. Mode Control Register - $0

	C3	C2	C1	C0
Write	HVSE	LINPE	MOD2	MOD1
Reset Value	1	1	-	-
Reset Condition	POR	POR	-	-

HVSE - High-Voltage Shutdown Enable

This write-only bit enables/disables automatic shutdown of the high side and the low side drivers during a high-voltage VSOV condition.

1 = automatic shutdown enabled

0 = automatic shutdown disabled

LINPE - LIN pull-up enable.

This write-only bit enables/disables the 30kΩ LIN pull-up resistor in Stop and Sleep modes. This bit also controls the LIN bus wake-up threshold.

1 = LIN pull-up resistor enabled

0 = LIN pull-up resistor disabled

MOD2, MOD1 - Mode Control Bits

These write-only bits select the Operating Mode and allow to clear the watchdog in accordance with Table 11 Mode Control Bits.

Table 10. Mode Control Bits

MOD2	MOD1	Description
0	0	Normal Mode
0	1	Stop Mode
1	0	Sleep Mode
1	1	Normal Mode + watchdog Clear

Voltage Status Register - VSR

Returns the status of the several voltage monitors. This register is also returned when writing to the MCR.

Table 11. Voltage Status Register - $0/$1

	S3	S2	S1	S0
Read	VSOV	VSUV	VDDOT	BATFAIL

VSOV - V_{SUP} Over-voltage

This read-only bit indicates an over-voltage condition on the VS1 pin.

1 = Over-voltage condition.

0 = Normal condition.

VSUV - V_{SUP} Under-voltage

This read-only bit indicates an under-voltage condition on the VS1 pin.

1 = Under-voltage condition.

0 = Normal condition.

VDDOT - Main Voltage Regulator Over-temperature Warning

This read-only bit indicates that the main voltage regulator temperature reached the Over-Temperature Prewarning Threshold.

1 = Over-temperature prewarning

0 = Normal

BATFAIL - Battery Fail Flag.

This read-only bit is set during power-up and indicates that the 33910 had a power on reset (POR).

Any access to the MCR or voltage status register (VSR) will clear the BATFAIL flag.

1 = POR Reset has occurred

0 = POR Reset has not occurred

Wake-up Control Register - WUCR

This register is used to control the digital wake-up input. Writing the wake-up control register (WUCR) will return the wake-up status register (WUSR).

Table 12. Wake-up Control Register - $2

	C3	C2	C1	C0
Write	0	0	0	L1WE
Reset Value	1	1	1	1
Reset Condition	POR, Reset Mode or ext_reset			

L1WE - Wake-up Input Enable

This write-only bit enables/disables the L1 input. In Stop and Sleep Mode the L1WE bit activates the L1 input for wake-up. If the L1 input is selected on the analog multiplexer, the L1WE is masked to 0.

1 = Wake-up Input enabled.

0 = Wake-up Input disabled.

Wake-up Status Register - WUSR

This register is used to monitor the digital wake-up inputs and is also returned when writing to the wake-up control register (WUCR).

Table 13. Wake-up Status Register - $2/$3

	S3	S2	S1	S0
Read	-	-	-	L1

L1 - Wake-up input

This read-only bit indicates the status of the L1 input. If the L1 input is not enabled then the wake-up status will return 0.

After a wake-up form Stop or Sleep Mode this bit also allows to verify the L1 input has caused the wake-up, by first reading the interrupt status register (ISR) and then reading the wake-up status register (WUSR).

1 = L1 Wake-up.

0 = L1 Wake-up disabled or selected as analog input.

LIN Control Register - LINCR

This register controls the LIN physical interface block. Writing the LIN control register (LINCR) returns the LIN status register (LINSR).

Table 14. LIN Control Register - $4

	C3	C2	C1	C0
Write	LDVS	RXONLY	LSR1	LSR0
Reset Value	0	0	0	0
Reset Condition	POR, Reset Mode or ext_reset	POR, Reset Mode, ext_reset or LIN failure gone*	POR	

* LIN failure gone: if LIN failure (overtemp, TXD/RXD short) was set, the flag resets automatically when the failure is gone.

LDVS - LIN Dominant Voltage Select

This write-only bit controls the LIN Dominant voltage:

1 = LIN Dominant Voltage = $V_{LIN\_DOM\_1}$ (1.7V typ)

0 = LIN Dominant Voltage = $V_{LIN\_DOM\_0}$ (1.1V typ)

RXONLY - LIN Receiver Operation Only

This write-only bit controls the behavior of the LIN transmitter.

In Normal Mode the activation of the RXONLY bit disables the LIN transmitter. In case of a LIN error condition this bit is automatically set.

In Stop Mode this bit disables the LIN wake-up functionality and the RXD pin will reflect the state of the LIN bus.

1 = only LIN receiver active (Normal Mode) or LIN wake-up disabled (Stop Mode).

0 = LIN fully enabled.

LSRx - LIN Slew-Rate

This write-only bit controls the LIN driver slew-rate in accordance with Table 15.

Table 15. LIN Slew-Rate Control

LSR1	LSR0	Description
0	0	Normal Slew Rate (up to 20kb/s)
0	1	Slow Slew Rate (up to 10kb/s)
1	0	Fast Slew Rate (up to 100kb/s)
1	1	Reserved

LIN Status Register - LINSR

This register returns the status of the LIN physical interface block and is also returned when writing to the LIN control register (LINCR).

Table 16. LIN Status Register - $4/$5

	S3	S2	S1	S0
Read	RXSHORT	TXDOM	LINOT	LINOC

RXSHORT - RXD Pin Short Circuit

This read-only bit indicates a short-circuit condition on the RXD pin (shorted either to 5.0V or to Ground). The short circuit delay must be 8µs worst case to be detected and to shutdown the driver. To clear this bit, it must be read after the condition is gone (transition detected on RXD pin). The LIN driver is automatically re-enabled once the condition is gone.

1 = RXD short circuit condition.

0 = None.

TXDOM - TXD Permanent Dominant

This read-only bit signals the detection of a TXD pin stuck at dominant (Ground) condition and the resultant shutdown in the LIN transmitter. This condition is detected after the TXD pin remains in dominant state for more than 1 second typical value.

To clear this bit, it must be read after TXD has gone high. The LIN driver is automatically re-enabled once TXD goes High.

1 = TXD stuck at dominant fault detected.

0 = None.

LINOT - LIN Driver Over-temperature Shutdown

This read-only bit signals that the LIN transceiver was shutdown due to over-temperature. The transmitter is automatically re-enabled after the over-temperature condition is gone and TXD is high. The LINOT bit is cleared after SPI read once the condition is gone.

1 = LIN over-temperature shutdown

0 = None

LINOC - LIN Driver Over-Current Shutdown

This read-only bit signals an over-current condition occurred on the LIN pin. The LIN driver is not shutdown but an $\overline{IRQ}$ is generated. To clear this bit, it must be read after the condition is gone.

1 = LIN over-current shutdown

0 = None

High Side Control Register - HSCR

This register controls the operation of the high side drivers. Writing to this register returns the High Side Status Register (HSSR).

Table 17. High Side Control Register - $6

	C3	C2	C1	C0
Write	PWMHS2	PWMHS1	HS2	HS1
Reset Value	0	0	0	0
Reset Condition	POR		POR, Reset Mode, ext_reset, HSx over-temp or (VSOV & HVSE)	

PWMHSx - PWM Input Control Enable

This write-only bit enables/disables the PWMIN input pin to control the high side switch. The high side switch must be enabled (HSx bit).

1 = PWMIN input controls HS1 output.

0 = HSx is controlled only by SPI.

HSx - High Side Switch Control.

This write-only bit enables/disables the high side switch.

1 = HSx switch on.

0 = HSx switch off.

High Side Status Register - HSSR

This register returns the status of the high side switch and is also returned when writing to the HSCR.

Table 18. High Side Status Register - $6/$7

	S3	S2	S1	S0
Read	HS2OP	HS2CL	HS1OP	HS1CL

High Side thermal shutdown

A thermal shutdown of the high side drivers is indicated by setting the HSxOP and HSxCL bits simultaneously.

HSxOP - High Side Switch Open-Load Detection

This read-only bit signals that the high side switch is conducting current below a certain threshold indicating possible load disconnection.

1 = HSx Open Load detected (or thermal shutdown)

0 = Normal

HSxCL - High Side Current Limitation

This read-only bit indicates that the high side switch is operating in current Limitation Mode.

1 = HSx in current limitation (or thermal shutdown)

0 = Normal

Timing Control Register - TIMCR

This register is a double purpose register which allows to configure the watchdog and the cyclic sense periods. Writing to the TIMCR will also return the WDSR.

Table 19. Timing Control Register - $A

	C3	C2	C1	C0
Write	CS/$\overline{WD}$	WD2	WD1	WD0
		CYST2	CYST1	CYST0
Reset Value	-	0	0	0
Reset Condition	-	POR		

CS/$\overline{WD}$ - Cyclic Sense or Watchdog Prescaler Select.

This write-only bit selects which prescaler is being written to, the cyclic sense prescaler or the watchdog prescaler.

1 = Cyclic Sense Prescaler selected

0 = Watchdog Prescaler select

WDx - Watchdog Prescaler

This write-only bits selects the divider for the watchdog prescaler and therefore selects the watchdog period in accordance with Table 20. This configuration is valid only if windowing watchdog is active.

Table 20. Watchdog Prescaler

WD2	WD1	WD0	Prescaler Divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

CYSTx - Cyclic Sense Period Prescaler Select

This write-only bits selects the interval for the wake-up cyclic sensing together with the bit CYSX8 in the configuration register (CFR) (see page 38).

This option is only active if the high side switch is enabled when entering in Stop or Sleep Mode. Otherwise a timed wake-up is performed after the period shown in Table 21.

Table 21. Cyclic Sense Interval

CYSX8[56]	CYST2	CYST1	CYST0	Interval
X	0	0	0	No Cyclic Sense
0	0	0	1	20ms
0	0	1	0	40ms
0	0	1	1	60ms
0	1	0	0	80ms
0	1	0	1	100ms
0	1	1	0	120ms
0	1	1	1	140ms
1	0	0	1	160ms
1	0	1	0	320ms
1	0	1	1	480ms
1	1	0	0	640ms
1	1	0	1	800ms
1	1	1	0	960ms
1	1	1	1	1120ms

Notes
56. bit CYSX8 is located in configuration register (CFR)

Watchdog Status Register

This register returns the watchdog status information and is also returned when writing to the TIMCR.

Table 22. Watchdog Status Register - $A/$B

	S3	S2	S1	S0
Read	WDTO	WDERR	WDOFF	WDWO

WDTO - Watchdog Time Out

This read-only bit signals the last reset was caused by either a watchdog timeout or by an attempt to clear the watchdog within the window closed.

Any access to this register or the TIMCR will clear the WDTO bit.

1 = Last reset caused by watchdog timeout

0 = None

WDERR - Watchdog Error

This read-only bit signals the detection of a missing watchdog resistor. In this condition the watchdog is using the internal, lower precision timebase. The windowing function is disabled.

1 = WDCONF pin resistor missing

0 = WDCONF pin resistor not floating

WDOFF - Watchdog Off

This read-only bit signals that the watchdog pin connected to GND and therefore disabled. In this case watchdog timeouts are disabled and the device automatically enters Normal Mode out of Reset. This might be necessary for software debugging and for programming the Flash memory.

1 = Watchdog is disabled

0 = Watchdog is enabled

WDWO - Watchdog Window Open

This read-only bit signals when the watchdog window is open for clears. The purpose of this bit is for testing. Should be ignored in case WDERR is High.

1 = Watchdog window open

0 = Watchdog window closed

Analog Multiplexer Control Register - MUXCR

This register controls the analog multiplexer and selects the divider ration for the L1 input divider.

Table 23. Analog Multiplexer Control Register -$C

	C3	C2	C1	C0
Write	L1DS	MX2	MX1	MX0
Reset Value	1	0	0	0
Reset Condition	POR	POR, Reset Mode or ext_reset		

L1DS - L1 Analog Input Divider Select

This write-only bit selects the resistor divider for the L1 analog input. Voltage is internally clamped to VDD.

0 = L1 Analog divider: 1

1 = L1 Analog divider: 3.6 (typ.)

MXx - Analog Multiplexer Input Select

These write-only bits selects which analog input is multiplexed to the ADOUT0 pin according to Table 24.

When disabled or when in Stop or Sleep Mode, the output buffer is not powered and the ADOUT0 output is left floating to achieve lower current consumption.

Table 24. Analog Multiplexer Channel Select

MX2	MX1	MX0	Meaning
0	0	0	Disabled
0	0	1	Reserved
0	1	0	Die Temperature Sensor
0	1	1	VSENSE input
1	0	0	L1 input
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Configuration Register - CFR

This register controls the cyclic sense timing multiplier.

Table 25. Configuration Register - $D

	C3	C2	C1	C0
Write	0	CYSX8	0	0
Reset Value	0	0	0	0
Reset Condition	POR, Reset Mode or ext_reset	POR	POR	POR

HVDD - Hall Sensor Supply Enable

This write-only bit enables/disables the state of the hall sensor supply.

1 = HVDD on

0 = HVDD off

CYSX8 - Cyclic Sense Timing x 8

This write-only bit influences the Cyclic Sense period as shown in Table 21.

1 = Multiplier enabled

0 = None

Interrupt Mask Register - IMR

This register allow to mask some of interrupt sources. The respective flags within the ISR will continue to work but will not generate interrupts to the MCU. The 5V Regulator over-temperature prewarning interrupt and under-voltage (VSUV) interrupts can not be masked and will always cause an interrupt.

Writing to the interrupt mask register (IMR) will return the ISR.

Table 26. Interrupt Mask Register - $E

	C3	C2	C1	C0
Write	HSM	-.	LINM	VMM
Reset Value	1	1	1	1
Reset Condition	POR			

HSM - High Side Interrupt Mask

This write-only bit enables/disables interrupts generated in the high side block.

1 = HS Interrupts Enabled

0 = HS Interrupts Disabled

LINM - LIN Interrupts Mask

This write-only bit enables/disables interrupts generated in the LIN block.

1 = LIN Interrupts Enabled

0 = LIN Interrupts Disabled

VMM - Voltage Monitor Interrupt Mask

This write-only bit enables/disables interrupts generated in the voltage monitor block. The only maskable interrupt in the voltage monitor block is the V_{SUP} over-voltage interrupt.

1 = Interrupts Enabled

0 = Interrupts Disabled

Interrupt Source Register - ISR

This register allows the MCU to determine the source of the last interrupt or wake-up respectively. A read of the register acknowledges the interrupt and leads $\overline{IRQ}$ pin to high, in case there are no other pending interrupts. If there are pending interrupts, $\overline{IRQ}$ will be driven high for 10µs and then be driven low again.

This register is also returned when writing to the interrupt mask register (IMR).

Table 27. Interrupt Source Register - $E/$F

	S3	S2	S1	S0
Read	ISR3	ISR2	ISR1	ISR0

ISRx - Interrupt Source Register

These read-only bits indicate the interrupt source following Table 28. If no interrupt is pending than all bits are 0.

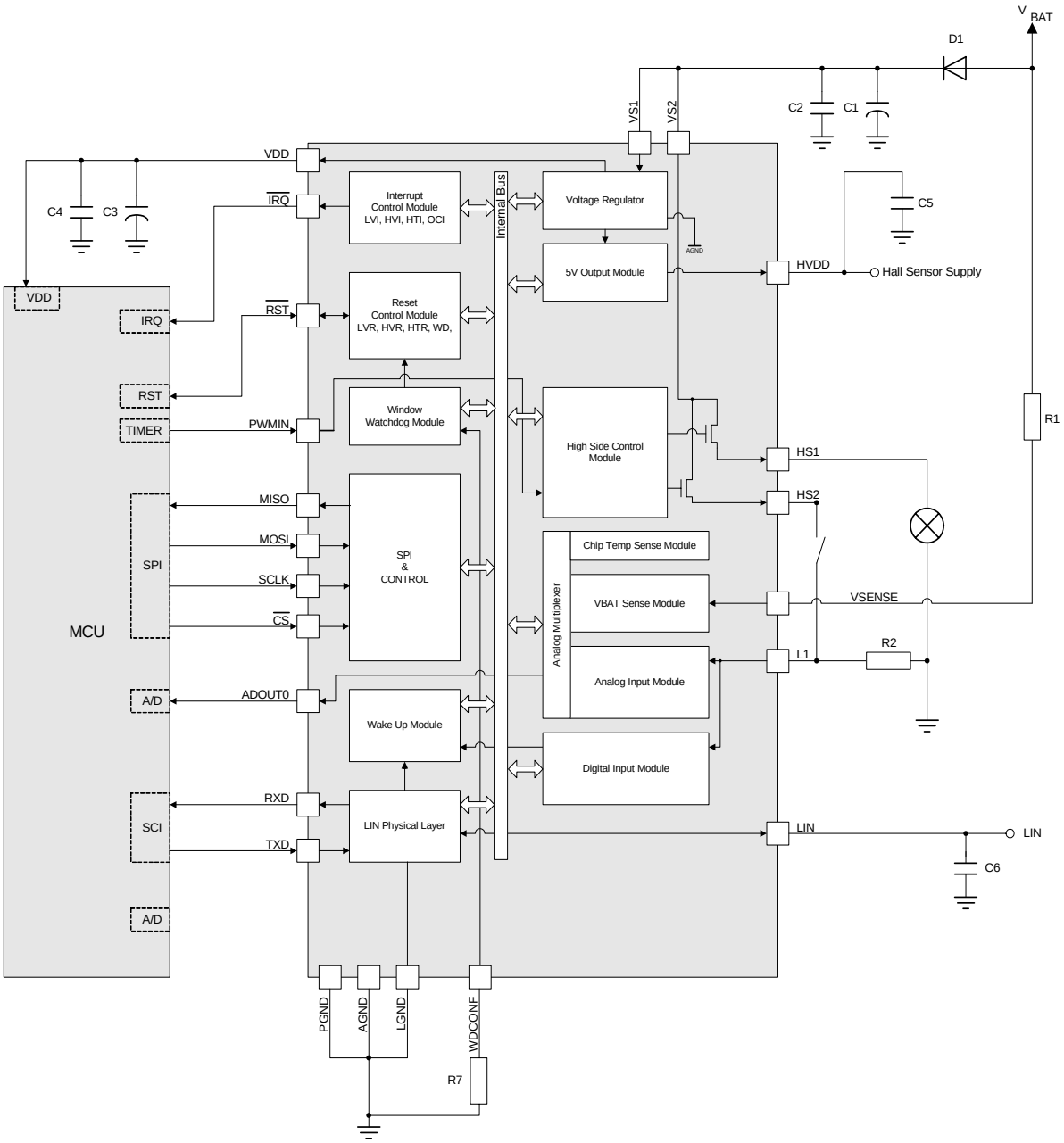
In case more than one interrupt is pending, than the interrupt sources are handled sequentially multiplex.

Table 28. Interrupt Sources

				Interrupt Source		Priority
ISR3	**ISR2**	**ISR1**	**ISR0**	**none maskable**	**maskable**	
0	0	0	0	no interrupt	no interrupt	none
0	0	0	1		L1 wake-up from Stop Mode-	highest
0	0	1	0	-	HS interrupt (Over-temperature)	
0	0	1	1	-	Reserved	
0	1	0	0		LIN interrupt (RXSHORT, TXDOM, LIN OT, LIN OC) or LIN wake-up	
0	1	0	1	Voltage monitor interrupt (Low-voltage and VDD over-temperature)	Voltage monitor interrupt (High-voltage)	
0	1	1	0	-	Forced wake-up	lowest

TYPICAL APPLICATIONS

The 33910 can be configured in several applications. The figure below shows the 33910 in the typical Slave Node Application.



Typical Component Values:

C1 = 47µF; C2 = C4 = 100nF; C3 = 10µF; C5 = 220pF

R1 = 10kΩ; R2 = 20kΩ-200kΩ

Recommended Configuration of the not Connected Pins (NC):

Pin 15, 16, 17, 19, 20, 21, 22 = GND

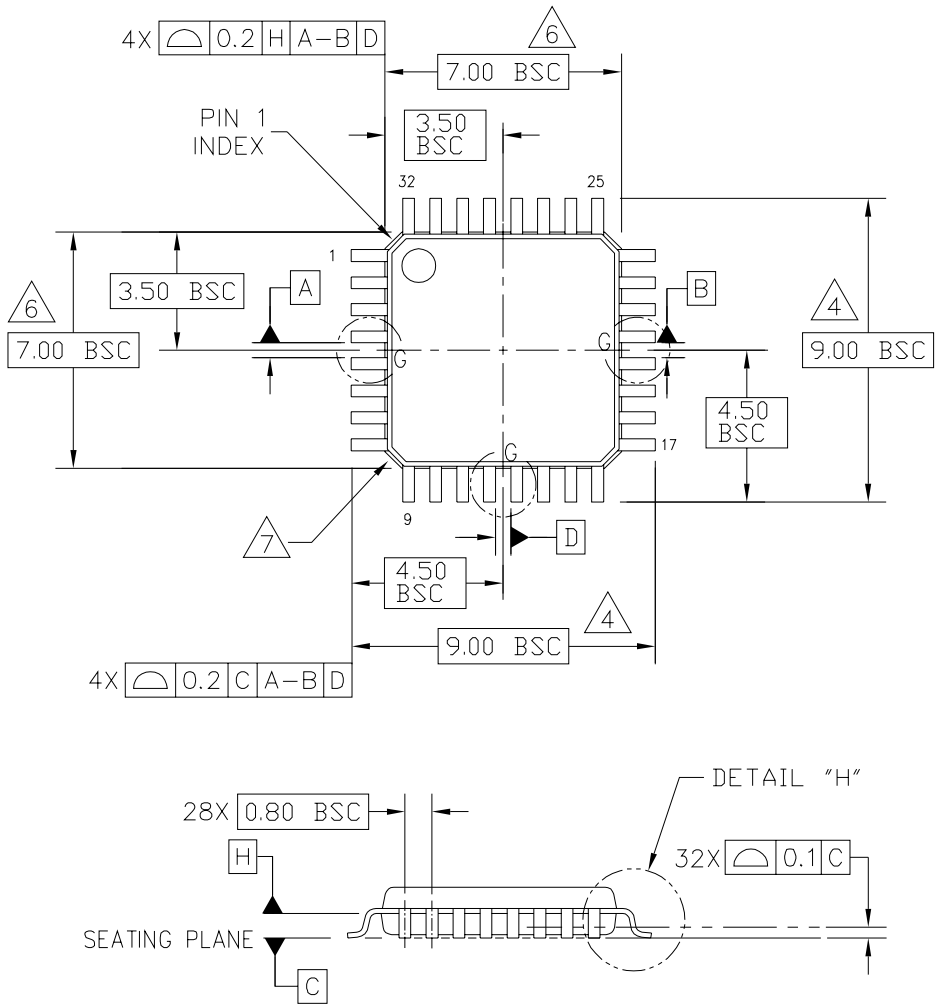
Pin 11 = open (floating)

Pin 28 = this pin is not internally connected and may be used for PCB routing optimization.

PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.Freescale.com and select Documentation, then under Available Documentation column select Packaging Information.



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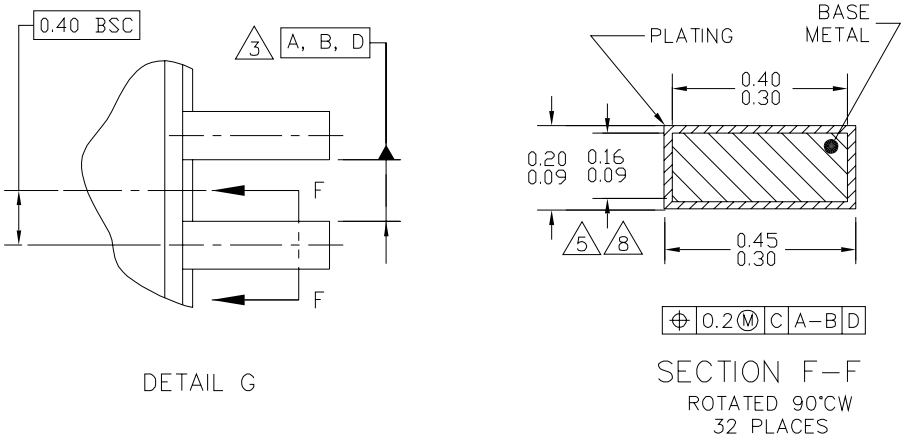
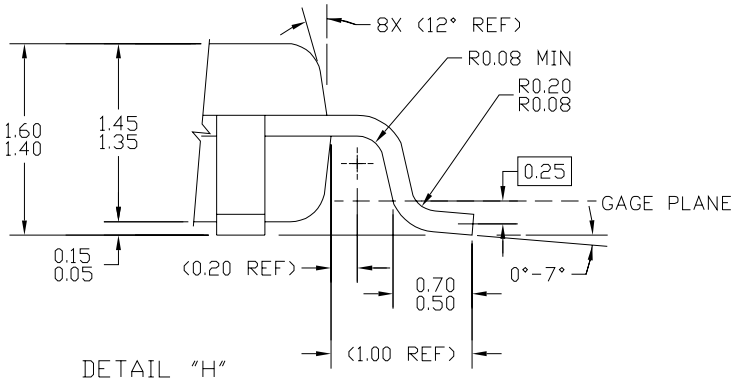
	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

AC SUFFIX (PB-FREE)
32-PIN LQFP
98ASH70029A
REVISION D

PACKAGE DIMENSIONS (Continued)





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AC SUFFIX (PB-FREE)
32-PIN LQFP
98ASH70029A
REVISION D

REVISION HISTORY

Revision	Date	Description of Changes
3.0	9/2007	• Initial Release
4.0	2/2008	• Changed Functional Block Diagram on page 22.

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