SINGLE CHANNEL HIGH SPEED TRANSISTOR OPTOCOUPLERS

HCPL-0452 HCPL-0500 HCPL-0501

DESCRIPTION

The HCPL-0500, HCPL-0501 and HCPL-0452 optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor housed in a compact 8-pin smalloutline package.

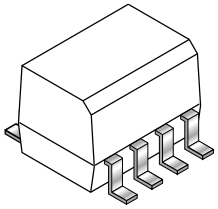
A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

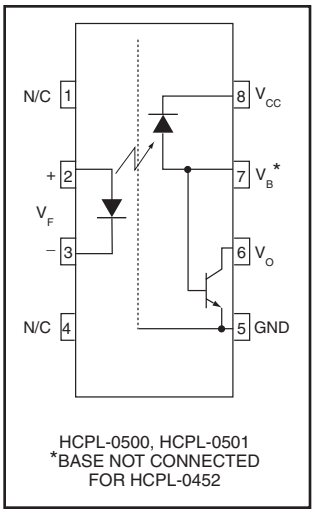
FEATURES

- High speed-1 MBit/s
- Superior CMR-1 kV/µs
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)

APPLICATIONS

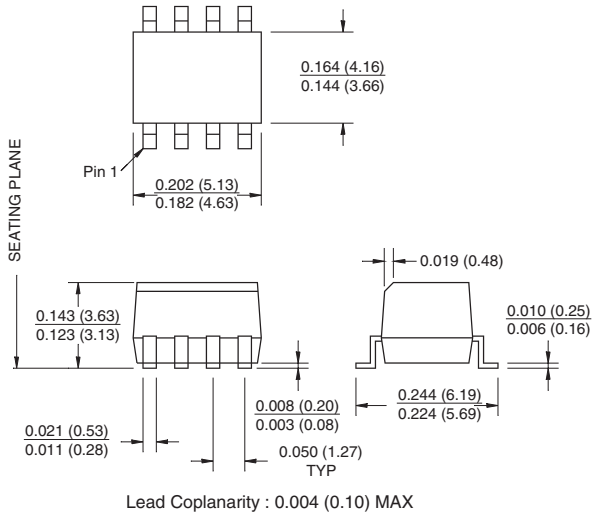
- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling





HCPL-0500, HCPL-0501
*BASE NOT CONNECTED
FOR HCPL-0452

PACKAGE DIMENSIONS



Lead Coplanarity : 0.004 (0.10) MAX

NOTE
All dimensions are in inches (millimeters)

SINGLE CHANNEL HIGH SPEED TRANSISTOR OPTOCOUPLERS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	T_{STG}	-55 to +125	°C
Operating Temperature	T_{OPR}	-55 to +100	°C
Reflow Temperature Profile (Refer to fig. 11)			
EMITTER			
DC/Average Forward Input Current	I_F (avg)	25	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	I_F (pk)	50	mA
Peak Transient Input Current - ([≤1 µs P.W., 300 pps)	I_F (trans)	1.0	A
Reverse Input Voltage	V_R	5	V
Input Power Dissipation	P_D	45	mW
DETECTOR			
Average Output Current (Pin 6)	I_O (avg)	8	mA
Peak Output Current	I_O (pk)	16	mA
Emitter-Base Reverse Voltage (Except HCPL-0452)	V_{EBR}	5	V
Supply Voltage	V_{CC}	-0.5 to 30	V
Output Voltage	V_O	-0.5 to 20	V
Base Current (Except HCPL-0452)	I_B	5	mA
Output power dissipation	P_D	100	mW

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER	(I_F = 16 mA, T_A =25°C)	V_F	All		1.45	1.7	V
Input Forward Voltage	(I_F = 16 mA)					1.8	
Input Reverse Breakdown Voltage	(I_R = 10 µA)	BV_R	All	5.0			V
Temperature coefficient of forward voltage	(I_F = 16 mA)	($\Delta V_F/\Delta T_A$)	All		-1.6		mV/°C
DETECTOR							
Logic high output current	(I_F = 0 mA, V_O = V_{CC} = 5.5 V) (T_A =25°C)	I_{OH}	All		0.001	0.5	µA
	(I_F = 0 mA, V_O = V_{CC} = 15 V) (T_A =25°C)		All		0.005	1	
	(I_F = 0 mA, V_O = V_{CC} = 15 V)		All			50	
Logic low supply current	(I_F = 16 mA, V_O = Open) (V_{CC} = 15 V)	I_{CCL}	All		120	200	µA
Logic high supply current	(I_F = 0 mA, V_O = Open, V_{CC} = 15 V) (T_A =25°C)	I_{CCH}	All		0.01	1	µA
	(I_F = 0 mA, V_O = Open) (V_{CC} = 15 V)		All			2	

TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
COUPLED Current transfer ratio (Note 5)	(I_F = 16 mA, V_O = 0.4 V) (V_{CC} = 4.5 V, T_A =25°C)	CTR	HCPL-0500	7	27	50	%
			HCPL-0452	19	27	50	
			HCPL-0501				
	(I_F = 16 mA, V_O = 0.5 V) (V_{CC} = 4.5 V)		HCPL-0500	5	30		
			HCPL-0452	15	30		
			HCPL-0501				
Logic low output voltage output voltage	(I_F = 16 mA, I_O = 1.1 mA) (V_{CC} = 4.5 V, T_A =25°C)	V_{OL}	HCPL-0500		0.18	0.4	V
	(I_F = 16 mA, I_O = 3 mA) (V_{CC} = 4.5 V, T_A =25°C)		HCPL-0452		0.25	0.4	
			HCPL-0501				
	(I_F = 16 mA, I_O = 0.8 mA) (V_{CC} = 4.5 V)		HCPL-0500		0.13	0.5	
	(I_F = 16 mA, I_O = 2.4 mA) (V_{CC} = 4.5 V)		HCPL-0452		0.23	0.5	
			HCPL-0501				

** All typicals at T_A = 25°C

SWITCHING CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified., V_{CC} = 5 V)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low	T_A = 25°C, (R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 9)	T_{PHL}	HCPL-0500		0.45	1.5	µs
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 9) T_A = 25°C		HCPL-0452		0.45	0.8	
			HCPL-0501				
	(R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 9)		HCPL-0500			2.0	
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 9)		HCPL-0452			1.0	
			HCPL-0501				
Propagation delay time to logic high	T_A = 25°C, (R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 9)	T_{PLH}	HCPL-0500		0.5	1.5	µs
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 9) T_A = 25°C		HCPL-0452		0.3	0.8	
			HCPL-0501				
	(R_L = 4.1 kΩ, I_F = 16 mA) (Note 6) (Fig. 9)		HCPL-0500			2.0	
	(R_L = 1.9 kΩ, I_F = 16 mA) (Note 7) (Fig. 9)		HCPL-0452			1.0	
			HCPL-0501				
Common mode transient immunity at logic high	(I_F = 0 mA, V_{CM} = 10 V_{P-P}, R_L = 4.1 kV) (Note 8) (Fig. 10) T_A = 25°C	$\|CM_H\|$	HCPL-0500		1,000		V/µs
	(I_F = 0 mA, V_{CM} = 10 V_{P-P}) T_A = 25°C, (R_L = 1.9 kΩ) (Note 8) (Fig. 10)		HCPL-0452		1,000		
			HCPL-0501				
Common mode transient immunity at logic low	(I_F = 16 mA, V_{CM} = 10 V_{P-P}, R_L = 4.1 kΩ) (Note 8) (Fig. 10) T_A = 25°C	$\|CM_L\|$	HCPL-0500		1,000		V/µs
	(I_F = 16 mA, V_{CM} = 10 V_{P-P}) (R_L = 1.9 kΩ) (Note 8) (Fig. 10)		HCPL-0452		1,000		
			HCPL-0501				

ISOLATION CHARACTERISTICS (T_A = 0°C to +70°C Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-Output Isolation Voltage	(f = 60 Hz, t = 1.0 min)[9,10]	V_{ISO}	2500	—	—	Vac_{RMS}
Isolation Resistance	(V_{I-O} = 500 V)[9]	R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance	(V_{I-O} = 0 , f = 1.0 MHz)[9]	C_{ISO}	—	0.2	—	pF

** All typicals at TA = 25°C

NOTES

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
5. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1kΩ pull-up resistor.
7. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull-up resistor.
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, VCM, to assure that the output will remain in a logic low state (i.e., V_O<0.8 V).
9. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
10. 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

TYPICAL PERFORMANCE CURVES

Fig. 1 Input Forward Current vs. Input Forward Voltage

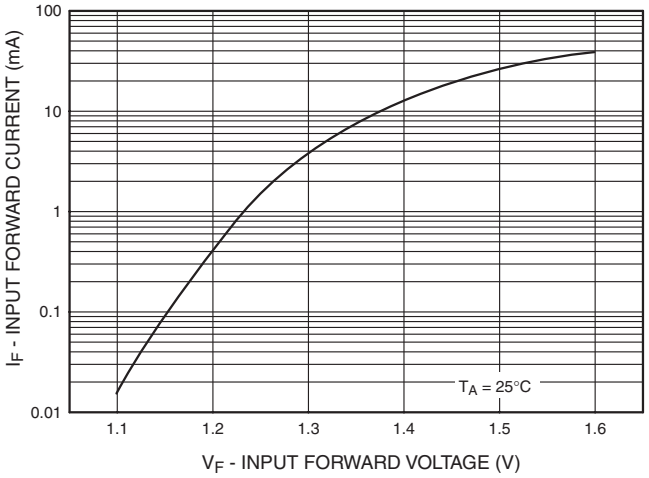


Fig. 2 Current Transfer Ratio vs. Input Current

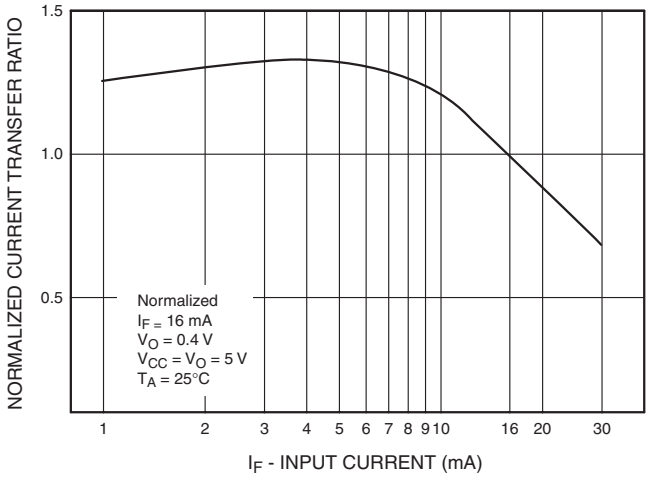


Fig. 3 Current Tansfer Ratio vs. Input Forward Current

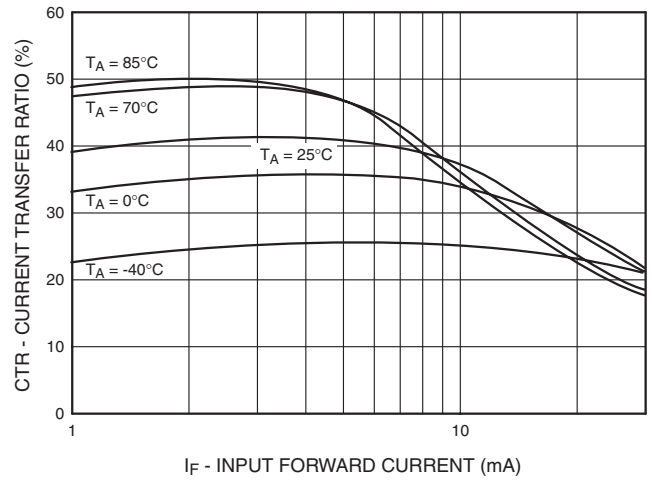
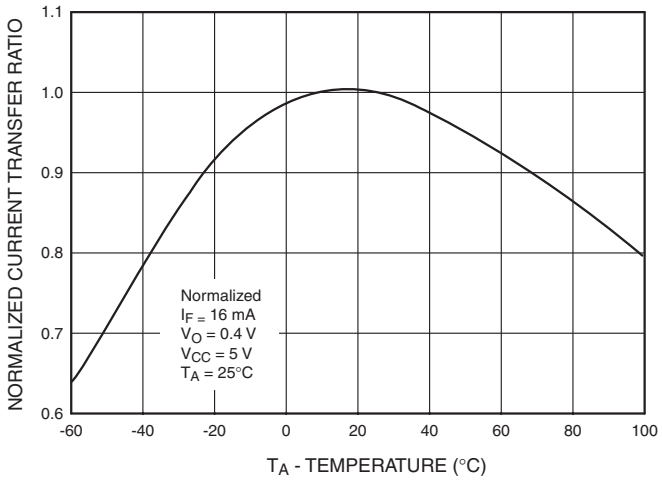


Fig. 4 Current Transfer Ratio vs. Temperature



TYPICAL PERFORMANCE CURVES

Fig. 5 DC Transfer Characteristics

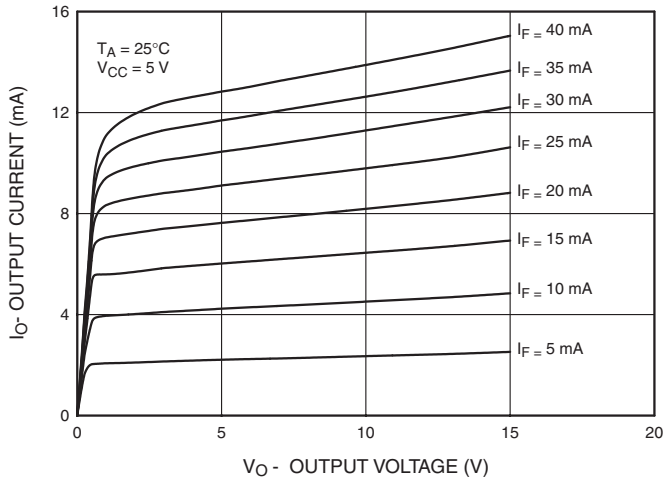


Fig. 6 Logic Low Supply Current vs. Input Current

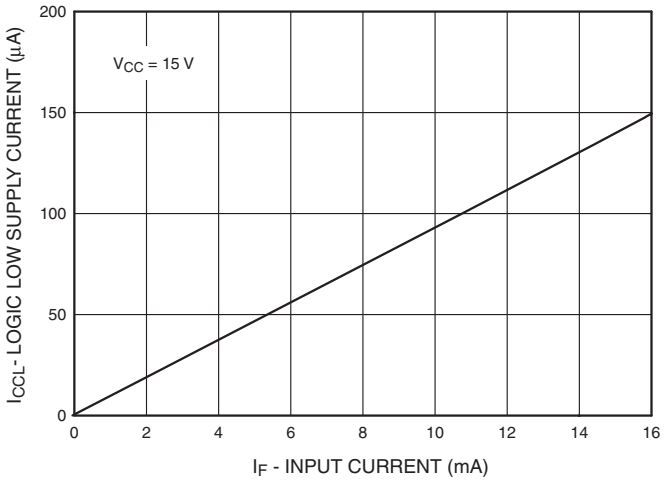


Fig. 7 Logic High Output Current vs. Temperature

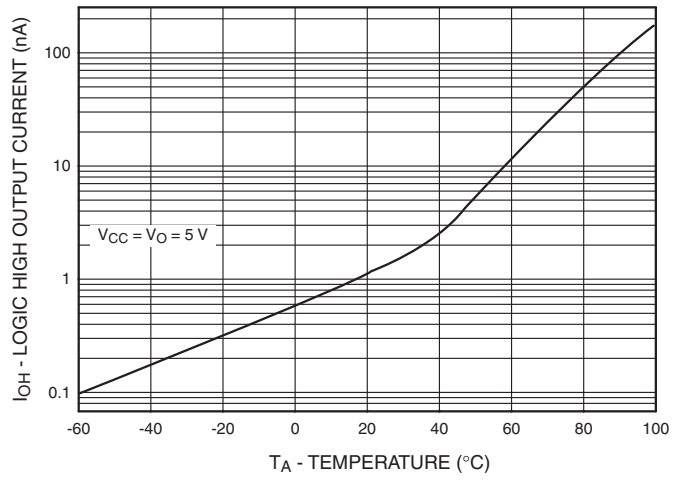
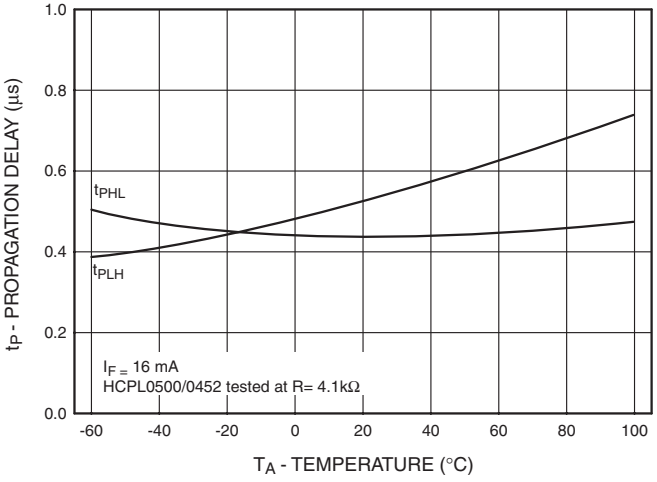


Fig. 8 Propagation Delay vs. Temperature



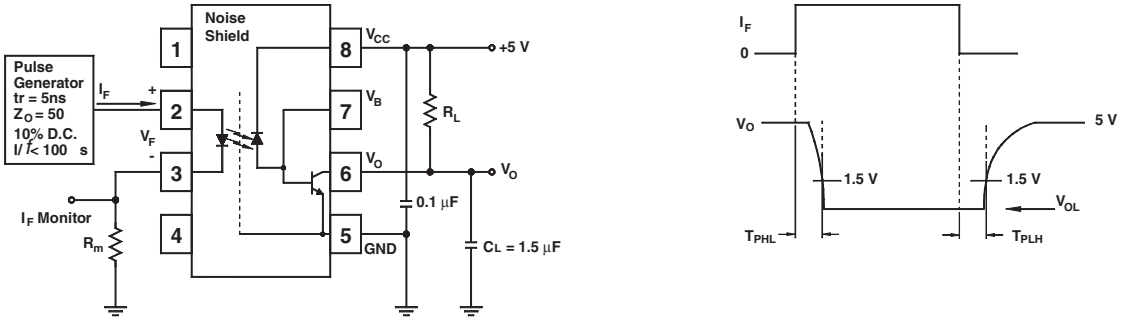


Fig. 9 Switching Time Test Circuit

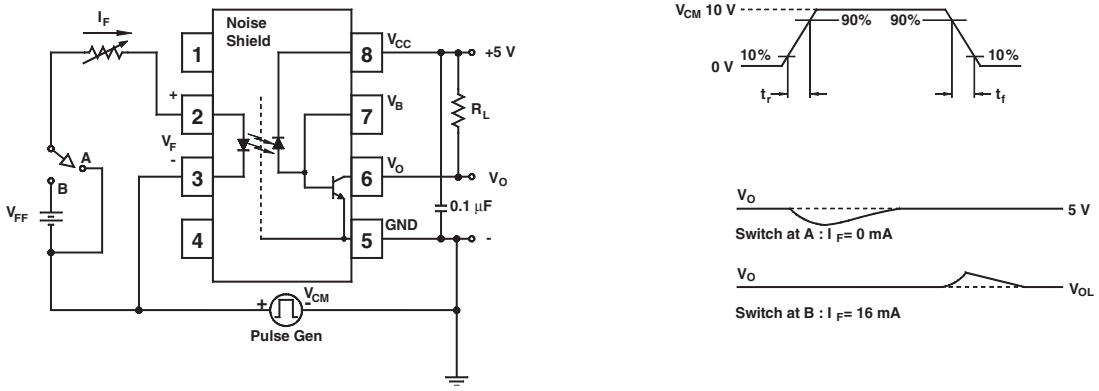
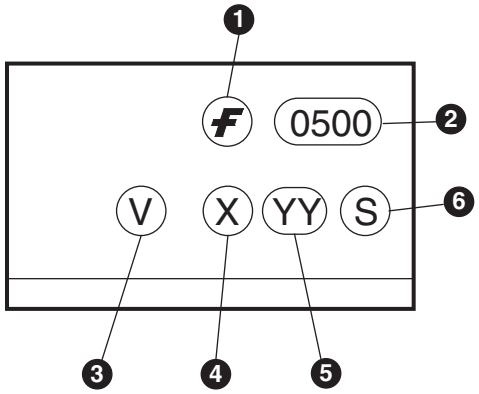


Fig. 10 Common Mode Immunity Test Circuit

ORDERING INFORMATION

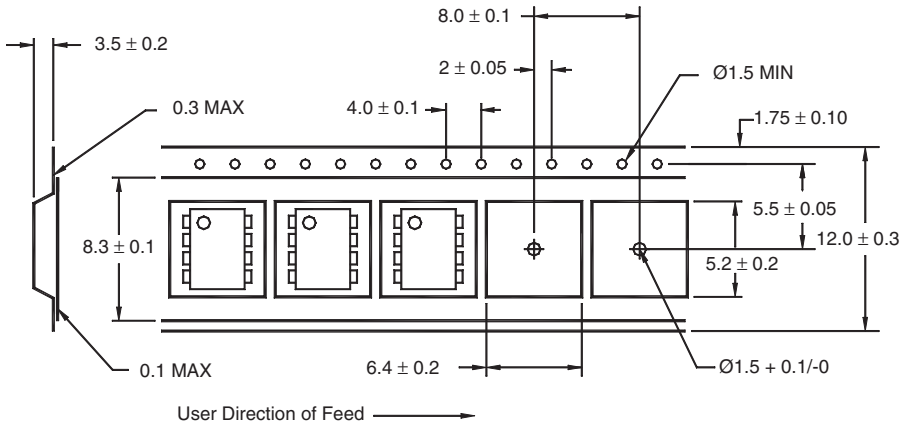
Option	Order Entry Identifier	Description
V	V	VDE 0884
R1	R1	Tape and reel (500 units per reel)
R1V	R1V	VDE 0884, Tape and reel (500 units per reel)
R2	R2	Tape and reel (2500 units per reel)
R2V	R2V	VDE 0884, Tape and reel (2500 units per reel)

MARKING INFORMATION

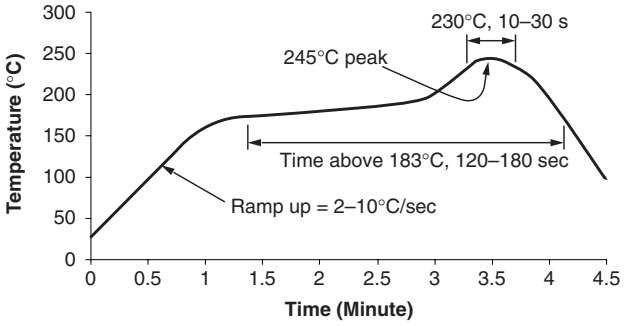


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., ‘3’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Carrier Tape Specifications



Reflow Profile



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.