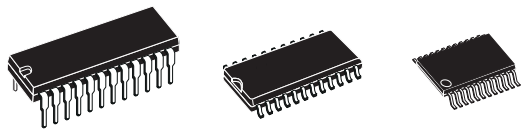
M74HC181

ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

- HIGH SPEED:
  t_{PD}= 13 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 181



DIP SOP TSSOP

ORDER CODES

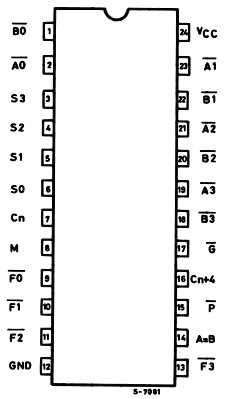
PACKAGE	TUBE	T & R
DIP	M74HC181B1R	
SOP	M74HC181M1R	M74HC181RM13TR
TSSOP		M74HC181TTR

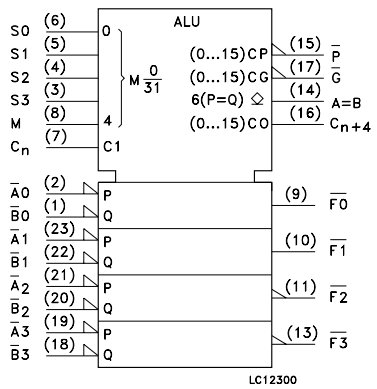
DESCRIPTION

The M74HC181 is an high speed CMOS ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR fabricated with silicon gate C^2MOS technology.

This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in tables 1 and 2. These operations are selected by the four function select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the M74HC182, full carry look-ahead circuits, high speed arithmetic operations can be performed. These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below . Subtraction is accomplished by 1,s complement addition where 1's complement of the subtrahend is generated internally. The resultant output is 1-B-1, which requires an end around or forced carry to produce A-B. The 181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs ($\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$) so that when two words of equal magnitude are applied at the A and

PIN CONNECTION AND IEC LOGIC SYMBOLS

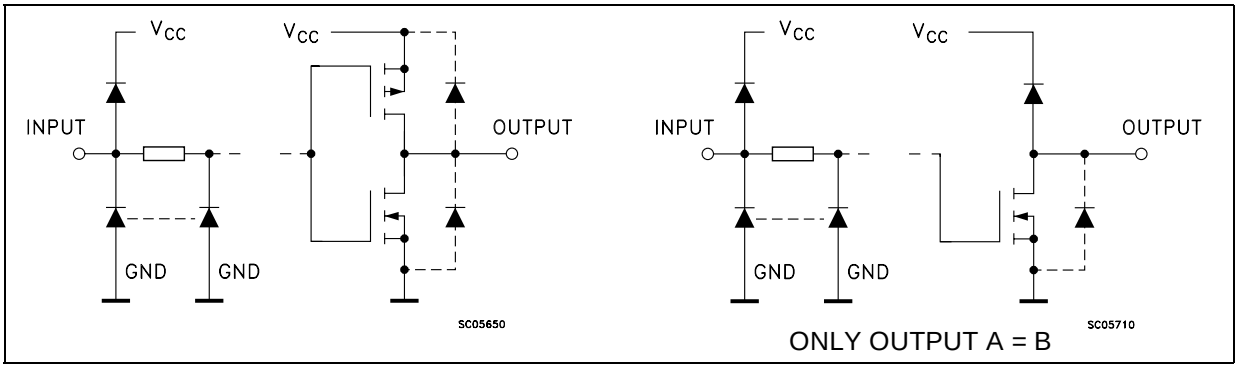




DESCRIPTION (Continued)
B inputs , it will assume a high level to indicated equality (A=B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open drain so that it can be wire-AND connected to give a comparison for more that four bits. The carry output (C_n + 4) can also be used to supply relative magnitude information.
Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively. These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible function of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode - control (M) at a high level to disable the internal carry.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUITS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 23, 21, 19	$\overline{A0}$ to $\overline{A3}$	Word A Inputs
1, 22, 20, 18	$\overline{B0}$ to $\overline{B3}$	Word B Inputs
6, 5, 4, 3	S0 to S3	Function Select Inputs
7	C_n	Inv. Carry Input
8	M	Mode Control Input
9, 10, 11, 13	$\overline{F0}$ to $\overline{F3}$	Function Outputs
14	A = B	Comparator Output
15	$\overline{P}$	Carry Propagate Output
16	C_n + 4	Inv. Carry Output
17	$\overline{G}$	Carry Generate Output
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
ACTIVE LOW DATA (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	C_n	C_n + 4	$\overline{P}$	$\overline{G}$
ACTIVE HIGH DATA (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	C_n	C_n + 4	X	Y

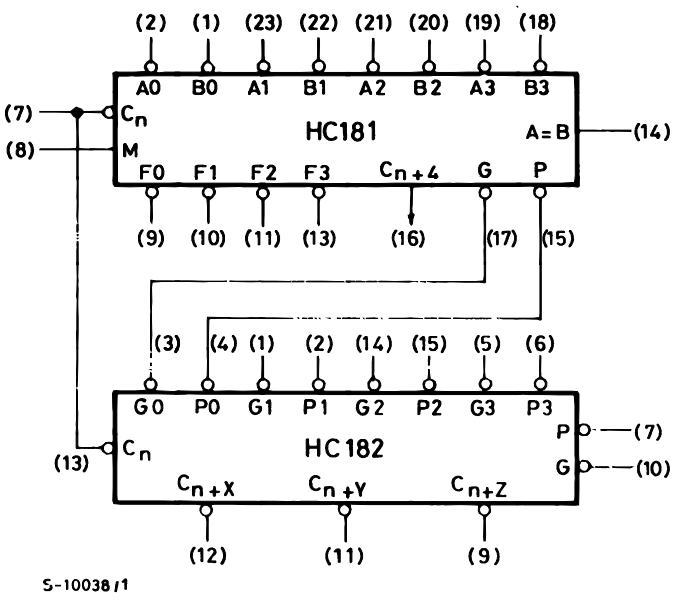
INPUT C_N	INPUT C_N + 4	ACTIVE LOW DATA (FIGURE1)	ACTIVE HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

TRUTH TABLE 1

SELECTION				ACTIVE LOW DATA		
				M = H LOGIC FUNCTIONS	M = L ARITHMETIC OPERATIONS	
S3	S2	S1	S0		Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A}$ + $\overline{B}$	F = A plus (A + $\overline{B}$)	F = A plus (A + $\overline{B}$) plus 1
L	H	L	H	F = $\overline{B}$	F =AB plus (A + B)	F = AB plus (A + $\overline{B}$) plus 1
L	H	H	L	F = $\overline{A}$ ⊕ $\overline{B}$	F = A minus B minus 1	F = A minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) plus 1
H	L	L	L	F = $\overline{AB}$	F = A plus (A + B)	F = A plus (A + B) plus 1
H	L	L	H	F = A ⊕ B	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	F =A$\overline{B}$ plus (A + B)	F = A$\overline{B}$ plus (A + B) plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) plus 1
H	H	L	L	F = 0	F = A plus A*	F = A plus A plus 1
H	H	L	H	F = A$\overline{B}$	F = AB plus A	F = AB plus A plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ plus A	F = A$\overline{B}$ plus A plus 1
H	H	H	H	F = A	F = A	F = A plus 1

* : Each bit is shifted to the next more significant position.

FIGURE 1

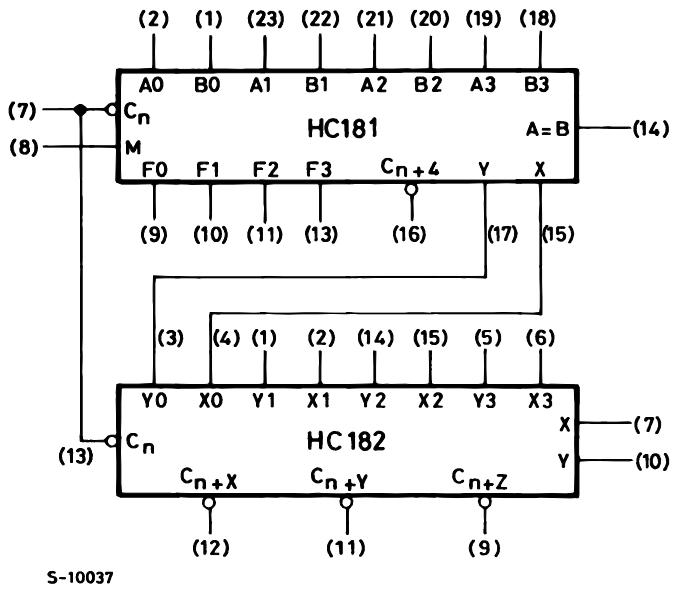


TRUTH TABLE 2

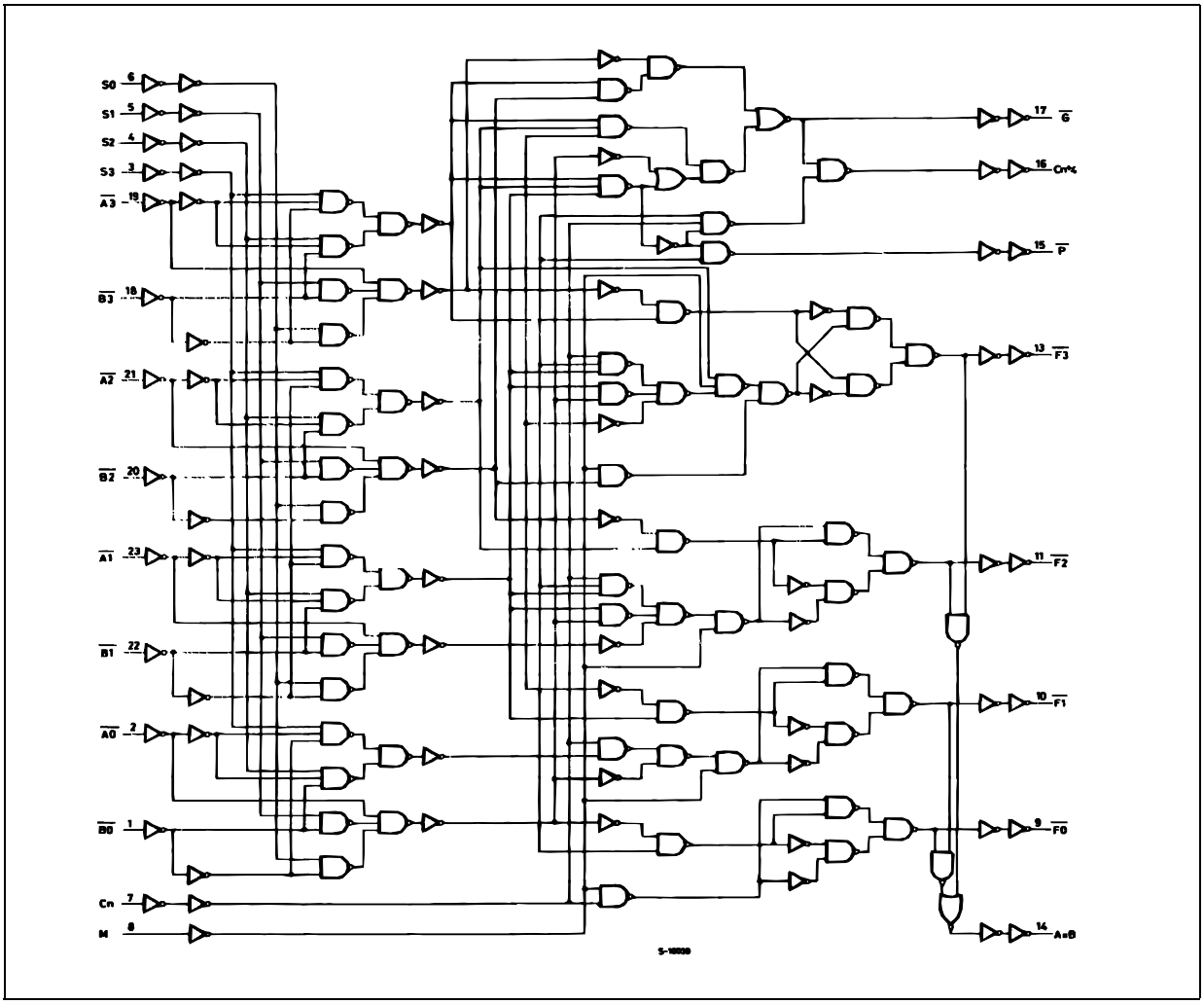
SELECTION				ACTIVE HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L ARITHMETIC OPERATIONS	
S3	S2	S1	S0		Cn = H (no carry)	Cn = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A minus 1	F = A plus 1
L	L	L	H	$F = \overline{A + B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
L	L	H	L	$F = \overline{AB}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
L	L	H	H	F = 0	F = minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	F = A plus $(A\overline{B})$	F = A plus $A\overline{B}$ plus 1
L	H	L	H	$F = \overline{B}$	F =A + B plus $A\overline{B}$	F = (A + B) plus $(A\overline{B})$ plus 1
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1	F = A minus B
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1	F = $A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A plus AB	F = A plus AB plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	$F = (A + \overline{B})$ plus AB	$F = (A + \overline{B})$ plus AB plus 1
H	L	H	H	F = AB	F = AB minus 1	F = AB
H	H	L	L	F = 1	F = A plus A*	F = A plus A plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) plus A	F = (A + B) plus A plus 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ plus A	$F = (A + \overline{B})$ plus A plus 1
H	H	H	H	F = A	F = A minus 1	F = A

* : Each bit is shifted to the next more significant position.

FIGURE 2



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (except A = B output)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (1)	2.0			54	120		150		170	ns
		4.5			16	24		30		45	
		6.0			13	20		26		35	
t_{PLH} t_{PHL}	Propagation Delay Time (2)	2.0			90	215		270		300	ns
		4.5			26	43		54		65	
		6.0			20	37		46		55	
t_{PLH} t_{PHL}	Propagation Delay Time (3)	2.0			97	215		270		300	ns
		4.5			27	43		54		65	
		6.0			21	37		46		60	
t_{PLH} t_{PHL}	Propagation Delay Time (4)	2.0			80	180		225		250	ns
		4.5			23	36		45		60	
		6.0			18	31		38		50	
t_{PLH} t_{PHL}	Propagation Delay Time (5)	2.0			81	190		240		260	ns
		4.5			24	38		48		60	
		6.0			19	32		41		50	
t_{PLH} t_{PHL}	Propagation Delay Time (6)	2.0			80	180		225		240	ns
		4.5			23	36		45		55	
		6.0			18	31		38		50	
t_{PLH} t_{PHL}	Propagation Delay Time (7)	2.0			80	170		215		230	ns
		4.5			23	34		43		50	
		6.0			18	29		37		48	
t_{PLH} t_{PHL}	Propagation Delay Time (8)	2.0			80	170		215		230	ns
		4.5			23	34		43		56	
		6.0			18	29		37		50	
t_{PLH} t_{PHL}	Propagation Delay Time (9)	2.0			95	220		275		290	ns
		4.5			27	44		55		65	
		6.0			21	37		47		60	
t_{PLH} t_{PHL}	Propagation Delay Time (10)	2.0			95	220		275		285	ns
		4.5			27	44		55		70	
		6.0			21	37		47		65	
t_{PLH} t_{PHL}	Propagation Delay Time (11)	2.0			86	200		250		260	ns
		4.5			24	40		50		65	
		6.0			18	34		43		60	
t_{PLH} t_{PHL}	Propagation Delay Time (12)	2.0	R_L = 1KΩ		92	210		265		280	ns
		4.5			27	42		53		60	
		6.0			27	36		45		55	

CAPACITIVE CHARACTERISTICS

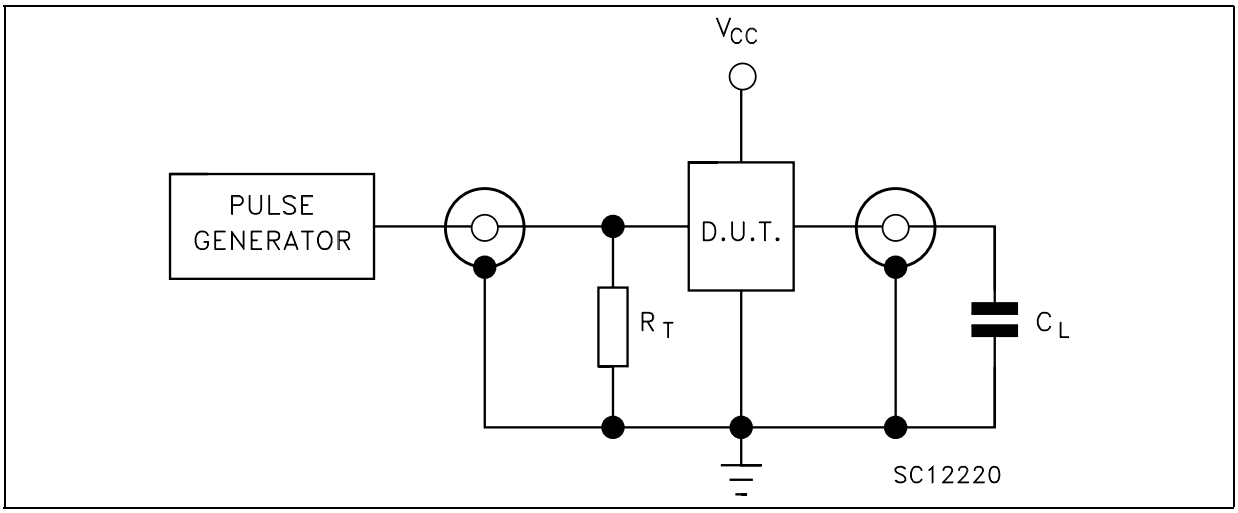
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)				195						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

PROPAGATION DELAY TIME TEST CONDITIONS

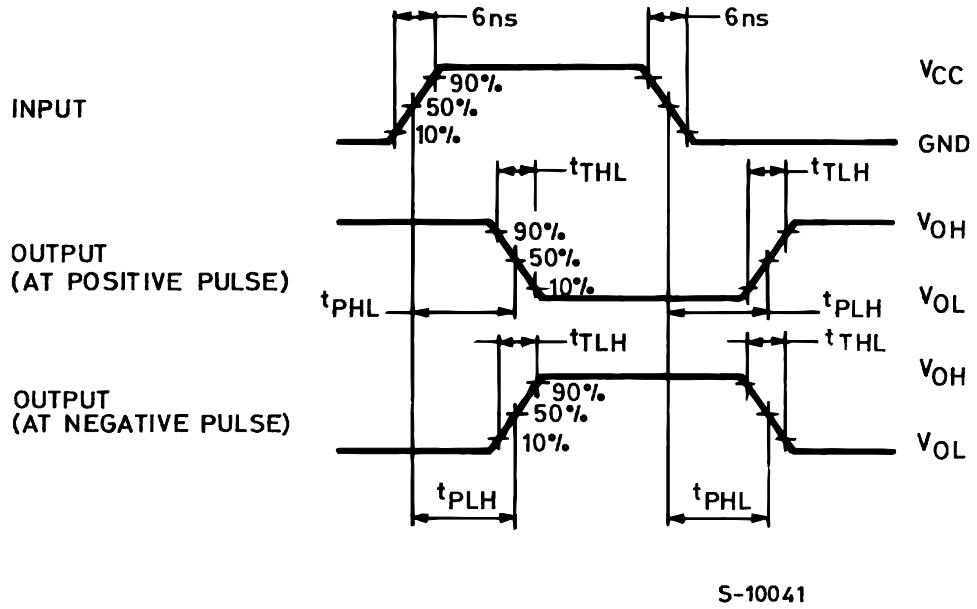
Test No	INPUT	OUTPUT	Test Conditions
(1)	C_n	$C_n + 4$	
(2)	Any $\overline{A}$ or $\overline{B}$	$C_n + 4$	M=GND, S0=S3=Vcc, S1=S2=GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	$C_n + 4$	M=GND, S0=S3=GND, S1=S2=Vcc ($\overline{DIFF}$ mode)
(4)	$\overline{C_n}$	Any $\overline{F}$	M=GND ($\overline{SUM}$ or $\overline{DIFF}$)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=Vcc, S1=S2=GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=GND, S1=S2=Vcc ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=Vcc, S1=S2=GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=GND, S1=S2=Vcc ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=Vcc, S1=S2=GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=GND, S1=S2=Vcc ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	Fi	M = Vcc (Logic Mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A = B	M=GND, S0=S3=GND, S1=S2=Vcc ($\overline{DIFF}$ mode)

TEST CIRCUIT



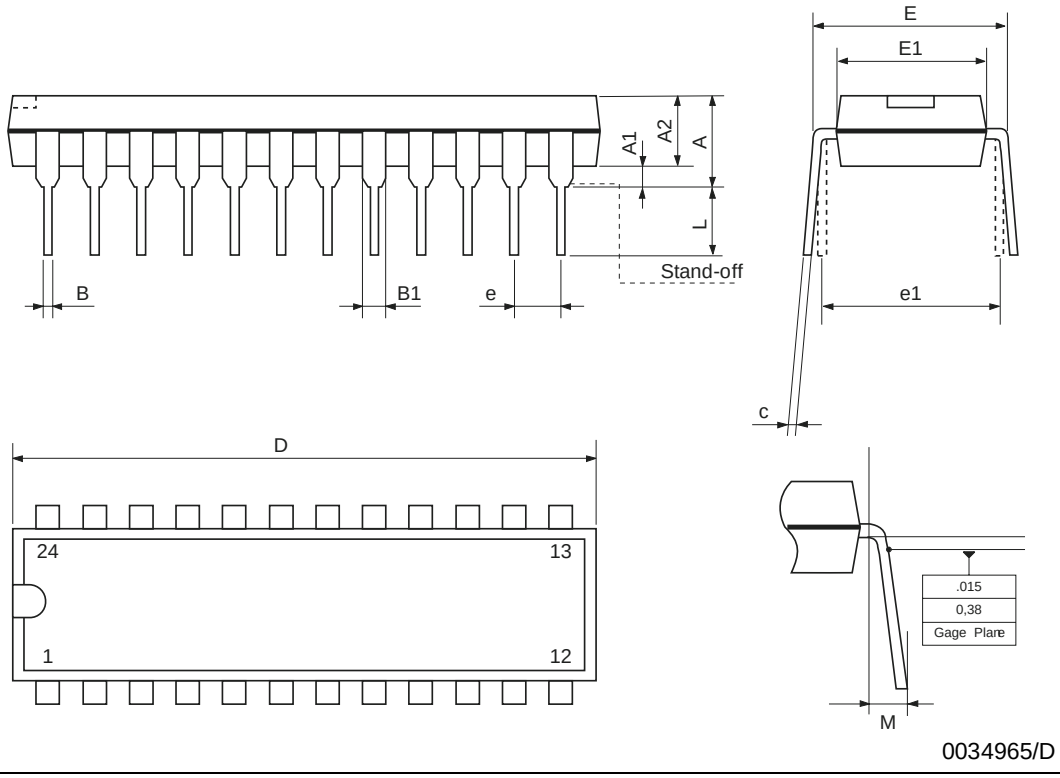
C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



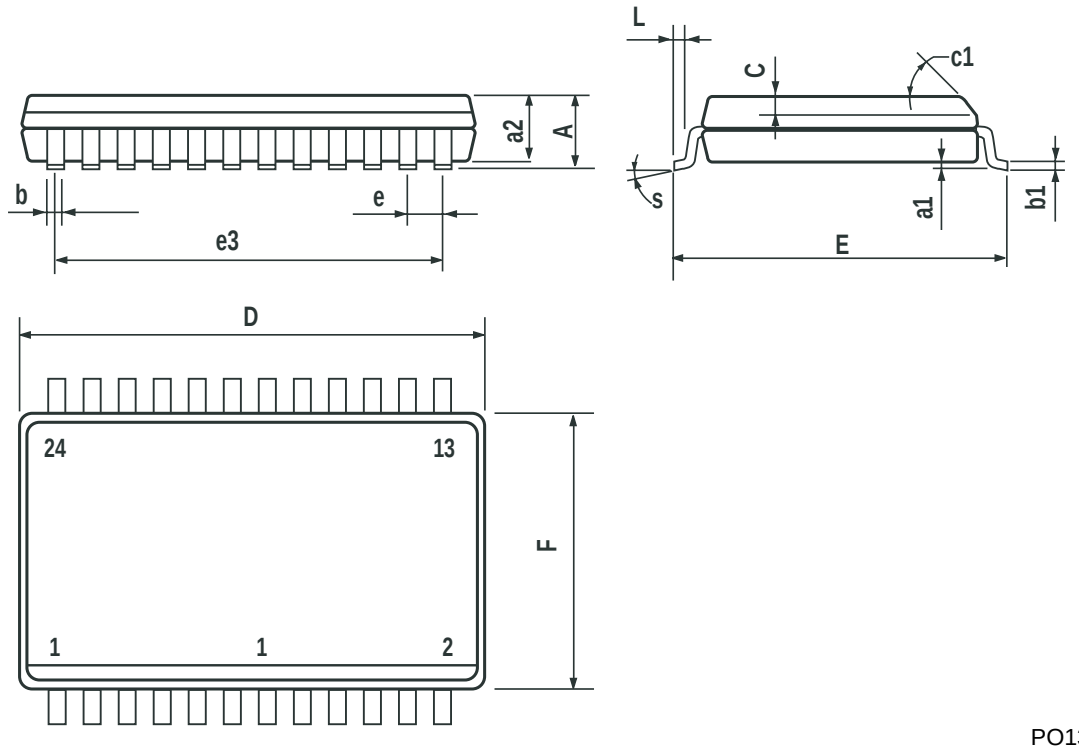
Plastic DIP-24 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			4.32			0.170
A1	0.38			0.015		
A2		3.3			0.130	
B	0.41	0.46	0.51	0.016	0.018	0.020
B1	1.40	1.52	1.65	0.055	0.060	0.065
c	0.20	0.25	0.30	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.62		8.26	0.300		0.325
E1	6.35	6.60	6.86	0.250	0.260	0.270
e		2.54			0.100	
E1		7.62			0.300	
L	3.18		3.43	0.125		0.135
M	0°		15°	0°		15°



SO-24 MECHANICAL DATA

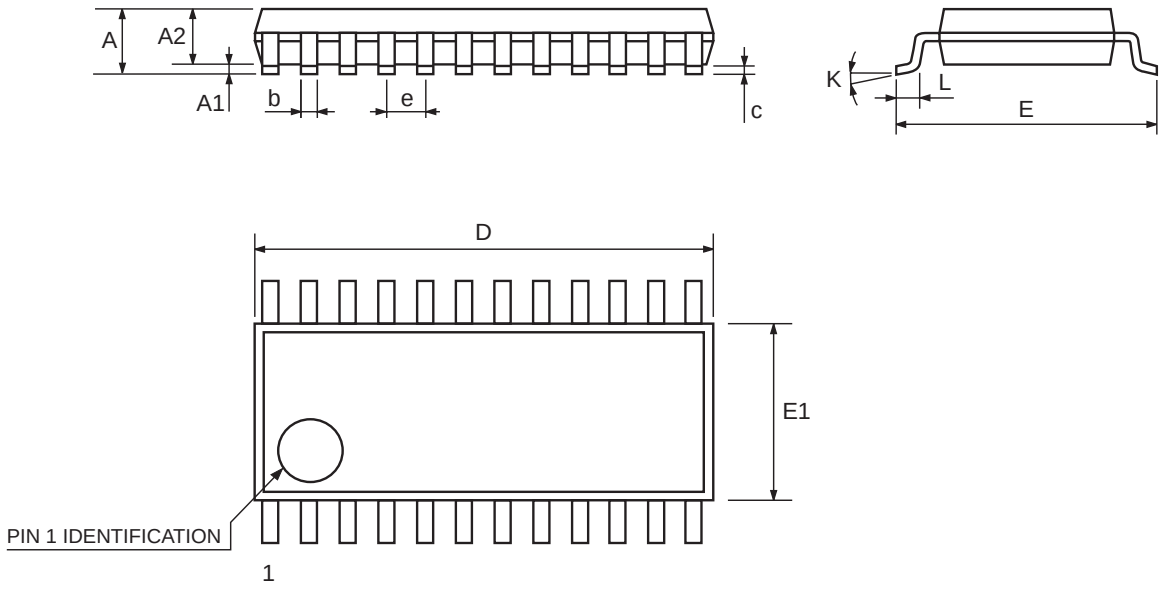
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



PO13T

TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	6.25		6.5	0.246		0.256
E1	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028



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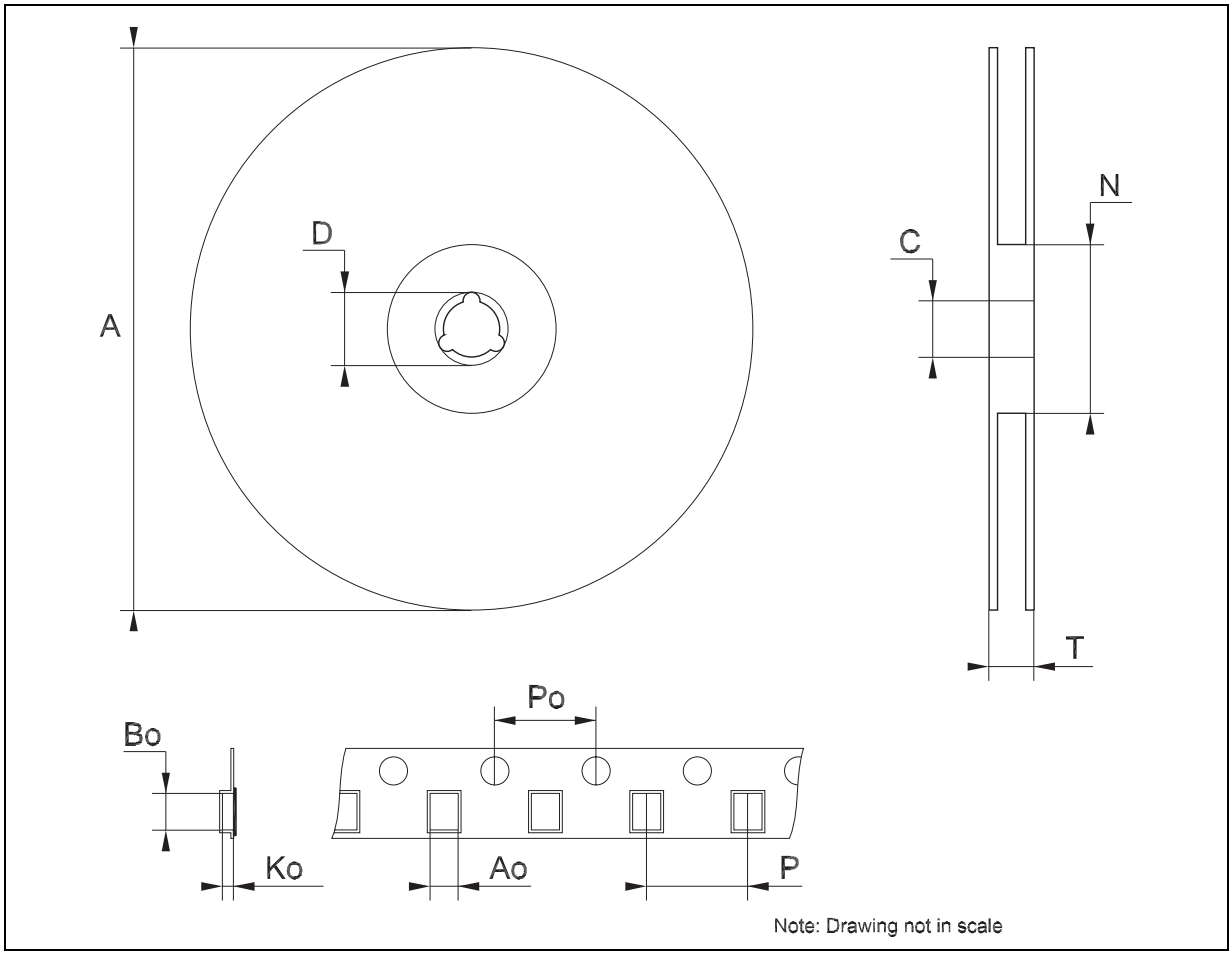
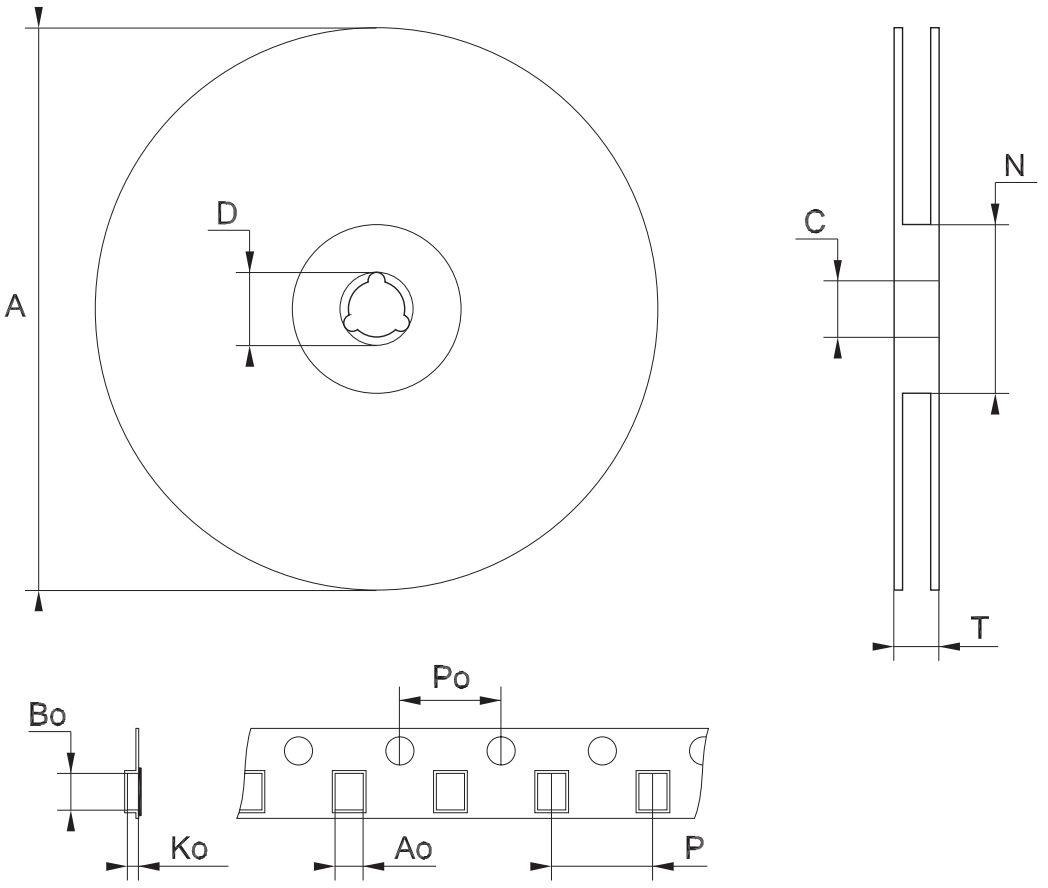
Tape & Reel SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Tape & Reel TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale