



STC2G15

BCMOS VOLTAGE REGULATOR DESIGNED FOR USE WITH VERY LOW ESR AND TANTALUM OUTPUT CAPACITOR

- INPUT VOLTAGE FROM 2.7V TO 5.02V
- STABLE WITH LOW ESR CERAMIC AND TANTALUM CAPACITORS
- VERY LOW QUIESCENT CURRENT (30 μ A TYP. AT NO LOAD; 2 μ A IN OFF MODE)
- GUARANTEED OUTPUT CURRENT UP TO 15mA
- OUTPUT VOLTAGE: 1.5V
- LOGIC-CONTROLLED ELECTRONIC SHUTDOWN
- INTERNAL CURRENT LIMIT
- JUNCTION TEMPERATURE RANGE: -40°C TO 95°C

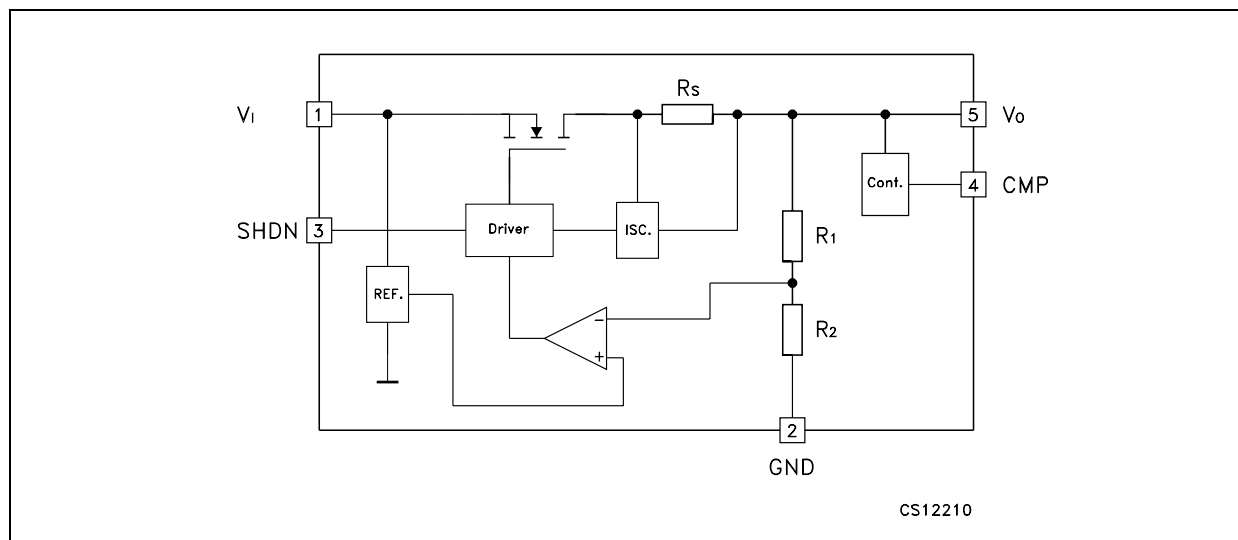
DESCRIPTION

The STC2G15 provides up to 15mA, from 2.5V to 6V input voltage. The low quiescent current makes it suitable for low power applications and in battery powered systems.



Shutdown Logic Control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The STC2G15 is designed to work with low ESR ceramic and tantalum capacitors. Typical applications are in mobile phone, blue-tooth module and similar battery powered wireless systems.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

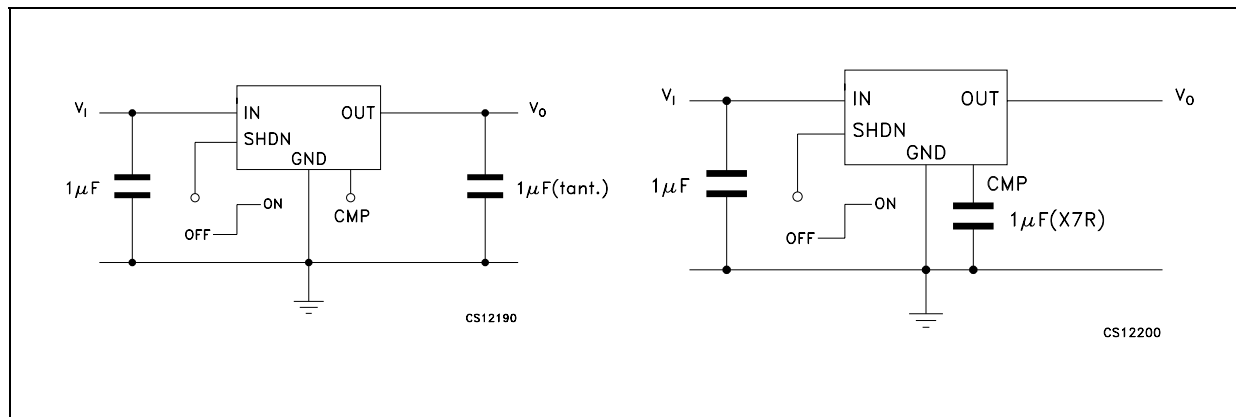
| Symbol | Parameter | Value | Unit |
|-----------|--------------------------------------|------------------------|------|
| V_I | DC Input Voltage | -0.3 to 5.4 | V |
| V_O | DC Output Voltage | -0.3 to $V_{IN} + 0.3$ | V |
| V_{INH} | INHIBIT Input Voltage | -0.3 to $V_{IN} + 0.3$ | V |
| I_O | Output Current | Internally limited | |
| P_{tot} | Power Dissipation | Internally limited | |
| T_{stg} | Storage Temperature Range | -55 to +150 | °C |
| T_{op} | Operating Junction Temperature Range | -40 to +95 | °C |
| ESD | Electrostatic Discharge HBM (DH11C) | 2 | kV |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

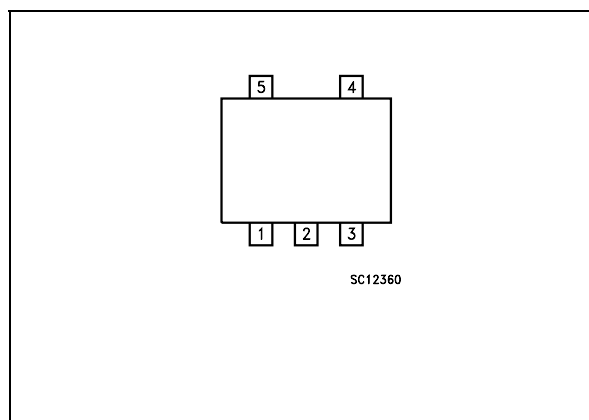
THERMAL DATA

| Symbol | Parameter | TSOT23-5L | Unit |
|----------------|-------------------------------------|-----------|------|
| $R_{thj-amb}$ | Thermal Resistance Junction-ambient | 225 | °C/W |
| $R_{thj-case}$ | Thermal Resistance Junction-case | 81 | °C/W |

APPLICATION CIRCUITS



CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

| Pin N° | Symbol | Name and Function |
|--------|--------|---|
| 1 | IN | Input Pin |
| 2 | GND | Ground Pin |
| 3 | SHDN | Shutdown Input: Disables the regulator when < 0.4V. Not internally pulled down. |
| 4 | CMP | Compensation Pin: Bypass with a 1µF ceramic X7R capacitor to GND or leave floating if the C_O is connected to OUT pin |
| 5 | OUT | Output Pin: Bypass with a 1µF tantalium capacitor to GND if ceramic X7R capacitor is not used. |

ORDERING CODES

| TYPE | TSOT23-5L | OUTPUT VOLTAGES |
|---------|-----------|-----------------|
| STC2G15 | STC2G15R | 1.5V |

ELECTRICAL CHARACTERISTICS ($C_I = 1\mu\text{F}$, $C_O = 1\mu\text{F}$ (tantalum connected between OUT pin and GND pin) or $C_{\text{CMP}} = 1\mu\text{F}$ (ceramic X7R connected between CMP pin and GND pin) (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|--|------|------|------|-------------------------|
| V_I | Input Voltage | | 2.7 | | 5.2 | V |
| V_O | Output Voltage | $V_I = 2.7$ to 5.2V $I_O = 0$ to 15mA $T_J = -40$ to 95°C | 1.41 | 1.5 | 1.59 | V |
| t_{RU} | Output Voltage Ramp-Up Time (Note 1) | $I_O = 0$ to 15mA | | 10 | 15 | μs |
| t_{RD} | Output Voltage Ramp-Down Time (Note 2) | $I_O = 0$ to 15mA | | 10 | 15 | μs |
| I_O | Current Capability | | 15 | | | mA |
| I_{min} | Minimum Load Current (Note 3) | | 0 | | | mA |
| | Load Regulation (Note 4) | | | 350 | | $\mu\text{V}/\text{mA}$ |
| | Temperature Drift (Note 4) | | | 100 | | $\mu\text{V}/\text{K}$ |
| SVR | Supply Voltage Rejection (Note 5) | $f = 1\text{KHz}$ | 30 | | | dB |
| I_d | Quiescent Current (ON mode) | $I_O = 0$ $I_O = 0$ $V_I = 2.7$ to 5.2V | | 30 | 60 | μA |
| I_d | Quiescent Current (OFF mode) | | | 2 | 4 | μA |
| I_{SHDN} | Shutdown Pin Current | | | 2 | 4 | μA |
| V_{SHDN} | Shutdown Logic Enable Low | | | | 0.4 | V |
| V_{SHDN} | Shutdown Logic Disabled High | | 1.15 | | | V |
| | Line Transient Response Time (Notes 9, 13) | | | 40 | | μs |
| | Load Transient Response Time (Notes 10, 13) | | | 50 | | μs |
| | Line Transient Response Peak + (Notes 9) | | | 80 | | mV |
| | Line Transient Response Peak - (Notes 10) | | | 60 | | mV |
| | Load Transient Response Peak (Notes 11) | | | 50 | | mV |
| eN | Output Noise Voltage | $B = 1\text{kHz}$ to 1MHz $C_O = 1\mu\text{F}$ | | 10 | | mV |

Note 1: Time for the output Voltage to rise from 50% to 85% of nominal value.

Note 2: Time for the output Voltage to fall from 85% to 50% of nominal value.

Note 3: Regulator must be able to sustain Regulated Output Voltage without load.

Note 4: Parameters are uncritical as long as the output voltage stays within limits.

Note 5: A sudden voltage rise/drop of 500mV mustn't bring the output Voltage out of limits.

Note 6: Ceramic Capacitors can be used if connected between CMP pin and GNG, instead of V_{OUT} pin and GND.

Note 8: Maximum and minimum values are guaranteed in full temperature range.

Note 9: Line transient is tested when the input voltage changes from 2.7 to 3.2V in 10 μs in full load range.

Note 10: Line transient is tested when the input voltage changes from 3.2 to 2.7V in 10 μs in full load range.

Note 11: Load transient is tested when the load changes from 0.1 to 15mA in 10 μs in all the input range

Note 13: Response time is defined as the time from the load line step until the output reaches a value within specification (1.41V, 1.59V).

Note 14: The maximum power dissipation for the operation depends on the ambient temperature.

For $T_J = 95^\circ\text{C}$, $T_A = 85^\circ\text{C}$ and $R_{\text{TJA}} = 220^\circ\text{C}/\text{W}$ the maximum power can be 0.045W. The maximum power dissipation for operation can be increased by 4.5mW each degree below $T_A = 85^\circ\text{C}$, and it must be derated by 4.5mW for each degree above 85°C

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified $C_{IN} = C_{COMP} = \text{SMD X5R}$
 $C_{OUT} = \text{Tant.}$, $T_j = 25^\circ\text{C}$)

Figure 1 : Output Voltage vs Temperature

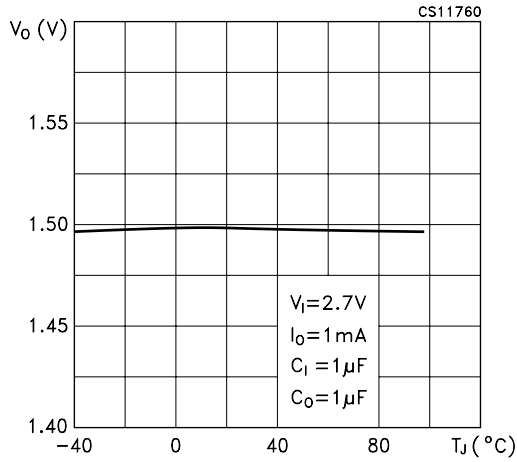


Figure 2 : Output Voltage vs Temperature

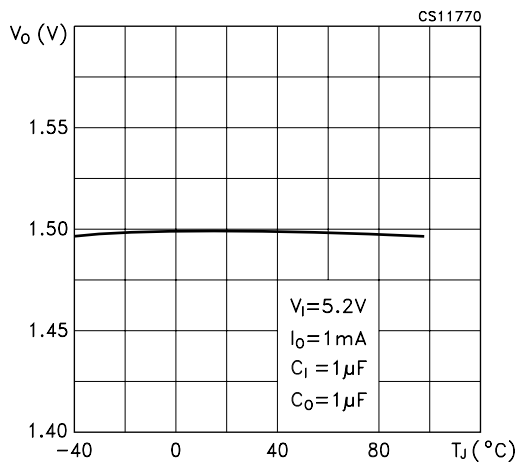


Figure 3 : Output Voltage vs Temperature

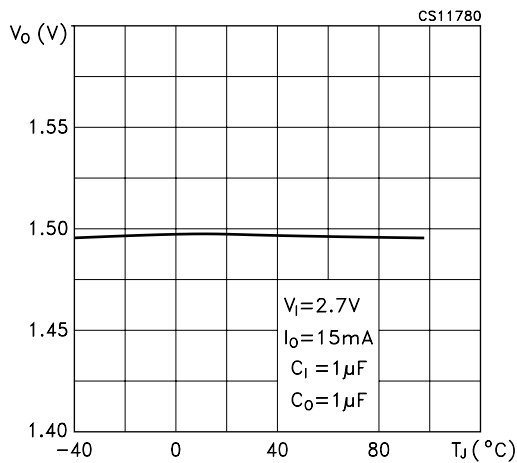


Figure 4 : Output Voltage vs Temperature

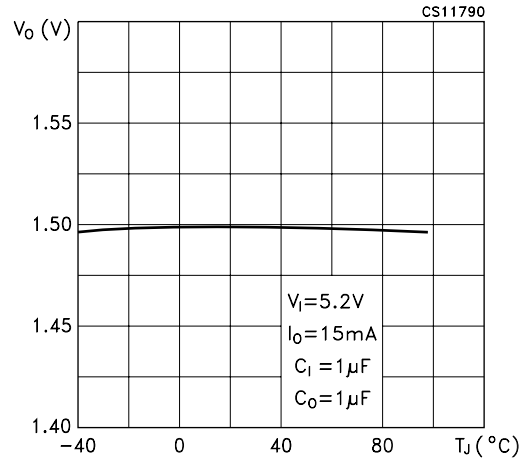


Figure 5 : Line Regulation vs Temperature

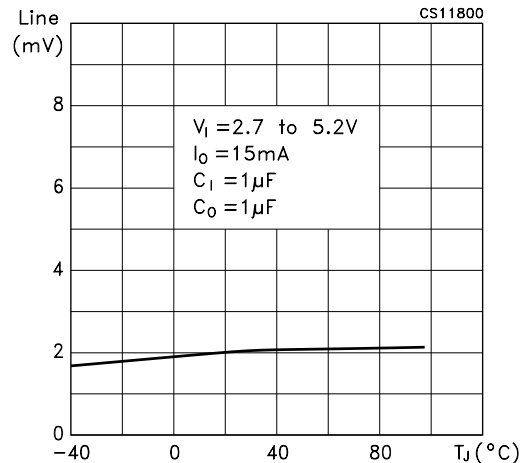


Figure 6 : Load Regulation vs Temperature

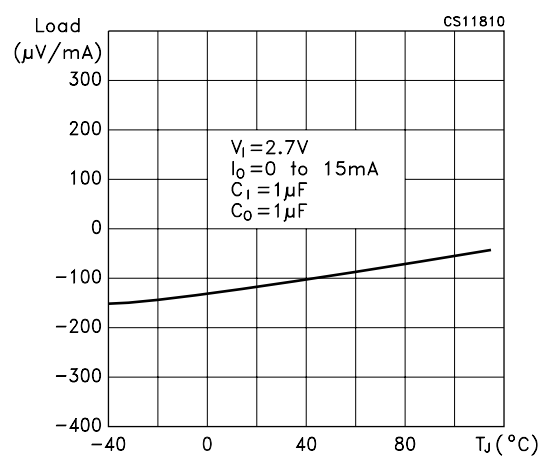


Figure 7 : Inhibit Threshold Voltage vs Temperature

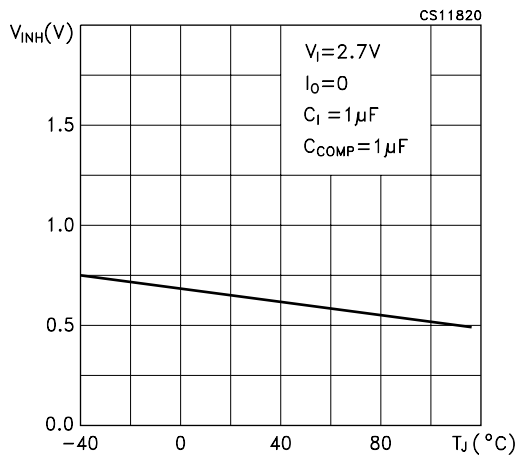


Figure 8 : Quiescent Current vs Temperature

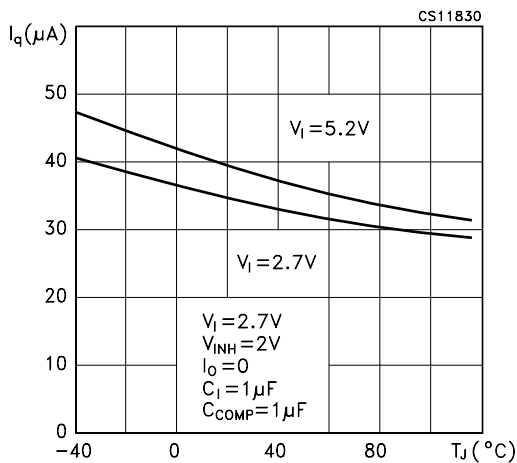


Figure 9 : Supply Voltage Rejection vs Temperature

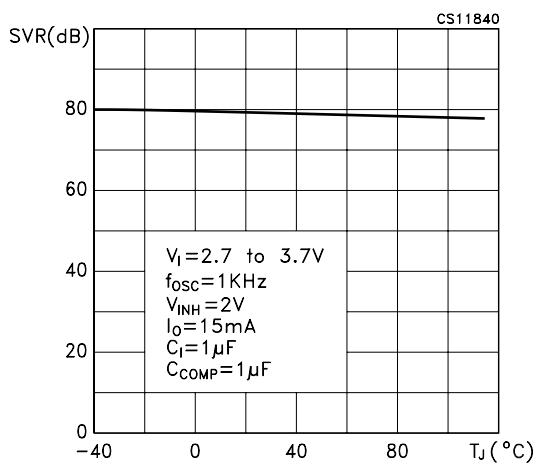


Figure 10 : Supply Voltage Rejection vs Output Current

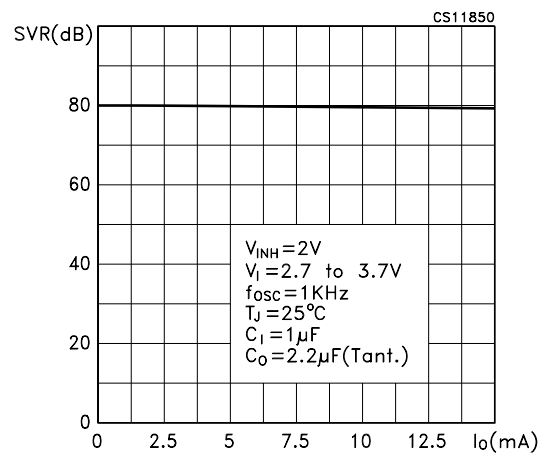


Figure 11 : Dynamic Precharge Mode

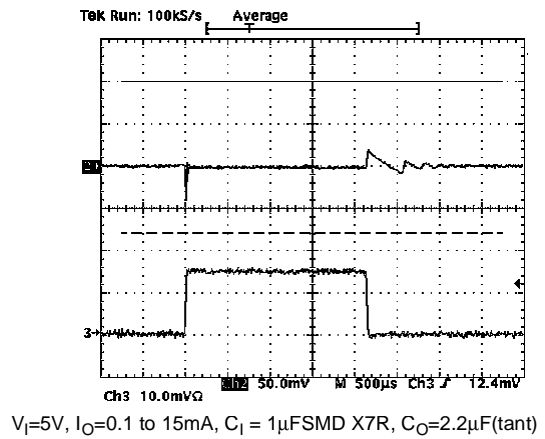


Figure 12 : Dynamic Precharge Mode

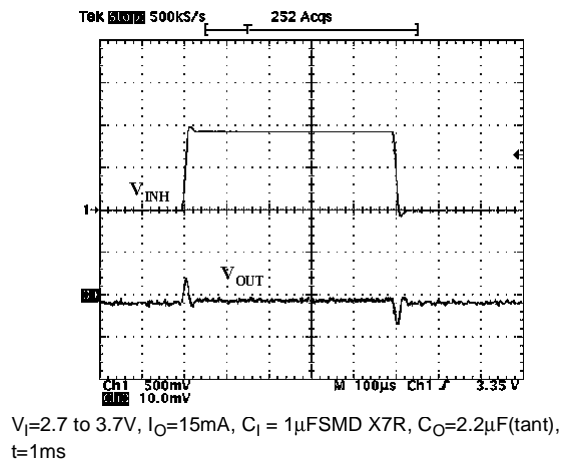
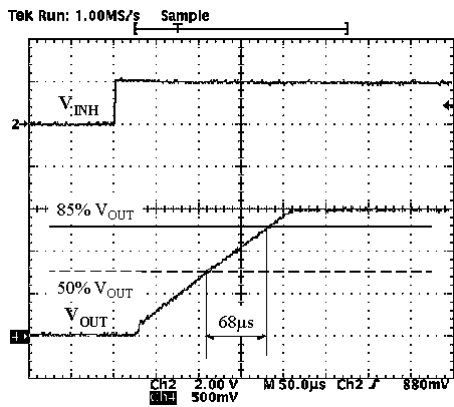
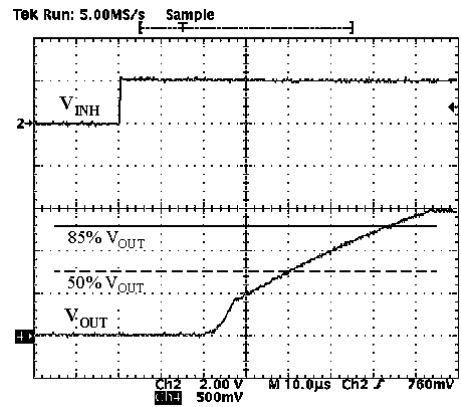


Figure 13 : Dynamic Precharge Mode



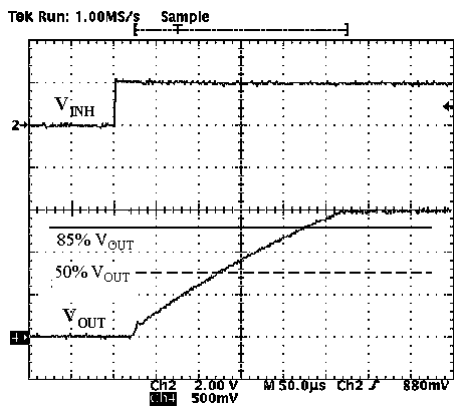
$V_{INH}=0$ to 2V, No load, $C_1 = 1\mu\text{FSMD X7R}$, $C_O=2.2\mu\text{F(tant)}$

Figure 15 : Dynamic Precharge Mode



$V_{INH}=0$ to 2V, $I_O=15\text{mA}$, $C_1 = 1\mu\text{FSMD X7R}$, $C_O=1\mu\text{F(tant)}$

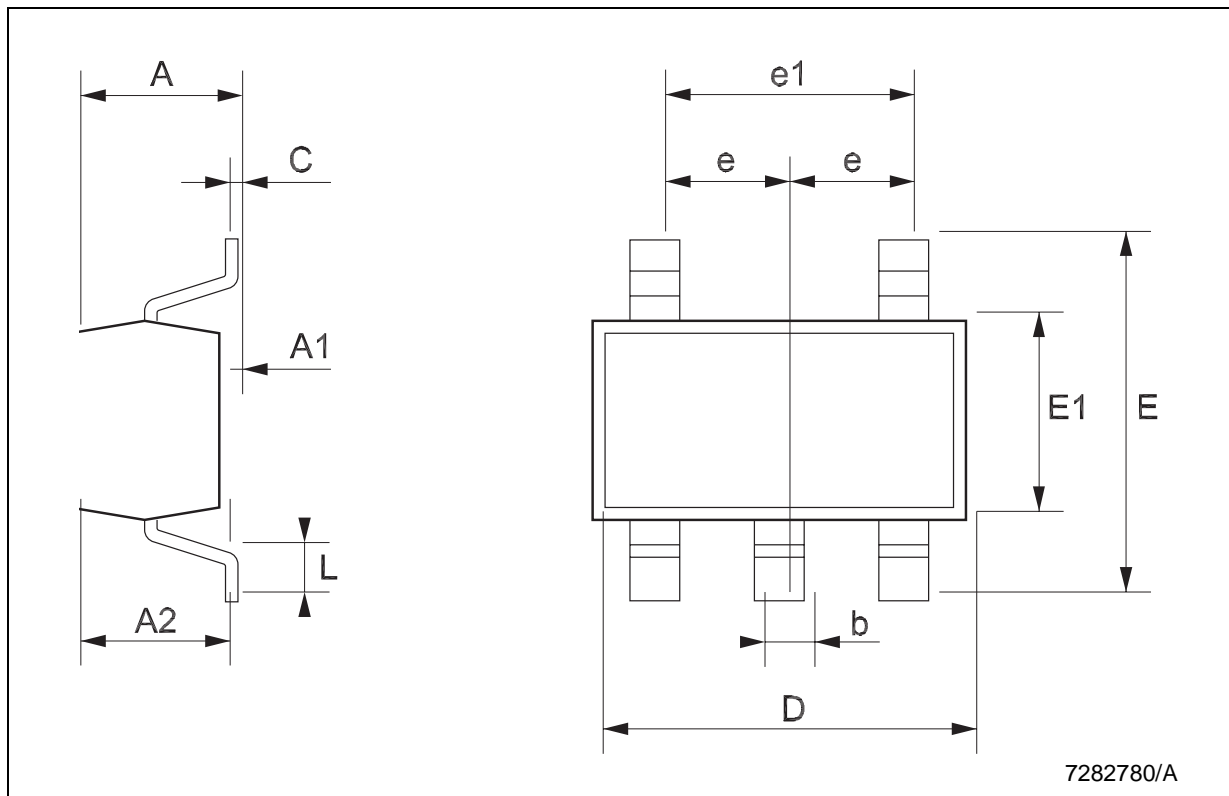
Figure 14 : Dynamic Precharge Mode



$V_{INH}=0$ to 2V, $I_O=15\text{mA}$, $C_1 = 1\mu\text{FSMD X7R}$, $C_O=2.2\mu\text{F(tant)}$

| |
|----------------------------------|
| TSOT23-5L MECHANICAL DATA |
|----------------------------------|

| DIM. | mm. | | | mils | | |
|------|------|------|------|------|-------|------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.1 | | | 43.3 |
| A1 | 0 | | 0.1 | | | 3.9 |
| A2 | 0.7 | | 1.0 | 27.6 | | 39.4 |
| b | 0.3 | | 0.5 | 11.8 | | 19.7 |
| C | 0.08 | | 0.2 | 3.1 | | 7.9 |
| D | | 2.9 | | | 114.2 | |
| E | | 2.8 | | | 110.2 | |
| E1 | | 1.6 | | | 63.0 | |
| e | 0 | .95 | | | 37.4 | |
| e1 | | 1.9 | | | 74.8 | |
| L | 0.3 | | 0.6 | 11.8 | | 23.6 |



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