



# VB125ASP

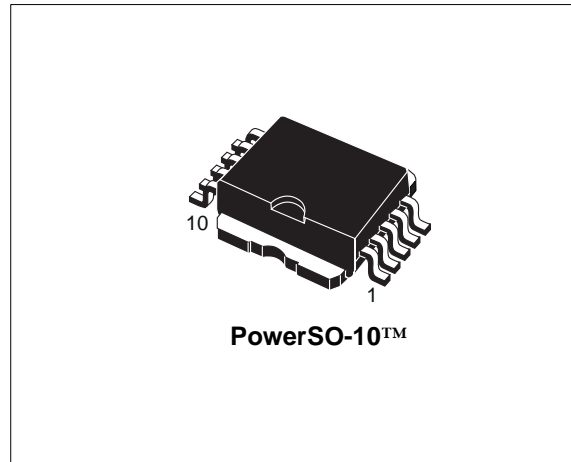
## HIGH VOLTAGE IGNITION COIL DRIVER POWER I.C.

TYPE	V <sub>cl</sub>	I <sub>cl</sub>	I <sub>CC</sub>
VB125ASP	340V	11.1A	200mA

- PRIMARY COIL VOLTAGE INTERNALLY SET
- COIL CURRENT LIMIT INTERNALLY SET
- LOGIC LEVEL COMPATIBLE INPUT
- BATTERY OPERATION
- SINGLE FLAG-ON COIL CURRENT
- TEMPERATURE COMPENSATED HIGH VOLTAGE CLAMP

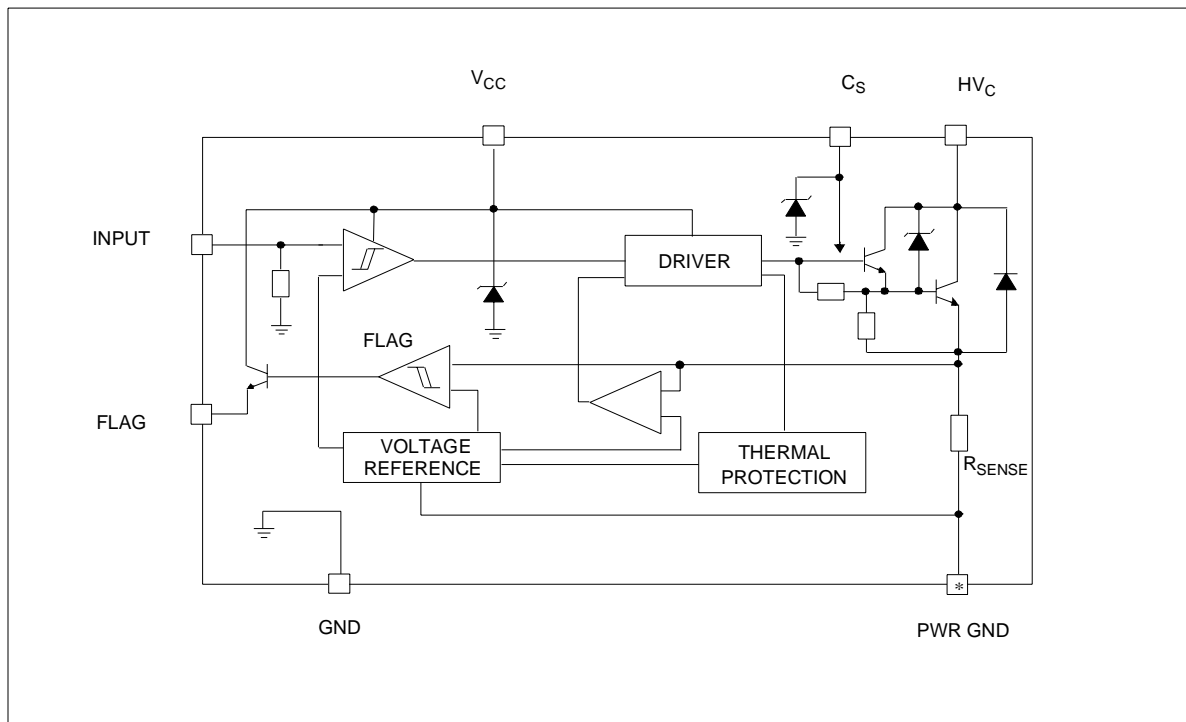
### DESCRIPTION

The VB125ASP is a high voltage power integrated circuit made using the STMicroelectronics VIPower™ M1-2 technology, with vertical current flow power darlington and logic level compatible driving circuit. The VB125ASP can be directly biased by using the 12V battery voltage, thus avoiding to use a low voltage regulator. It has



built-in protection circuit for coil current limiting and collector voltage clamping. It is suitable as smart, high voltage, high current interface in advanced electronic ignition system.

### BLOCK DIAGRAM



(\*) Pins 1...5

## VB125ASP

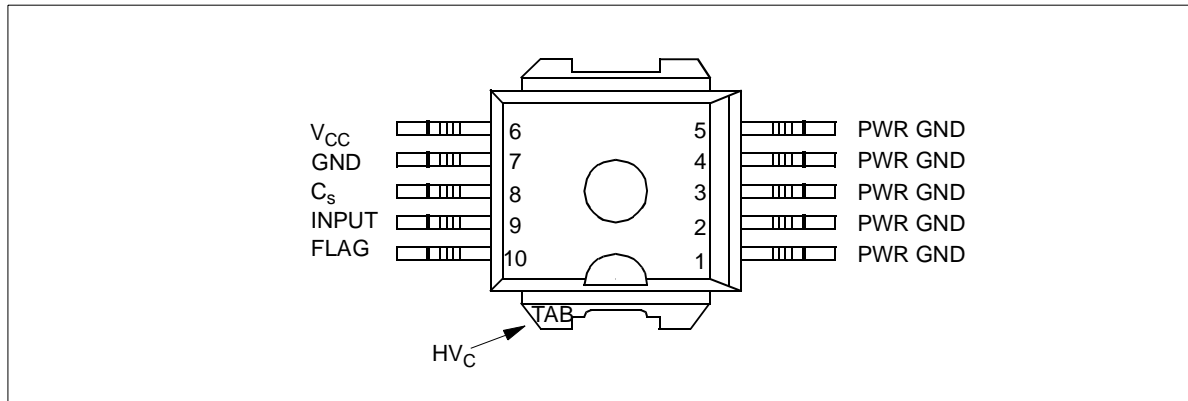
### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
$HV_C$	Collector voltage (Internally limited)	-0.3 to $V_{cl}$	V
$I_C$	Collector current (Internally limited)	11.1	A
$V_{CC}$	Driving stage supply voltage	-0.2 to 40	V
$I_{CC}$	Driving circuitry supply current	400	mA
$I_S$	Logic circuitry supply current	100	mA
$V_{IN}$	Input voltage	-0.3 to 6	V
$P_{tot}$	Power dissipation at $T_C \leq 25^\circ\text{C}$	100	W
$V_{ESD}$	ESD Voltage ( $HV_C$ pin)	-4 to 4	KV
$V_{ESD}$	ESD Voltage (other pin)	-2 to 2	KV
$T_j$	Junction operating temperature	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	1.2	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	62.5	$^\circ\text{C}/\text{W}$

### CONNECTION DIAGRAM (TOP VIEW)



### PIN FUNCTION

No	Name	Function
1÷5	PWR GND	Emitter power ground
6	$V_{CC}$	Logic supply voltage
7	GND	Control ground (*)
8	$C_s$	Logic level supply voltage filter capacitor
9	INPUT	Logic input channel
10	FLAG	Diagnostic output signal
TAB	$HV_C$	Primary coil output driver

(\*) Pin 7 must be connected to pins 1÷5 externally.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=6$  to  $24V$ ;  $-40^{\circ}C < T_j < 125^{\circ}C$ ;  $R_{coil}=400$  to  $700m\Omega$ ;  $L_{coil}=2$  to  $6mH$  unless otherwise specified; see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{cl}$	High voltage clamp	$I_C=7A$ ; (See note 2)	340	370	400	V
		$I_C=2A$ ; (Switching off from 7A)	300		400	V
$V_{cg(sat)}$	Power stage saturation voltage	$I_C=6A$ ; $V_{CC}=14V$ ; $V_{IN}=4V$			2	V
		$I_C=7A$ ; $V_{CC}=14V$ ; $V_{IN}=4V$ (See note 3)			3	V
$I_{CC(off)}$	Power-off supply current	$V_{IN}=0.4V$ ; $V_{CC}=14V$			20	mA
		$V_{IN}=0.4V$ ; $V_{CC}=24V$ (See note 4;5)			80	mA
$I_{CC(on)}$	Power-on supply current	$V_{IN}=4V$ ; $V_{CC}<14V$ ; $I_C=4A$			200	mA
		$V_{IN}=4V$ ; $V_{CC}=24V$ ; $I_C=4A$ (See note 4; 5)			300	mA
$I_{cl}$	Collector current limit	$V_{IN}=4V$ ; $10V < V_{CC} < 19V$ (See note 6; 7)	8.8		11.1	A
$V_{INH}$	High level input voltage		4			V
$V_{INL}$	Low level input voltage				0.8	V
$V_{IN(hyst)}$	Hysteresis input voltage		0.4			V
$I_{INH}$	High level input current	$V_{IN}=4V$	10		150	$\mu A$
$I_{INL}$	Low level input current	$V_{IN}=0.8V$	0		30	$\mu A$
$V_{diagH}$	High level diagnostic output voltage	$R_{EXT}=22K\Omega$ ; $C_{EXT}=1nF$ (See note 8)	3.5		5.5	V
$V_{diagL}$	Low level diagnostic output voltage	$R_{EXT}=22K\Omega$ ; $C_{EXT}=1nF$ (See note 8)			0.5	V
$I_{C(diag)}$	Threshold level collector current	$T_j=-40^{\circ}C$ ; $10V < V_{CC} < 19V$	5.45		6.8	A
		$T_j=25^{\circ}C$ ; $10V < V_{CC} < 19V$	5.55		6.35	A
		$T_j=125^{\circ}C$ ; $10V < V_{CC} < 19V$ (See note 7; 9 and fig. 5)	5.5		6.35	A
$I_{C(diag)}$	Threshold level collector current	$T_j=-40^{\circ}C$ ; $V_{CC}=7V$	5.9		6.6	A
		$T_j=25^{\circ}C$ ; $V_{CC}=7V$	5.7		6.3	A
		$T_j=125^{\circ}C$ ; $V_{CC}=7V$ (See note 7; 9 and fig. 5)	5.5		6.3	A
$I_{diag}$	High level flag output current	$I_C > I_{C(diag)}$ (See note 7)	0.5			mA
$I_{diag(leak)}$	Leakage current on flag output	$V_{IN}=LOW$			10	$\mu A$
$V_f$	Diode forward voltage	$I_f=10A$			3.5	V
$E_{s/b}$	Single pulse avalanche energy		300			mJ
$T_j$	Thermal output current control	IN=ON (See note 10)	150			$^{\circ}C$
$t_{d(on)}$	Turn-on delay time of output current	(See note 11)		1		$\mu s$
$t_{d(off)}$	Turn-off delay time of output current	(See note 12)	7		60	$\mu s$

## VB125ASP

**NOTE 1:** Only functionality is guaranteed with  $6V < V_{CC} < 10V$  and  $V_{CC} > 24V$  and not parameter values.

**NOTE 2:** In the high voltage clamping structure of this device a temperature compensation has been implemented. The circuit schematic is shown in fig. 1. The KVbe cell takes care of the temperature compensation. The whole electrical characteristic of the new circuit is shown in fig. 2. Up to  $V_{CE} = nV_Z$  no current will flow into the collector (just the leakage current of the power stage); for  $nV_Z < V_{CE} < V_{CL}$  a current begins to flow across the resistances of the KVbe compensation circuit (typical slope  $\approx 20 \text{ K}\Omega$ ) as soon as the  $V_{CL}$  reached the dynamic resistance drop to  $\sim 4\Omega$  to protect the device against overvoltage (See figure 3).

**NOTE 3:** The saturation voltage of the Power stage includes the drop on the sensing resistor.

**NOTE 4:** Considering the different ways of operation of the device (with or without spark, etc...) there are some short periods of time in which the output terminal ( $HV_C$ ) is pulled below ground by a negative current due to leakage inductances and stray capacitances of the ignition coil. With VIPower devices, if no corrective action is taken, these negative currents can cause parasitic glitches on the diagnostic output. To kill this potential problem, a circuit that avoids the possibility for the  $HV_C$  to be pulled underground, by sending the required negative current from the battery is implemented in the VB125ASP. For this reason there are some short periods in which a current exceeding 220 mA flows in the  $V_{CC}$  pin.

**NOTE 5:** A zener protection of 16V (typical) is placed on the supply pin ( $V_{CC}$ ) of the chip to protect the internal circuitry. For this reason, when the battery voltage exceeds that value, the current flowing into  $V_{CC}$  pin can be greater than the maximum current specified at  $V_{CC} = 14V$  (both in power on and power off conditions): it will be limited by an internal resistor.

**NOTE 6:** The primary coil current value  $I_{cl}$  must be measured 1 ms after desaturation of the power stage.

**NOTE 7:** These limits apply with regard to the minimum battery voltage and resistive drop on the coil and cables that permit to reach the limitation or diagnostic level.

**NOTE 8:** No internal Pull-Down.

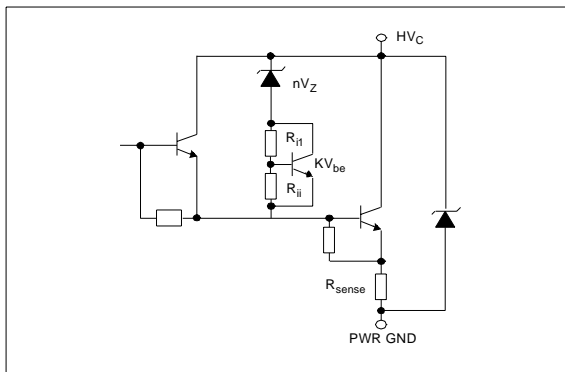
**NOTE 9:** When  $I_C$  gets over  $I_{C(diag)}$ , the diagnostic output voltage rises to the high level and so it remains until the end of the input signal.

**NOTE 10:**  $T_{jmin} = 150^\circ\text{C}$  means that the behavior of the device will not be affected for junction temperature lower than  $150^\circ\text{C}$ . For higher temperature, the thermal protection circuit will begin its action reducing the  $I_{cl}$  limit according with the power dissipation. Chip temperature is a function of the  $R_{th}$  of the whole system in which the device will be operating (See Fig.4).

**NOTE 11:** Turn on delay time measured from 90% of input voltage rising edge to 10% of output voltage falling edge.

**NOTE 12:** Turn off delay time is defined as the time between the 90% of input pulse falling edge and the point where the  $HV_C$  reaches 200V.

**FIGURE 1:** Temperature compensated high voltage clamp



**FIGURE 2:** Electrical characteristic of the circuit shown in Figure 1.

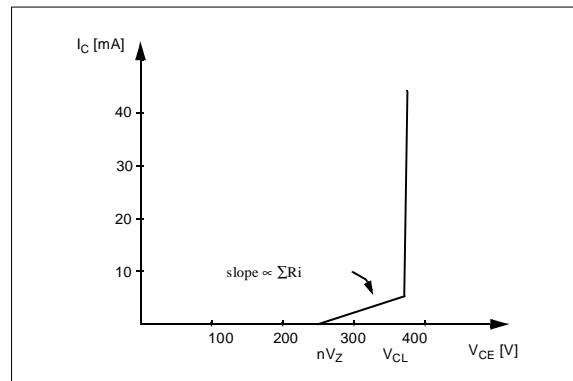


FIGURE 3:  $V_{cl}$  with load  $L=4mH$

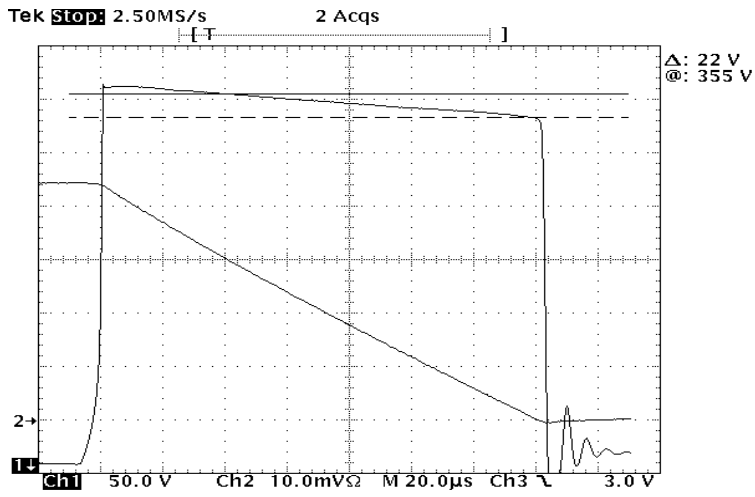
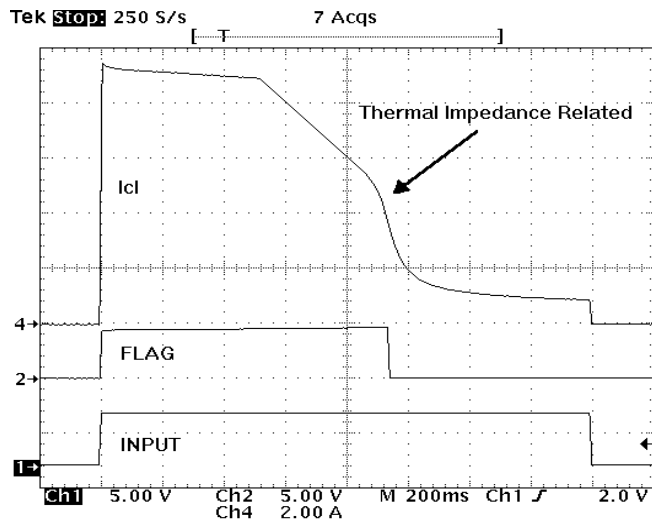
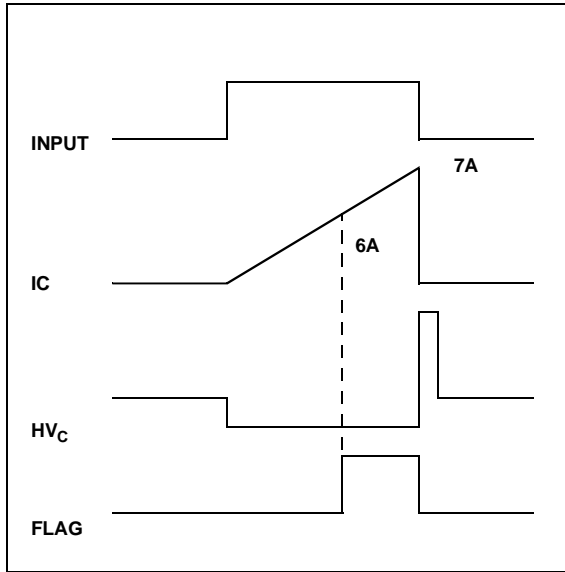


FIGURE 4: Output Current Waveform after Thermal Protection Activation.

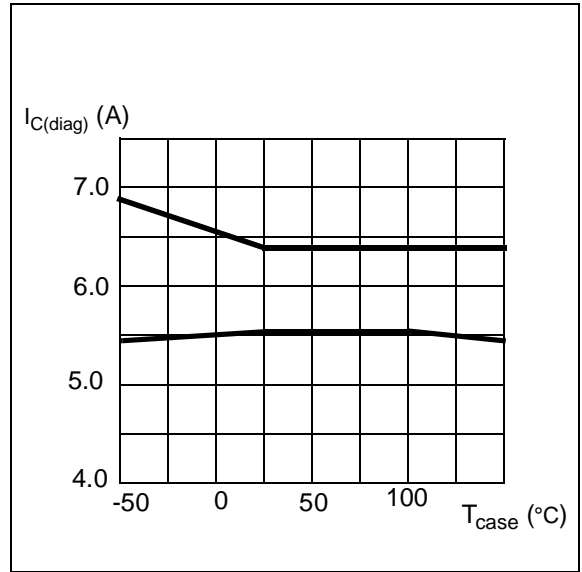


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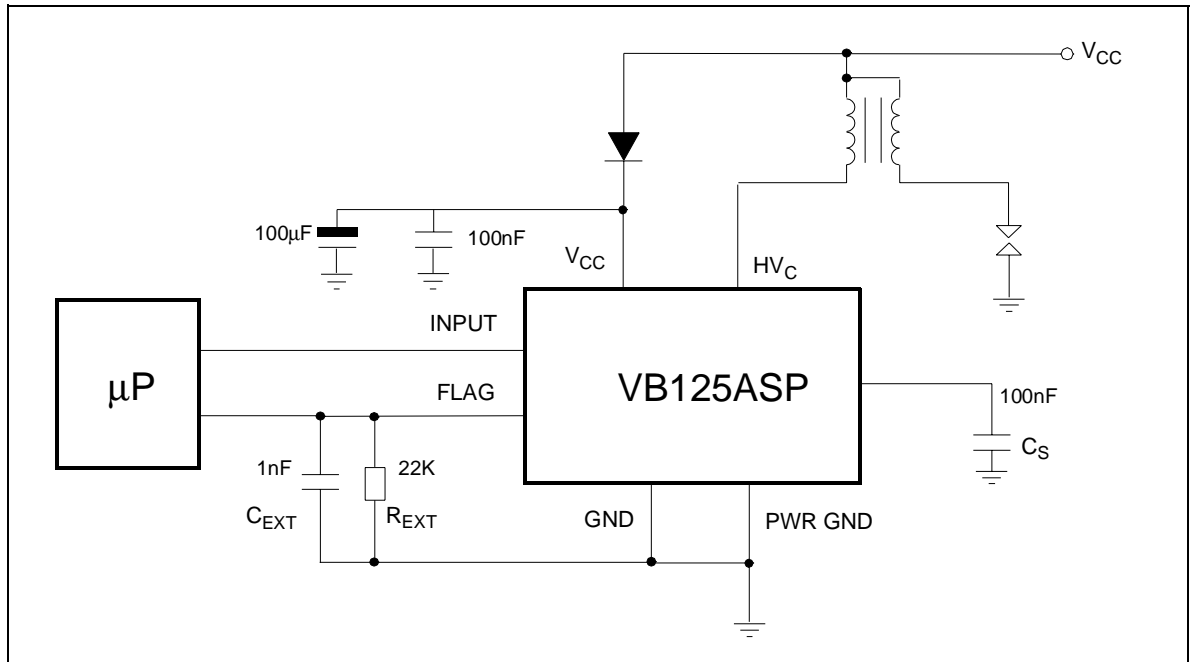
**FIGURE 5: Waveforms**



**FIGURE 6: Threshold Collector Current Vs Temperature**



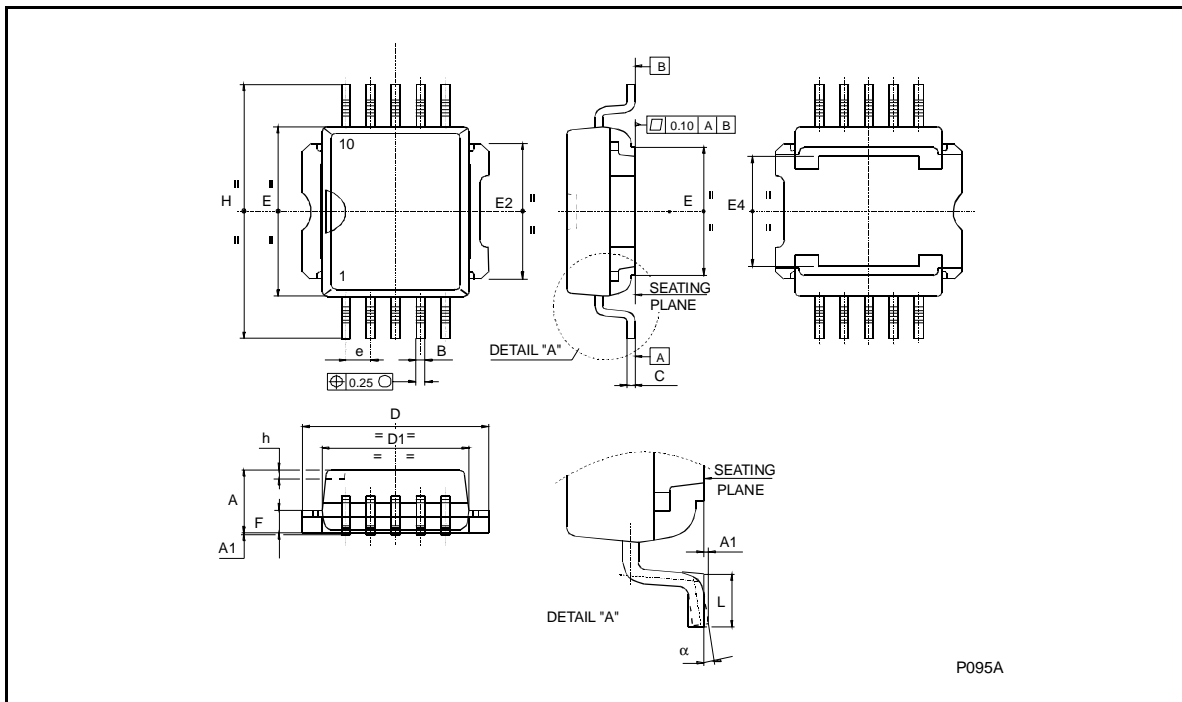
**FIGURE 7: Application Circuit**



**PowerSO-10™ MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

(\*) Muar only POA P013P



# VB125ASP

## PowerSO-10™ SUGGESTED PAD LAYOUT



## TUBE SHIPMENT (no suffix)

**CASABLANCA**

**MUAR**

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
<b>Casablanca</b>	50	1000	532	10.4	16.4	0.8
<b>Muar</b>	50	1000	532	4.9	17.2	0.8

## TAPE AND REEL SHIPMENT (suffix "13TR")

### REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

### TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

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