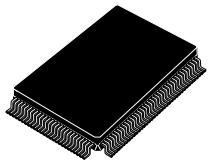
STE1000P

SINGLE PORT GIGABIT ETHERNET TRANSCEIVER

PRODUCT PREVIEW

1 GENERAL DESCRIPTION

The STE1000P designed by STMicroelectronics, is a high performance, ultra low power, single port transceiver that performs all the physical layer interface functions for Gigabit Ethernet over 100-meter CAT 5 cabling. It also provides 100BASE-TX and 10BASE-T Ethernet capabilities, which enables a smooth migration from current 10/100 networks to 1000Mbps-based networks.



Package Options: PQFP128
Ordering Part Number: STE1000P

2 MAIN FEATURES

- Fully standards compliant: IEEE 802.3, IEEE 802.3u, IEEE 802.3z and IEEE 802.3ab
- Six different operating modes
  - 1000BASE-T Full Duplex and 1000BASE-T Half Duplex
  - 100BASE-TX Full Duplex and 100BASE-TX Half Duplex
  - 10BASE-T Full Duplex and 10BASE-T Half Duplex
- BER of better than or equal to 10^{-10} in 1000BASE-T mode, 10^{-8} in 100BASE-TX mode.
- Configurable MAC interface: MII, GMII or TBI
- Automatic configure operating mode and MAC interface
- Hardware configuration for default operation
- Automatic detection and correction of pair swaps (Auto-MDIX), pair skew and pair polarity
- Management interface
- Management interrupt
- Baseline wander compensation
- On-chip transmit wave-shaping
- On-chip hybrid circuit
- 10KB jumbo frames
- Internal, external and remote loop back
- LED indication: link mode, status, speed, activity, and collision
- Power down mode
- JTAG (IEEE 1149.1) interface

2.1 OPERATING CONDITIONS

- Supply voltage: 1.8V for core, 3.3V for I/O
- Temperature range: 0-85^{o} C
- Power consumption: 600mW (typical)

3 TYPICAL APPLICATIONS

- Ethernet Switches
- Hubs/Repeaters
- Up-link Interfaces
- Network Interface Cards (NICs)
- LAN on Mother board (LOM)

4 FUNCTIONAL DESCRIPTION

The STE1000P chip consists of 8 functional blocks:

- Auto-Negotiation block, which is responsible for advertising the chip's capabilities and establishing the link.
- Management Register block, which contains all the configuration registers
- Management Data Interface
- Physical Coding Sublayer block, which contains the 1000/100/10 Base T sub-blocks
- Mac Interface.
- DPMA: Digital Physical Media Attachment, which consists of 1000/100/10 Base T sub-blocks:
- Clock Distribution and Reset circuitry.
- LED: Light Emitting Diodes circuitry.

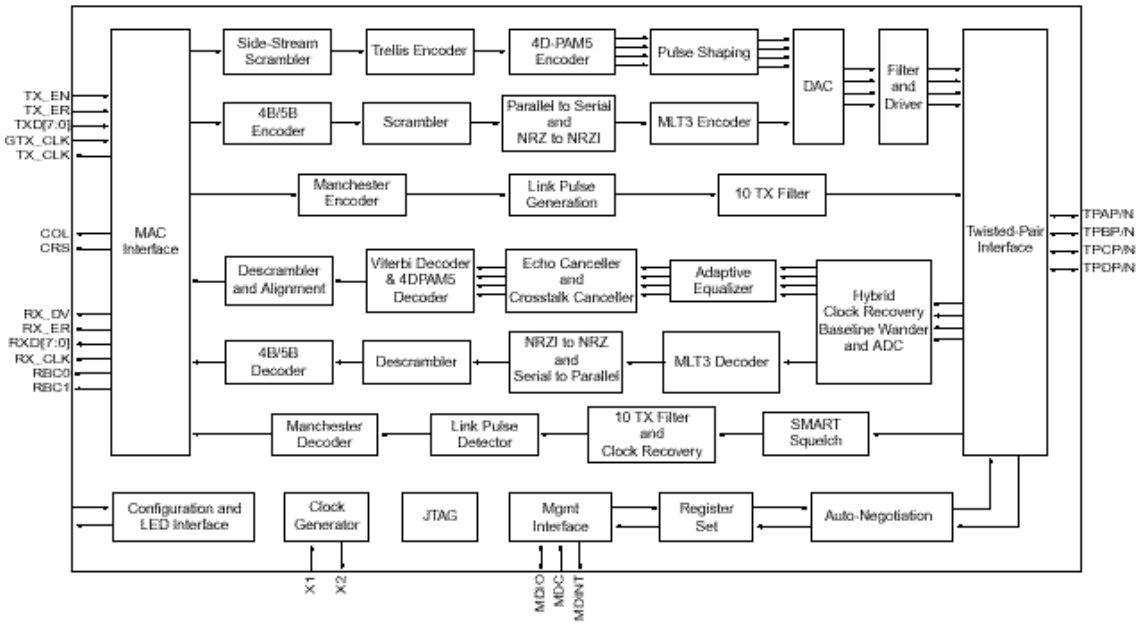


Figure 1: STE1000P Block Diagram