HARRIS
SEMICONDUCTOR

HGTG34N100E2

April 1995

34A, 1000V N-Channel IGBT

Features

- **34A, 1000V**
- **Latch Free Operation**
- **Typical Fall Time - 710ns**
- **High Input Impedance**
- **Low Conduction Loss**

Description

The HGTG34N100E2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

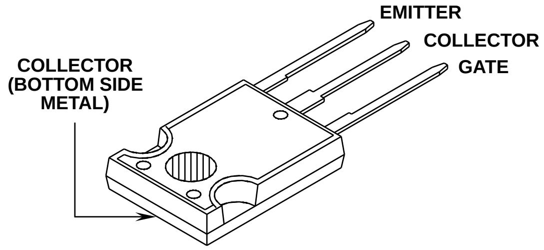
PART NUMBER	PACKAGE	BRAND
HGTG34N100E2	TO-247	G34N100E2

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA9895.

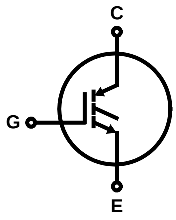
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTG34N100E2	UNITS
Collector-Emitter Voltage	BV_{CES}	1000	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	V_{CGR}	1000	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	55	A
at $V_{GE} = 15V$, at $T_C = +90^oC$	I_{C90}	34	A
Collector Current Pulsed (Note 1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = +150^oC$	SSOA	200A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25^oC$	P_D	208	W
Power Dissipation Derating $T_C > +25^oC$		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	3	µs
at $V_{GE} = 10V$	t_{SC}	10	µs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)} = 600V$, $T_C = +125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		1000	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	1.0	mA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	2.8	3.2	V
			$T_C = +125^oC$	-	2.8	3.1	V
		$I_C = I_{C90}$, $V_{GE} = 10V$	$T_C = +25^oC$	-	2.9	3.3	V
			$T_C = +125^oC$	-	3.0	3.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	185	240	nC
			$V_{GE} = 20V$	-	240	315	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	610	795	ns
Current Fall Time	t_{FI}			-	710	925	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	7.1	-	mJ
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 10V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off	$t_{D(OFF)I}$			-	460	600	ns
Current Fall Time	t_{FI}			-	670	870	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	6.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	$^oC/W$

NOTE: 1. Turn-Off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG34N100E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

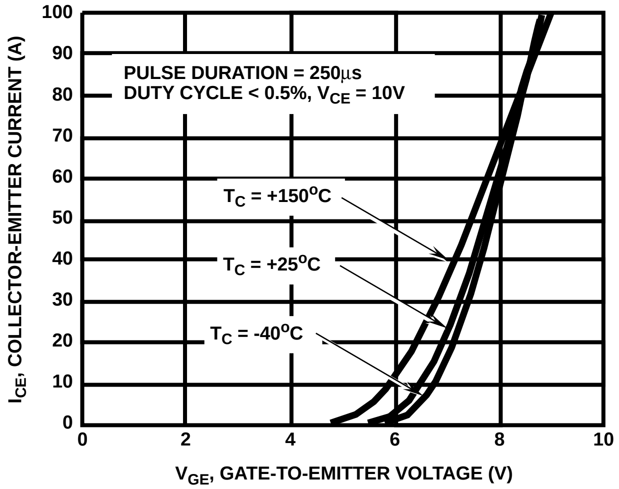


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

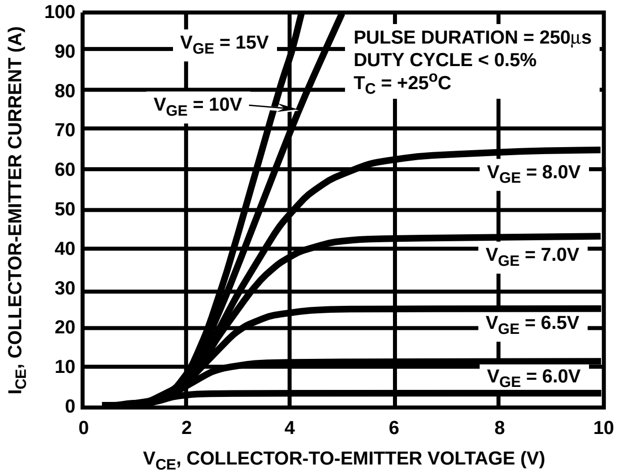


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

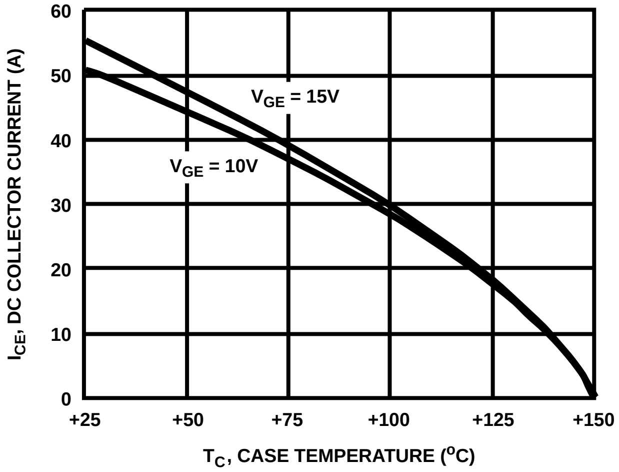


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

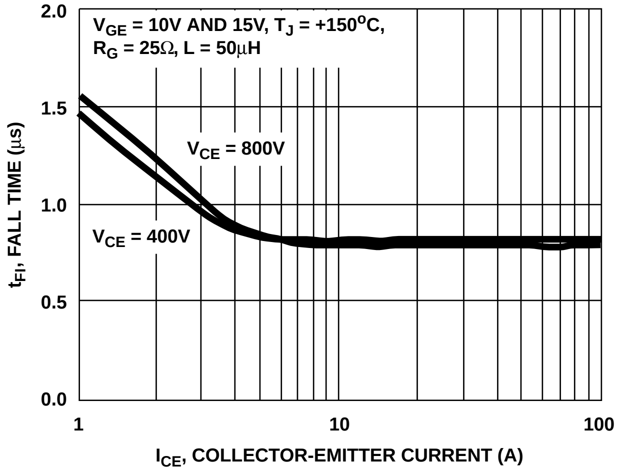


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

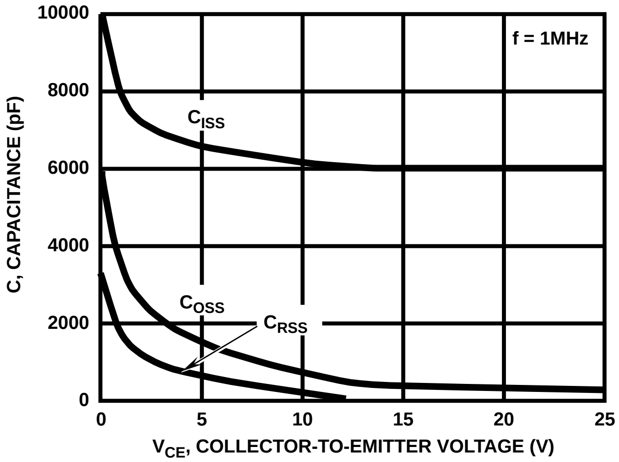


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

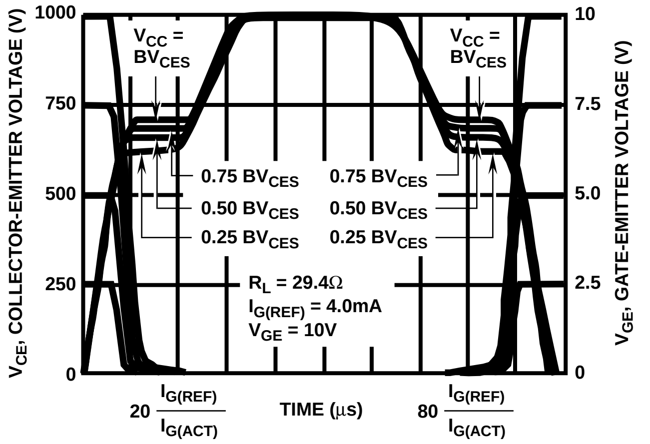


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

Typical Performance Curves (Continued)

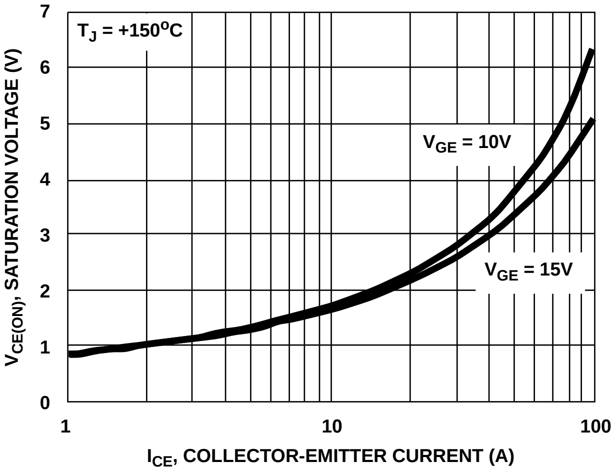


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

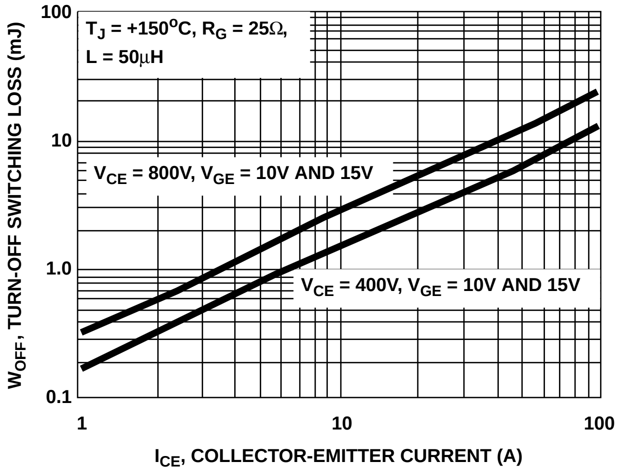


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

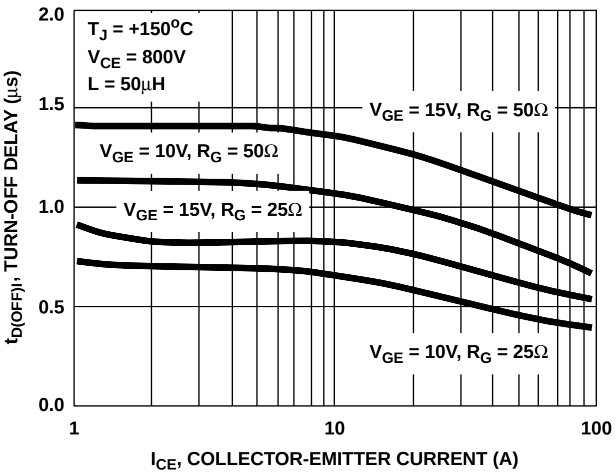
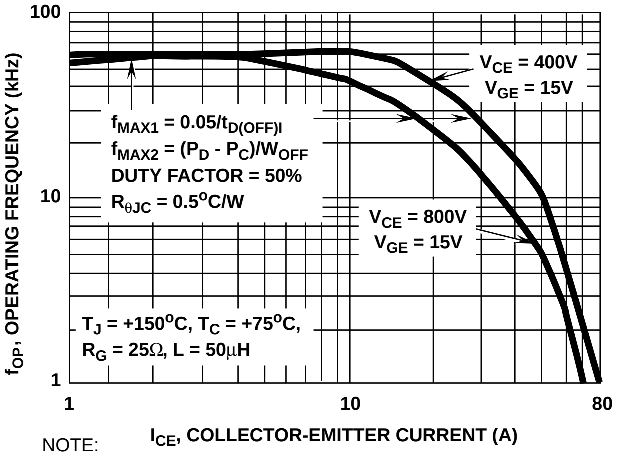


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

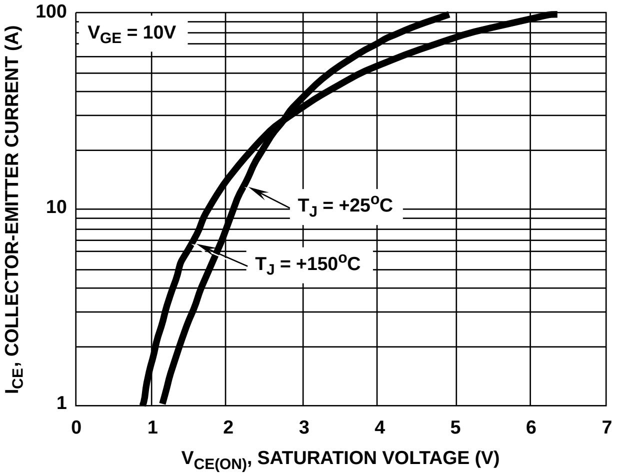


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLTAGE

Test Circuit

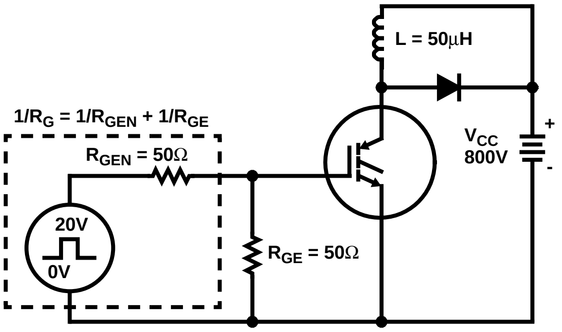


FIGURE 12. INDUCTION SWITCHING TEST CIRCUIT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.