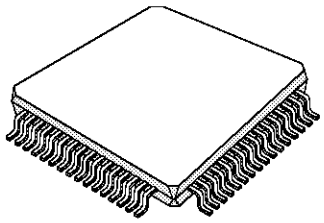
SGS-THOMSON MICROELECTRONICS

STV0030

SATELLITE SOUND AND VIDEO PROCESSOR

- TWO INDEPENDENTLY PROGAMMABLE SOUND DEMODULATORS
- PLL DEMODULATION WITH 5-9MHz FREQUENCY SYNTHESIS
- 50/75µs, J17 OR NO DE-EMPHASIS PROGRAMMABLE OPTIONS
- DYNAMIC NOISE REDUCTION SYSTEM
- FIXED LEVEL AUXILIARY AUDIO INPUTS AND OUTPUTS
- VOLUME CONTROLLED AND MUTEABLE AUDIO OUTPUTS
- COMPOSITE VIDEO 6-BIT GAIN CONTROL
- COMPOSITE VIDEO SELECTABLE INVERTER
- COMPOSITE VIDEO DEEMPHASIS AMPLIFIER
- 9 x 5 VIDEO MATRIX AND SWITCHES WITH GRAPHICS INPUT
- 8-BIT DAC OUTPUT
- FULLY CONTROLLED VIA I^2C BUS
- TWO HARDWARE SELECTABLE ADDRESSES (06_{HEX} and 46_{HEX})



PQFP64
(Plastic Package)

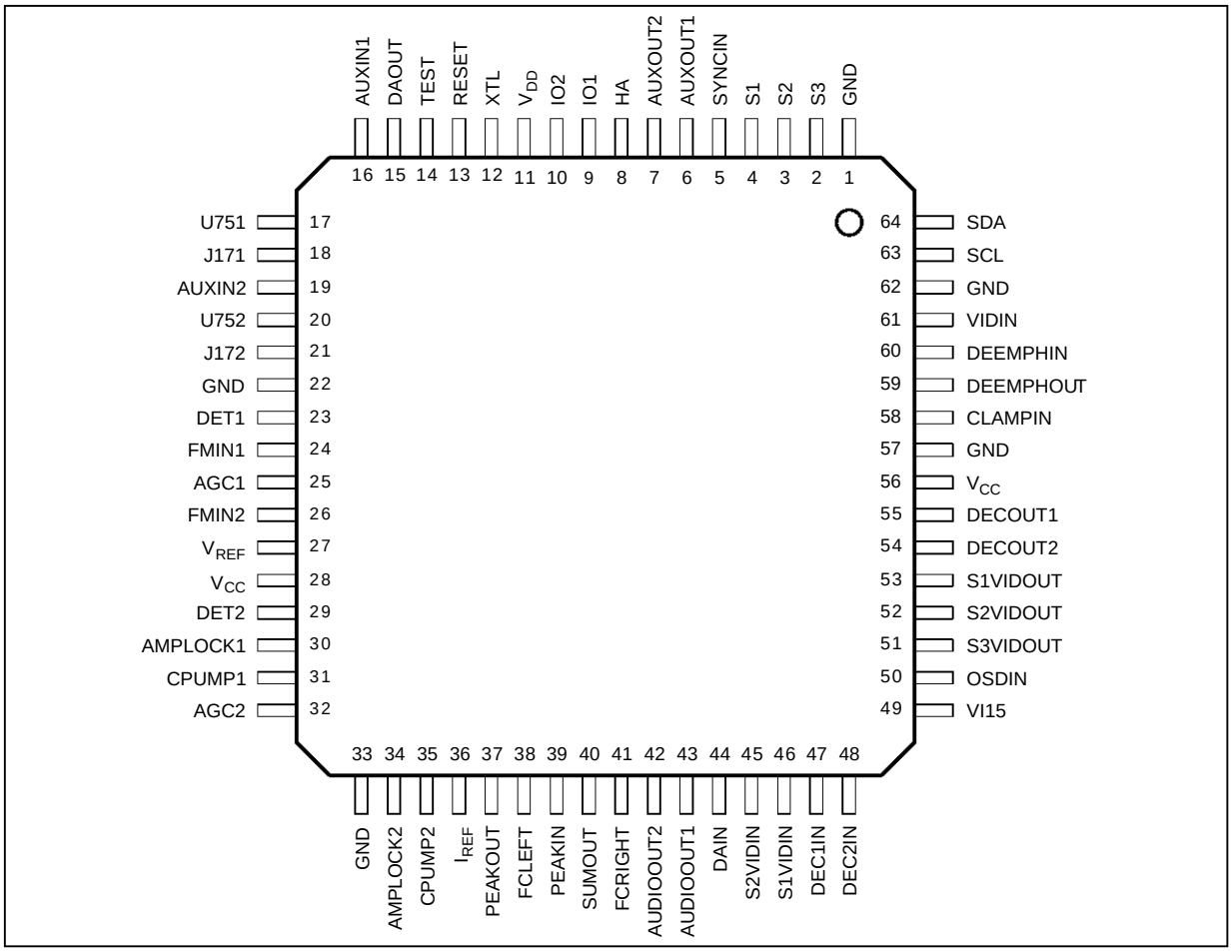
ORDER CODE : STV0030

DESCRIPTION

The STV0030 is a BICMOS integrated circuit for use in satellite receivers. The great variety of FM deviations, energy dispersal and subcarrier standards makes the design of satellite receivers able to receive all programs a complex task. The device has been designed to specially adapt to all known conditions in analog video and radio transmissions.

The choice of the surface mounting PQFP64 package ensures optimisation of real-estate requirements.

PIN CONNECTIONS



PIN ASSIGNMENT

Pin	Name	Function
1	GND	Digital Power Ground
2	S3	SCART-3 Driver
3	S2	SCART-2 Driver
4	S1	SCART-1 Driver
5	SYNCIN	Digital or Analog Sync Signal Input
6	AUXOUT1	Fixed Level Audio Output Left
7	AUXOUT2	Fixed Level Audio Output Right
8	HA	Hardware Address
9	IO1	Digital Input/Output 1
10	IO2	Digital Input/Output 2
11	V_{DD}	Digital 5V Power Supply
12	XTL	4/8MHz Clock Input (optionally 4/8MHz Quartz Crystal)
13	RESET	System Reset
14	TEST	Test Pin
15	DAOUT	DAC Amplifier Output
16	AUXIN1	Auxilliary Audio Input Left
17	U751	75µs De-emphasis Time Constant Left

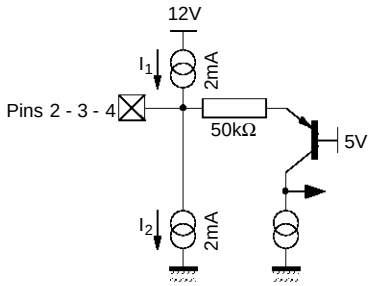
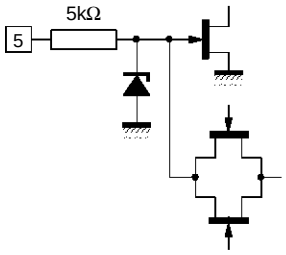
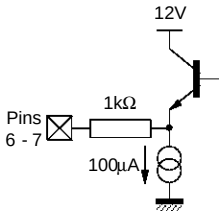
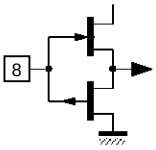
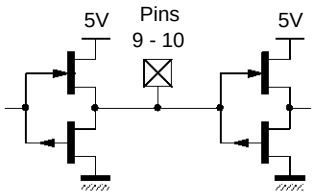
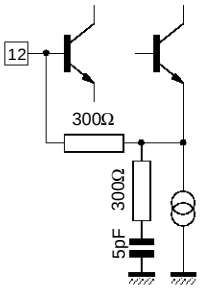
0030-01.TBL

PIN ASSIGNMENT

Pin	Name	Function
18	J171	J17 De-emphasis Time Constant Left
19	AUXIN2	Auxiliary Audio Input Right
20	U752	75µs De-emphasis Time Constant Right
21	J172	J17 De-emphasis Time Constant Right
22	GND	RF and Audio Ground
23	DET1	FM PLL Filter Left
24	FMIN1	FM Demodulator +ve Input
25	AGC1	AGC Peak Detect Capacitor Left
26	FMIN2	FM Demodulator -ve Input
27	V_{REF}	2.44V Reference
28	V_{CC}	Audio 12V Supply
29	DET2	FM PLL Filter Right
30	AMPLOCK1	Amplitude Detector Capacitor Left
31	CPUMP1	FM PLL Charge Pump Capacitor Left
32	AGC2	AGC Peak Detect Capacitor Right
33	GND	Ground for Volume Control ANRS, VCO
34	AMPLOCK2	Amplitude Detector Capacitor Right
35	CPUMP2	FM PLL Charge Pump Capacitor Right
36	I_{REF}	Current Reference Resistor
37	PEAKOUT	ANRS Peak Detector Capacitor
38	FCLEFT	Audio Roll-off Left
39	PEAKIN	ANRS Peak Detector Input
40	SUMOUT	ANRS Summing Output
41	FCRIGHT	Audio Roll-off Right
42	AUDIOOUT2	Level Controlled Audio Out Right
43	AUDIOOUT1	Level Controlled Audio Out Left
44	DAIN	Digital/Analog Converter Sense Input
45	S2VIDIN	External Video Input 2
46	S1VIDIN	External Video Input 1
47	DEC1IN	Decoder 1 Input (e.g. D2MAC)
48	DEC2IN	Decoder 2 Input (e.g. Videocrypt)
49	VI5	Clamped Video Input
50	OSDIN	On-screen Display Video Input
51	S3VIDOUT	SCART-3 Video Output (with OSD)
52	S2VIDOUT	SCART-2 Video Output (with OSD)
53	S1VIDOUT	SCART-1 Video Output (without OSD)
54	DECOUT2	Satellite Decoder Drive 2
55	DECOUT1	Satellite Decoder Drive 1
56	V_{CC}	Video 12V Supply
57	GND	Video Ground
58	CLAMPIN	Sync-tip Clamp Input
59	DEEMPHOUT	Video De-emphasis Output
60	DEEMPHIN	Video De-emphasis Input
61	VIDIN	Video Input Buffer
62	GND	Video Input Ground
63	SCL	I^2C Bus Clock
64	SDA	I^2C Bus Data

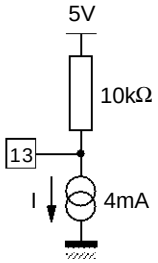
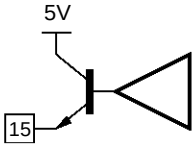
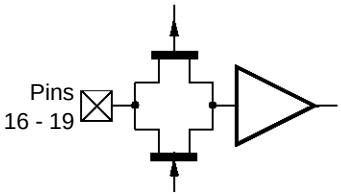
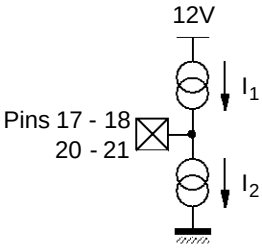
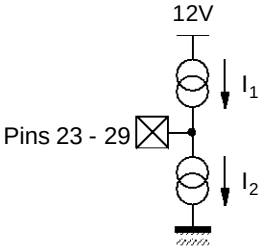
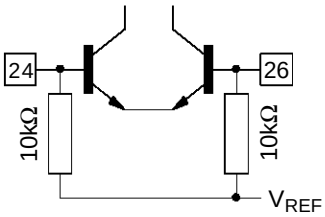
0030-02.TBL

INPUT/OUTPUT PIN CONNECTION

Pin N°	Circuitry	Comments
2 - 3 - 4	 0030-09.EPS	As an input I_1, I_2 off, $Z_{IN} \geq 10k\Omega$ As an output $V_{OUT} \leq 2V$ (L) I_1 : OFF, I_2 : ON $V_{OUT} \geq 9.5V$ (H) I_1 : ON, I_2 : OFF
5	 0030-10.EPS	
6 - 7	 0030-11.EPS	
8	 0030-12.EPS	Input with TTL compatible levels
9 - 10	 0030-13.EPS	Input/Output with TTL compatible levels
12	 0030-14.EPS	

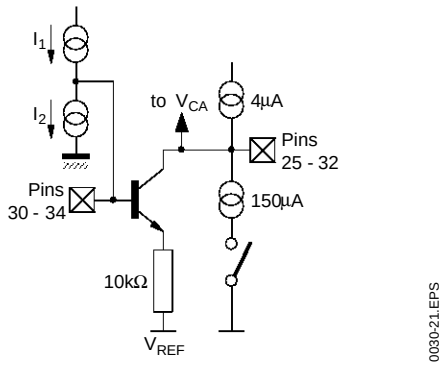
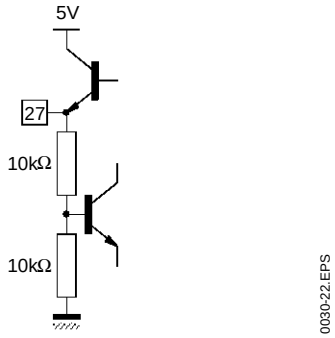
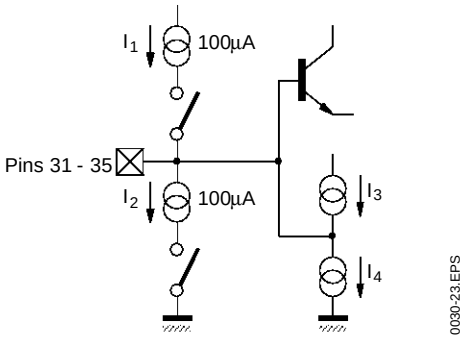
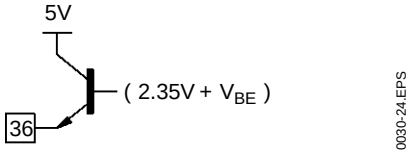
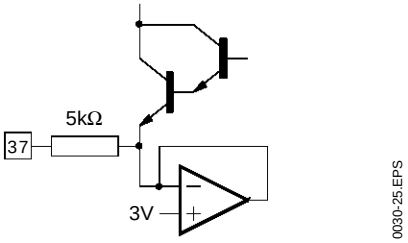
0030-09.TBL

INPUT/OUTPUT PIN CONNECTION (continued)

Pin N°	Circuitry	Comments
13	 0030-15.EPS	V_{13} : L Reset active (I : ON)
14		To be grounded
15	 0030-16.EPS	$I_{15\ (Max.)}$ = 2mA
16 - 19	 0030-17.EPS	To be externally DC biased to $V \cong V_{REF}$
17 - 18 20 - 21	 0030-18.EPS	$I_1 - I_2 = \frac{V_{AUD}}{18k}$
23 - 29	 0030-19.EPS	$I_1 - I_2 = f(\phi)$ ϕ : phase difference
24 - 26	 0030-20.EPS	Either Pin 24 or Pin 26 must be AC coupled to ground

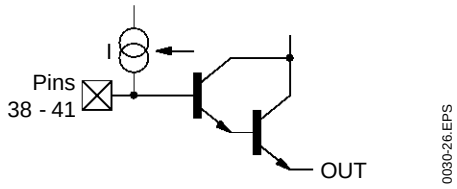
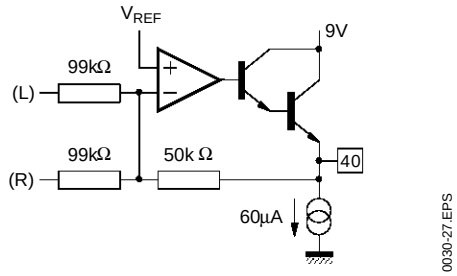
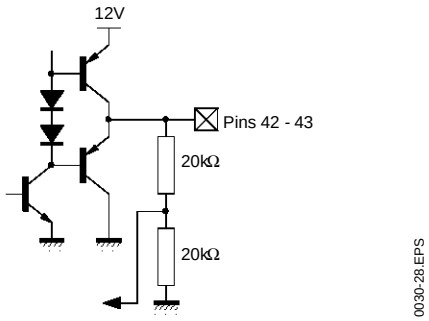
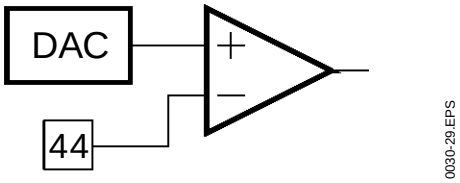
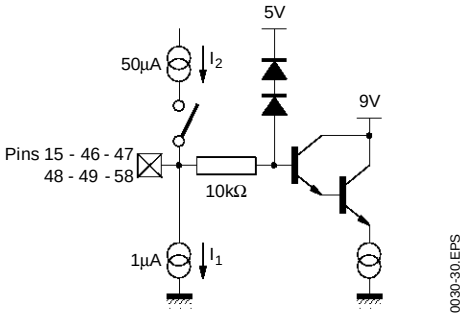
0030-10.TBL

INPUT/OUTPUT PIN CONNECTION (continued)

Pin N°	Circuitry	Comments
25- 32 30 - 34		I_1, I_2 current generator belong to the amplitude mixer
27		V_{DC} = 2.44V
31 - 35		Reg 6 b4 : H, then I_1, I_2 enabled. I_3, I_4 << I_1, I_2
36		Recommanded value at Pin 36 : 240kΩ
37		DC voltage = f (audio amplitude)

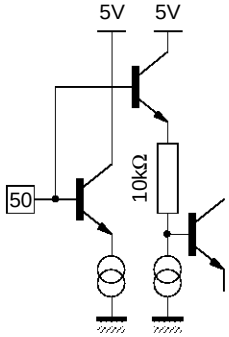
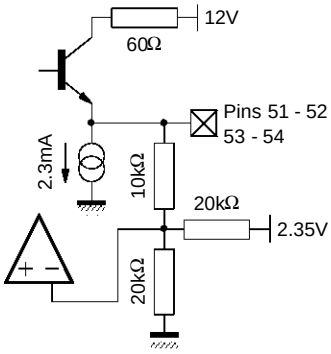
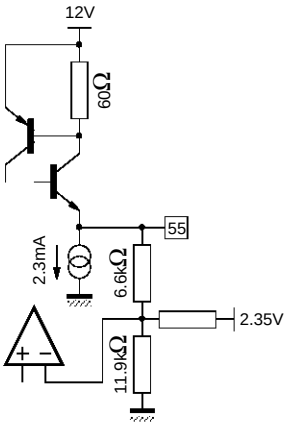
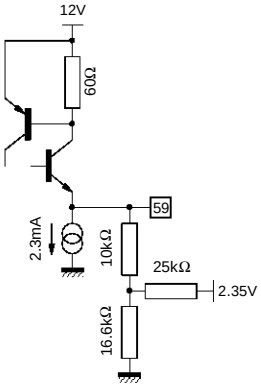
0030-11.TBL

INPUT/OUTPUT PIN CONNECTION (continued)

Pin N°	Circuitry	Comments
38 - 41		I controlled by the amplitude of the audio signal ; $I = f(V_{37})$
40		$V_{OUT\ DC}$ = 2.44V V_{BE} needs to be AC coupled to the next stage
42 - 43		V_{DC} = 4.7V Short circuit protected
44		V_{DC} = DAC output
15 - 46 - 47 48 - 49 - 58		I_2 active if $V_{PIN} \leq 2.7V$

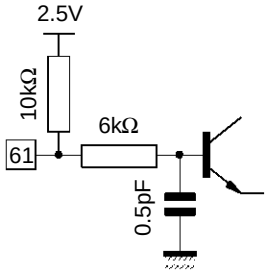
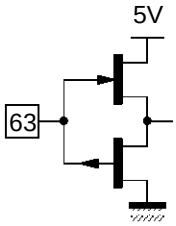
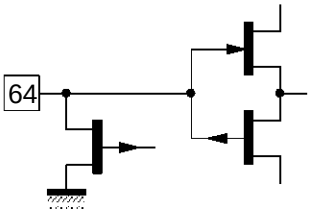
0030-12.TBL

INPUT/OUTPUT PIN CONNECTION (continued)

Pin N°	Circuitry	Comments
50		
51 - 52 53 - 54		Output not selected $V_{DC} \cong 0$ Output selected, $V_{OUT} = 2\ V_{IN} - 1.22$
55		Output not selected, $V_{OUT} = 0$ Output selected, $V_{OUT} = 1.87\ V_{IN} - 0.8$ (Videocrypt compatible level)
59		Gain is given by deemphasis filter component

0030-13.TBL

INPUT/OUTPUT PIN CONNECTION (continued)

Pin N°	Circuitry	Comments
61	 0030-35.EPS	V_{DC} = 2.5V
63	 0030-36.EPS	
64	 0030-37.EPS	

0030-14.TBL

PIN FUNCTION DESCRIPTION

1 - SCART DRIVERS WITH OSD

'Text' must be able to be added to the video on command with or without 'blanking'. Blanking adds either a black line around the characters or a black box for the characters to sit in. During 'blanking' the chip will output OSD 'background' level.

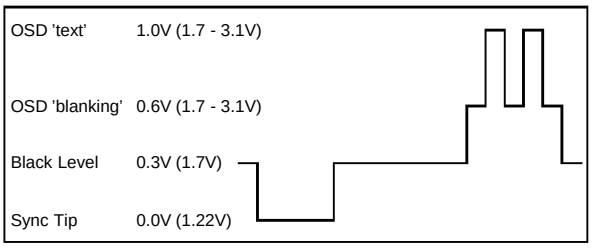
There are 2 basic presentation modes of OSD 'text'.

1) OSD 'text' written on a blank screen of selectable brightness.
2) OSD 'text' written on top of the TV picture.

Additionally the OSD 'text' can be displayed with or without 'blanking'. The blanking from the microcontroller typically comes in two styles. Either as a line around characters or a box for the characters to sit in).

1 of 4 output levels from the SCART are required when using OSD. The diagram below shows part of a TV line displaying a small OSD. It starts with :

a) a line sync pulse of 5µs at 0V then,
b) 13µs at black level, followed by
c) 2µs at OSD 'background' level.
d) This is the OSD 'text' which has been shown as 2µs pulses going to peak white. These would be typically programmed to say 0.8V with the OSD 'background' at 0.3V (1.7V at matrix output).



0030-07.EPS

In order to achieve this two DACs are used to generate the programmable voltage levels for OSD 'background' and 'text'.

The video outputs and terms are :

i) Normal video

sync tips = +1.22V
black level = +1.7V
peak white = +3.1V

ii) Video with OSD
Video with OSD
sync tips = +1.22V
black level = +1.7V
'background' level = +1.7V to 3.1V, programmable in 8 steps of 0.2V per step
'text' = +3.1V to 1.7V, programmable in 8 steps of 0.2V per step

iii) 'background' occurs during active video so whenever the micro generates 'blanking' it will force the SCART output to 'background' level (+1.7V to +3.1V).

iv) 'text' occurs during active video so whenever OSD occurs the SCART output is forced to 'peak white' (+3.1V to +1.6V). In fact the OSD 'text' has higher priority than 'background' so gets applied to the signal stream after 'background'.

Described above is an ideal situation with $2.0V_{PP}$ video with the bottom of the sync pulses at 1.22V. However the actual voltage of the sync tips will vary because the video is AC coupled and the picture content will change. Thus, in order to apply the 'blanking' or 'OSD' we need DC restored video the voltage of the sync tips are known and this is achieved by having 'DC level clamps' on all video input pins.

Pin 2 S3

This is the tri-stateable bi-directional SCART pin 8 driver for SCART-3. Since SCART-1,2 & 3 can be either controller or receiver SCART pin 8 is either an output or input. Since some equipment does not follow the SCART spec fully, the micro has full control of these pins via bits in the 'control' block.

As input; Z_{IN}>10kΩ <2V = logic 0, >9.5V = logic 1
As output; logic 0 outputs sink 1-3mA to gnd
logic 1 outputs source 1-3mA from V_{CC}-1V

Pin 3 S2

SCART-2 driver, same spec as pin 2.

Pin 4 S1

SCART-1 driver, same spec as pin 2.

2 - CONTROL BLOCK

This has an I^2C bus 2 wire interface with the related registers. It also contains 2 bi-directional tri-stateable logic I/O drives.

Pin 1 Ground

The main power ground connection for the control logic, registers, the I^2C bus interface, synthesiser & watchdog.

Pin 8 HA

For the I^2C bus interface it is necessary to have a programmable bit on the address in case the chip address clashes with that of another chip in the application. CMOS input levels must be held high or low externally ; 0 = 06h, 1 = 46h.

Pin 9 IO1

A general purpose I/O pin.

Pin 10 IO2

A general purpose I/O pin. It may alternatively be programmed via I^2C bus to output an internally generated 20kHz squarewave for LNB control (ASTRA recommandation is 22kHz ± 4kHz).

Pin 11 V_{DD}

Digital +5V power supply.

Pin 63 SCL

This is the I^2C bus clock line. Clock = DC to 100kHz. Requires external pull up eg. 10kΩ to 5V.

Pin 64 SDA

This is the I^2C bus data line. Requires external pull up eg. 10kΩ to 5V.

3 - MISCELLANEOUS BITS

Pin 12 XTL

This pin allows for the on-chip oscillator to be either used with a crystal to ground of 4MHz, or to be driven by an external source via a 22kΩ series resistor and 1nF series capacitor. This second option is recommanded. The external source can be either 4MHz or 8MHz. A programmable bit in the control block removes a÷ 2 block when the 4MHz option is selected.

Pin 13 RESET

Power on reset output. This is a voltage sensitive circuit and will give a LOW output until both supplies to this chip rise to greater than 80% of their correct value. It has some hysteresis so will remain HIGH until either of the supplies falls below 65%. The output is a current sink, 2mA, with an internal 10kΩ pull-up resistor. It is possible to force the chip into or out of reset and by pass the on-chip delay.

Typical thresholds are:	V_{DD}=5V	V_{CC}=12V
power up	3.8V	9.2V
power down	3.2V	7.5V

Pin 14 TEST

Test pin to enable scan path testing of logic.
Normal operation = L Test mode = H
It must be grounded for normal operation.

Pin 15 DAOUT

This is the LNB drive which is the output of an amplifier that compares the input on pin 44 with an 8-bit DAC. The DAC is programmed through the I^2C bus interface to set the reference voltage for the LNB drive amplifier. The voltage range is 0 to 2.35 volts (2 bandgaps), hence the feedback signal must be divided down to be in this range. Pin 15 output current must be maintained lower than 2mA.

Pin 44 DAIN

The voltage actually fed to the LNB is divided down & connected here (feedback) for the on-chip regulator.

4 - SOUND DETECTION BLOCK

The different de-emphasis formats are selected through the audio MUX and are the same for both channels. That is, as with the volume control, the I^2C bus registers simultaneously control both channels with each bit of registers.

Pin 6 AUXOUT1 (LEFT)

This audio output is sourced directly from the audio MUX, and as a result does not include any volume control function. It will output $1V_{PP}$ biased at 2.35V with Z_{OUT}=1kΩ. If SCART socket drive is needed then an external buffer will be required.

Pin 7 AUXOUT2 (RIGHT)

See pin 6.

Pin 16 AUXIN1 (LEFT)

This pin allows an auxilliary audio signal to be connected to the input of channel 1 audio processor and hence makes use of the on chip volume control. An on-board MAC decoder is a typical user of this feature. Needs to be externally biased to V_{REF}.

Pin 17 U751 (LEFT)

A capacitor and resistor in parallel of 75µs time constant connected between here and V_{REF} (pin 27) to provide 75µs de-emphasis for channel 1. Internally selectable is an internal resistor that can be programmed to be added in parallel thereby converting the network to approx 50µs de-emphasis. The value of the internal resistor is 44kΩ ± 30%. The amplifier for this filter is voltage input, current output; with ± 500mV input the output will be ± 55µA.

Pin 18 J171 (LEFT)

The external J17 de-emphasis network for channel 1. The amplifier for this filter is voltage input, current output; with ± 500mV input the output will be ± 55µA.

Pin 19 AUXIN2 (RIGHT)

Same as Pin 16.

Pin 20 U752 (RIGHT)

Same as Pin 17.

Pin 21 J172 (RIGHT)

Same as Pin 18.

Pin 22 GND

This ground pin is double bonded ; 1) to channel 1 RF section & VCO and 2) to both AGC amplifiers, channel 1 audio section, audio MUX, internal power & references to audio section.

Pin 23 DET1 (LEFT)

The output of FM phase detector 1 (left channel). This is for the connection of an external loop filter for the PLL. The output is a push pull current source with ± 90µA output with ± 500mV input to the internal mixer.

Pin 24 FMIN1

This is the positive input to the two FM demodulators. It feeds two AGC amplifiers with a bandwidth of at least 5-10MHz. There is one amplifier for each channel both with the same differential input. The AGC amplifiers have a 0dB to + 40dB range ; in conjunction with AMPLOCK function it will produce a constant amplitude of the selected subcarrier.
Z_{IN} = 5kΩ Min input = $2mV_{PP}$ per subcarrier
Max input = $500mV_{PP}$ (max when all subcarriers are added together, when their phases coincide).

Pin 25 AGC1 (LEFT)

AGC amplifier 1 peak detector capacitor connection. The output current has an attack/decay ratio of 1:32. That is the ramp up current is approximately 5µA and decay current is approximately 160µA. 11V gives maximum gain. This pin is also driven by a circuit monitoring the voltage on AMPLOCK1.

Pin 26 FMIN2

This is the -ve input to the AGC amplifiers forming a differential input stage. All inputs are biased to V_{REF} (2.35V) via an internal 10kΩ resistor.

Pin 27 VREF (2.35V)

This is the audio processor voltage reference used throughout the FM/audio section of the chip. As such it is essential that it is well decoupled to ground to reduce as far as possible the risk of crosstalk and noise injection. This voltage is derived directly from the bandgap reference. It cannot sink current.

Pin 28 V_{CC} (+12V power supply)

Double bonded main power pin for the audio/FM section of the chip. The two bond connections are; (1 to the ESD and guard rings and 2) to power the circuit and on chip regulators/references.

Pin 29 DET2 (RIGHT)

Same as Pin 23.

Pin 30 AMPLOCK1 (LEFT)

The output of amplitude detector 1. Requires a capacitor and a resistor to GND. The voltage across this is used to decide whether there is a signal being received by FM det 1. The level detector output drives a bit in the 'control block' I^2C bus register 7 bit 0. This also drives AGC amp 1. When the voltage on this pin is >(V_{REF}+1V_{BE}) it sinks current to V_{REF} from pin 25 to reduce the AGC gain.

Pin 31 CPUMP1 (LEFT)

The output from the frequency synthesizer is a push-pull current source which requires a capacitor to ground to derive a voltage to pull the VCO to the target frequency. The output is ± 100µA to achieve lock and ± 2µA during lock to provide a tracking time constant of approximately 10Hz.

Pin 32 AGC2 (RIGHT)

Same as Pin 25.

Pin 33 GND

This ground pin is double bonded ; 1) to the volume control, ANRS, ESD and guard rings and 2) to the VCO & RF section of channel 2.

Pin 34 AMPLOCK2 (RIGHT)

Same as Pin 30

Pin 35 CPUMP2 (RIGHT)

Same as Pin 31.

Pin 36 IREF

This is a buffered V_{REF} output to an off-chip resistor to produce an accurate current reference, within the chip, for the biasing of amplifiers with current outputs into filters. It is also required for the ANRS circuit to provide accurate rolloff frequencies. This pin should not be decoupled as it will inject current noise. The target current is 10µA ± 2 thus a 240kΩ ± 1% is required.

5 - AUTOMATIC NOISE REDUCTION SYSTEM (ANRS) AND VOLUME CONTROL

There is a ANRS defeat which allows the audio to bypass the ANRS section but still go to the volume control. The volume control will be 32 steps of 1.25dB, with the lowest step being audio 'mute' (no output).

Pin 37 PEAKOUT

The ANRS control loop peak detector output requires a capacitor to ground from this pin. Also a resistor to V_{REF} pin 27 to give some accurate decay time constant. The value of the capacitor and resistor control the attack and decay times, typically 0.1ms attack & 25ms decay.

Pin 38 FCLEFT

The variable bandwidth gm amplifier has a current output which is variable depending on the input signal amplitude as defined by the control loop. The output current is then dumped into an off-chip capacitor which together with the accurate current reference define the min/max rolloff frequencies. A capacitor is connected to ground from this pin for channel 1 (left).

Pin 39 PEAKIN

This is the input to the control loop peak detector and is connected to the output of the off-chip control loop band pass filter. This requires AC coupling between this input pin and the summer output Pin 40.

Pin 40 SUMOUT

The two audio demodulated signals are summed together with an amplifier with a gain of 0.5 ie. if both inputs are 1 volt then the output is 1 volt. This amplifier has an input follower buffer which gives a V_{BE} offset in the DC bias voltage. Thus the filter which this amplifier drives must include AC coupling to the next stage (pin 39).

Pin 41 FCRIGHT

Same as Pin 38

Pin 42 AUDIOOUT2 (RIGHT)

The main audio output from the volume control level shifted and amplified to produce $2V_{PP}$ on a DC bias of 4.7 volts. This amplifier has short circuit protection and is intended to drive a SCART connector directly via AC coupling and meets the standard SCART drive requirements.

Pin 43 AUDIOOUT1 (LEFT)

Same as Pin 42.

6 - VIDEO BLOCK

Pin 5 SYNCIN

This input can be programmed to accept either a digital or an analog sync stream. The digital input will accept a made up sync signal consisting of the Genlock 'line' and 'frame' sync output. If it is smaller than 0.8V then it produces a sync tip level voltage (1.22V). If it is greater than 2.0V it produces black level (1.52V). This will generate a sync stream signal consisting of syncs only, that will be available on the 'Video Matrix'. The DC level of these syncs at the SCART O/Ps will be sync tip = 1.22V black level = 1.7V. The analog path is connected directly to the video matrix.

When pin-49 is selected for the video MUX, it is still possible to insert an external sync. The input must be a digital sync (Reg 18b6 = 1 > sync enabled) and is typically used to stabilise the OSD on a bad or noisy video on pin-52 only.

Control bits

2 bits	I^2C bus Reg 1	bits 6	,5	Effect
				Sync source
	default ------	X	0	Digital
		0	1	Analog
		1	1	Pin-49 clamped

Pin 45 S2VIDIN

External video input $1V_{PP}$ AC coupled 75Ω source impedance returned from a VCR for example. This input has a DC restoration clamp on its input. This gets the video to the correct DC level so that OSD can be added later when it is essential that the voltages of the video and OSD are at the correct levels with respect to each other. The clamp sink current is 1µA ± 30% with the buffer Z_I > 1MΩ. This signal is an input to the Video Matrix and is called SCART-2 Return.

Pin 46 S1VIDIN

External video input $1.0V_{PP}$ AC coupled 75Ω source impedance. This input has a DC restoration clamp on its input. This gets the video to the correct DC level so that OSD can be added later when it is essential that the voltages of the video and OSD are at the correct levels with respect to each other. The clamp sink current is 1µA ± 30% with the buffer Z_{IN} > 1MΩ. This signal is an input to the Video Matrix and is called SCART-1 Return.

Pin 47 DEC1IN

This input receives a PAL encoded output from, for instance a D2MAC decoder inside the receiver. The signals from pins 47 and 48 go to an internal selector switch that selects which signal goes to the Video Matrix.

Control bit

1 bit	I^2C bus Reg 1	bit	4	Signal selected
	default	---	0	Pin 48 (DEC2IN)
			1	Pin 47 (DEC1IN)

The output signal from the selector switch, which goes to the Video Matrix, is called Internal Decoder Return.

Pin 48 DEC2IN

This input can be driven for instance by the output of a Videocrypt decoder ZOUT = 500Ω video about $1.0V_{PP}$ from the reconstruction filter. This input has a DC restoration clamp on its input. This gets the video to the correct DC level so that OSD can be added later when it is essential that the voltages of the video and OSD are at the correct levels with respect to each other.

The clamp sink current is 1µA ± 30% with the buffer Z_{IN} > 1MΩ. The signals from pins 47 and 48 go to an internal selector switch that selects which signal goes to the Video Matrix.

Control bit

1 bit	Reg 1	bit	4	Signal selected
	default	---	0	Pin 48 (DEC2IN)
			1	Pin 47 (DEC1IN)

Pin 49 VI5

A video input with clamp @ 1.22V internally. It may be employed for use with noisy video signals by overiding the sync clamp externally at about 3V (this overcomes the 1.22V plus 2x V_{BE}).

Pin 50 OSDIN

Typically driven by a combination of an OSD O/P and the 'Blank' output from the OSD bit of the Micro. This input is then threshold detected and two outputs are generated.

Input	Output	
	Background	Text
< 0.8V	0	0
1.5-2.5V	1	0
> 3.5V	1	1

Pin 51 S3VIDOUT

Video driver for SCART-3 with OSD. This requires an external emitter follower buffer to drive a 150Ω load. The average DC voltage to be 1.5V on the O/P. The signal on pin 51 is video $2.0V_{PP}$ 5.5MHz B/W with sync tip=1.22V. This SCART O/P will be used to drive the TV typically. This pin gets its signal from the Video Matrix. It is then amplified and OSD is added before being output. The signal selected from the Video Matrix for output on this pin is controlled by a control register.

Control bits

3 bits I^2C bus Reg 4 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
default	------	0	1	0	Normal video
		0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

OSD addition is controlled by a control register. It is possible to separately control whether or not to add 'blanking' and/or 'text' to the video stream to this SCART output.

Control bits

2 bits I^2C bus Reg 4 bits		4,	3	Effect enabled
default	------	0	0	Background = Off Text = Off
		0	1	Background = On Text = Off
		1	0	Background = Off Text = On
		1	1	Background = On Text = On

Pin 52 S2VIDOUT

(See 1/ SCART drivers with OSD). Video driver for SCART-2. See pin 51.

Control bits

3 bits I^2C bus Reg 3 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
default	------	0	1	0	Normal video
		0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

OSD addition is controlled by a control register. It is possible to separately control whether or not to add 'blanking' and/or 'text' to the video stream to this SCART output.

Control bits

2 bits I^2C bus Reg 3 bits		4,	3	Effect enabled
default	----	0	0	Background = Off Text = Off
		0	1	Background = On Text = Off
		1	0	Background = Off Text = On
		1	1	Background = On Text = On

See also pin-5 where it is possible to add sync to stabilise OSD or video.

Pin 53 S1VIDOUT

Video driver for SCART 1. See pin 51. No OSD available on this output.

Control bits

3 bits I^{2}C bus Reg 2 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
default	------	0	1	0	Normal video
		0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

Pin 54 DECOUT2

Drives a second decoder such as D2MAC and this is able to pass 10MHz. See pin 53.

Control bits

3 bits I^{2}C bus Reg 6 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
default	------	0	1	0	Normal video
		0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

Pin 55 DECOUT1

This output can drive for instance a decoder. To allow for D2MAC it is able to pass 10MHz ; ZOUT < 75Ω. Video on this pin will be 1.9V_{PP}. When a Videocrypt encoded signal is output to the decoder on this pin its sync tips must be at 1.46V_{DC} . This pin gets its signal from the Video Matrix. It is then level shifted and amplified by 1.9 before being output. The signal selected from the Video Matrix for output on this pin is controlled by a control register.

Control bits

3 bits I^{2}C bus Reg 5 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
default	------	0	1	0	Normal video
		0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

Pin 56 V_{CC}

+12V double bonded ; 1) ESD+guard rings & 2) video circuit power.

Pin 57 GND

Strategically placed video power ground connection to reduce video currents getting into rest of circuitry.

Pin 58 CLAMPIN

This pin clamps the most negative extreme of the input (the sync tips) to +1.22V_{DC} (or appropriate voltage). The video at the clamp input is only 1V_{PP}. This clamped video which is de-emphasised, filtered and clamped (energy dispersal removed) is normal, negative syncs, video. This signal drives the Video Matrix input called Normal Video.
It has a weak (1.0µA ± 15%) stable current source pulling the input towards GND. Otherwise the input impedance is very high at DC to 1kHz Z_{IN} > 2MΩ. Video bandwidth through this is -1dB at 5.5MHz. The CLAMP input DC restore voltage is then used as a means for getting the correct DC voltage on the SCART outputs.

Pin 59 DEEMPHOUT

Output of de-emphasis Z_{OUT} < 50Ω 2V_{PP} B/W still 10.25MHz. This is the output that drives the capacitor into the CLAMP. It has to do this via the sound removal filter which may be a 5 or 7 pole low pass filter Z_{IN} = Z_{OUT} = 500Ω -3dB corner about 5.25MHz. Video at pin 59 is positive. Internally the 2V_{PP} video is reduced to 1V_{PP} to drive the internal Video Matrix input called De-emphasised video. This signal also called 'Unclamped Unfiltered' and is the signal required by Filmnet PAL decoders for example. It is called unfiltered because it still has its high frequency sub-carriers (not been through the low pass filter).

Pin 60 DEEMPHIN

Input of de-emphasis stage, with a Z_{IN} of 10kΩ or greater. B/W is 10.25MHz. The network between pins 59 & 60 will give 2x gain at 1.52MHz, about -2dB gain at 5MHz and +17dB gain at 10kHz as in accordance with CCIR 405-1.

Pin 61 VIDIN

AC-coupled Video input from a tuner. This is raw baseband up to 10.25MHz. Input amplitude is 0.25-1.0V_{PP} at 1.52MHz. Z_{IN} > 5kΩ. This drives an on-chip video amplifier. The other input pin of this amp is AC grounded by being connected to an internal V_{REF}. The video amplifier has selectable gain from 0dB to 12.7dB in 63 steps. This is programmable, as is the output selected, whether normal or inverted.

Control bits

6 bits	I^2C bus Reg 18	bits	5,	4,	3,	2,	1,	0	Gain Selected
	default	------	0	0	0	0	0	0	0dB
			n						n x 0.202dB
			1	1	1	1	1	1	+12.7dB

The normal or inverted output selected (which is 1.0V_{PP}) also drives the Video Matrix input called Baseband.

Control bit

1 bit	I^2C bus Reg 1	bit	3	Video selected
	default	----	0	Normal
			1	Inverted

Pin 62 GND

Ground, especially for the low level input from the tuner.

Figure 1 : Fundamental Block Diagram

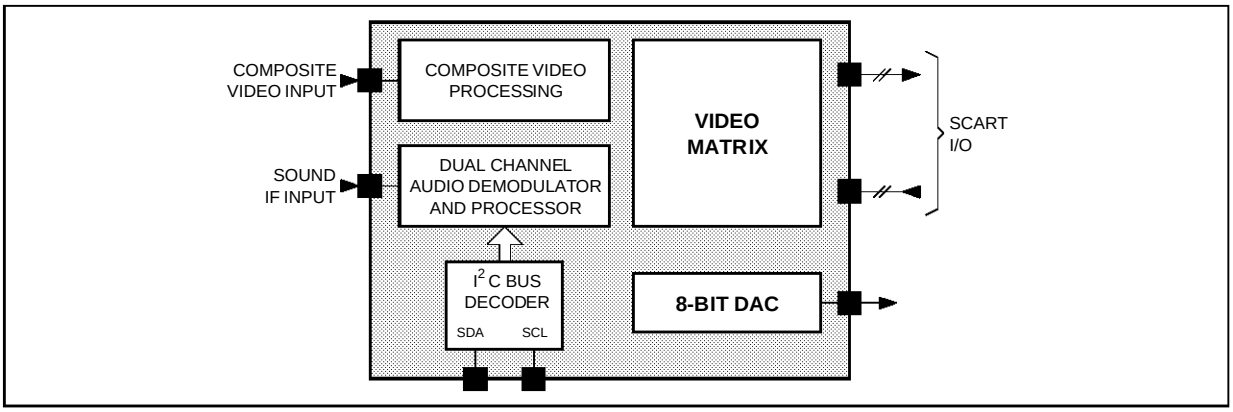


Figure 2 : Video Processing Block Diagram

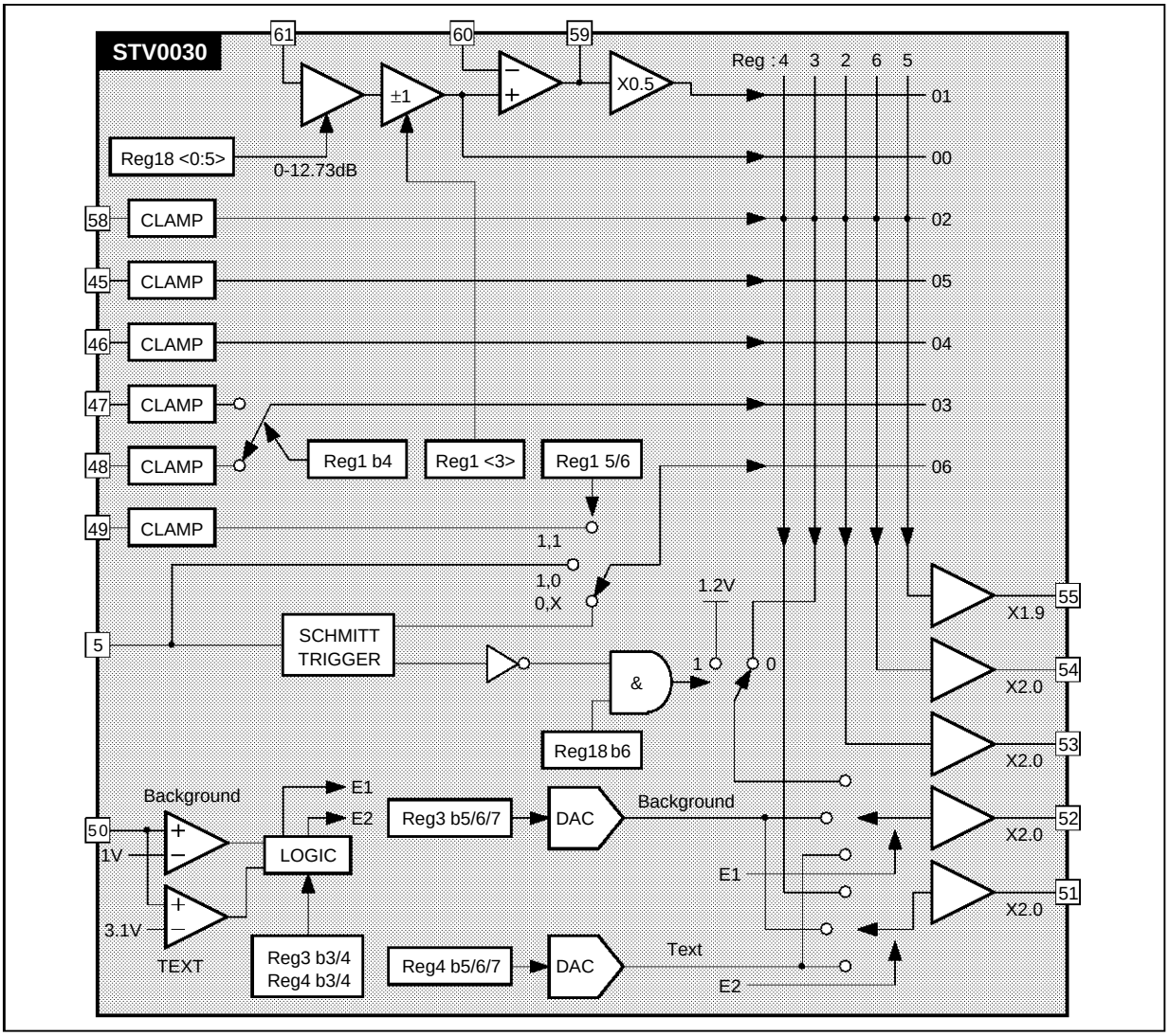


Figure 3 : FM Demodulation Block Diagram

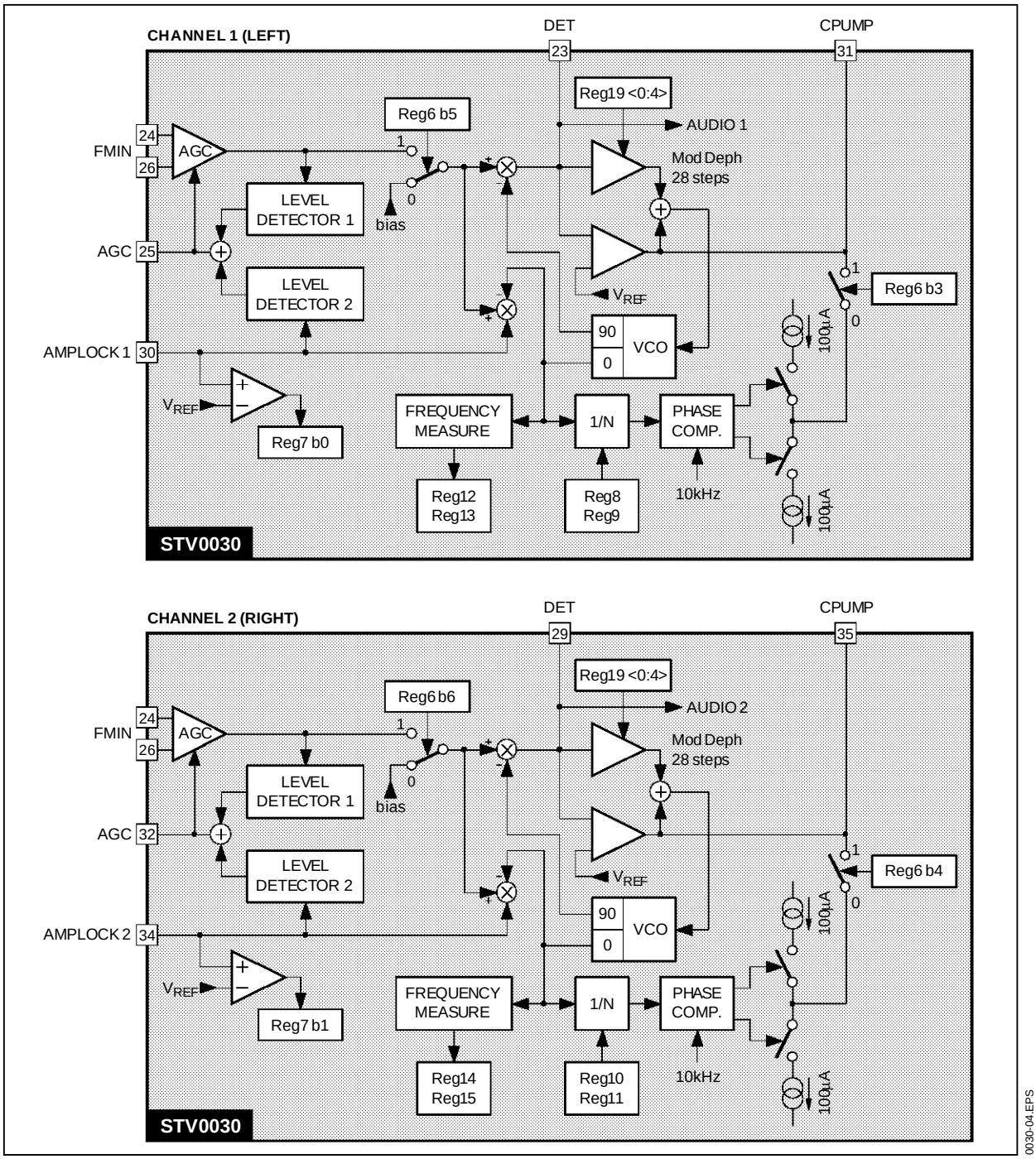
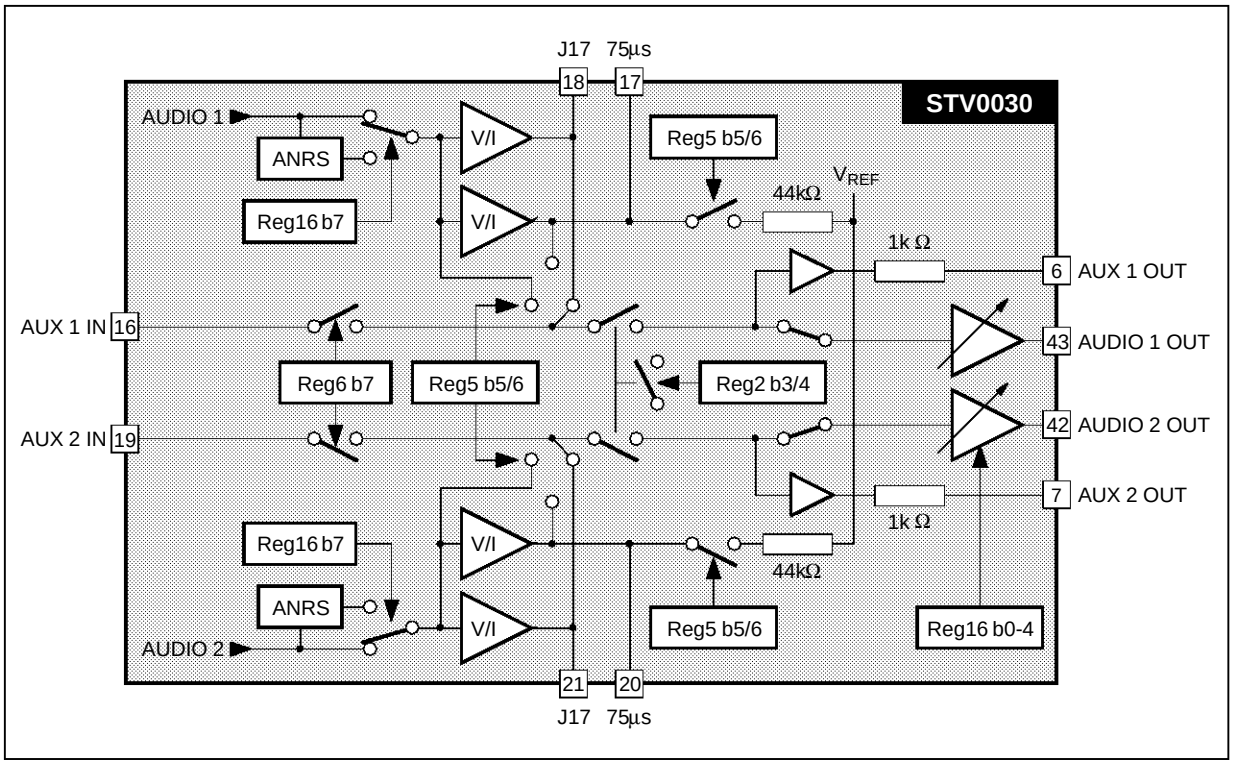


Figure 4 : Audio Processing Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC} V_{DD}	Supply Voltage	13.2 7.0	V V
P_{tot}	Total Power Dissipation	1.0	W
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-55, +150	°C

0030-03.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Thermal Resistance Junction-ambient	60	°C/W

0030-04.TBL

DC AND AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} V_{DD}	Supply Voltage Range		11.4 4.75	12 5.0	12.6 5.25	V V
IQ_{cc} IQ_{dd}	Supply Current			55 8	70 15	mA mA

0030-05.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO DEMODULATOR (see Figure 3)						
FMI	FM Subcarrier Input Level Pin 24 - Pin 26 for AGC action	VCO locked on carrier at 6MHz, 680kΩ load on Pin 30 and Pin 34	5		500	mV_{PP}
DETH	Detector 1 and 2 (Pins 30 and 34) threshold for activating AGC			3.1		V
IDETA	Max sink/source Pins 30 and 34 current	With AGC operation		100		µA
IDETS	Max sink/source Pins 30 and 34 current	Without AGC limited gain		200		µA
VCOMI	VCO Mini Frequency	V_{CC} = 11.4 to 12.6V T_{amb} = 0 to 70°C			5	MHz
VCOMA	VCO Maxi Frequency		10			MHz
AP50	1kHz Audio Level at PLL output Pins 23 and 29	$0.5V_{PP}$ 50kHz dev. FM input, Coarse deviation set to 50kHz (Reg 19 = 16_{HEX})	0.5	1	1.5	V_{PP}
APA50	1kHz Audio Level at PLL output Pins 23 and 29	$0.5V_{PP}$ 50kHz dev. FM input, Coarse and fine settings used	0.85	1	1.15	V_{PP}
DPCO	Digital Phase Comparator Pins 31 and 35 output current	Sink and source current to external capacitor		100		µA
AUDIO DE-EMPHASIS ($1V_{PP}$ on Detector 1 and 2 - Pins 23, 29)						
D50e	1kHz Audio Level on 50µs de-emphasis output Pins 17 and 20	22kΩ and 2.2nF load Internal 44kΩ off input and settings as APA50		1.91		V_{PP}
D50i	1kHz Audio Level on 50µs de-emphasis output Pins 17 and 20	22kΩ and 3.3nF load Internal 44kΩ on input and settings as APA50		1.3		V_{PP}
D75	1kHz Audio Level on 50µs de-emphasis output Pins 17 and 20	22kΩ and 3.3nF load Internal 44kΩ off input and settings as APA50		1.80		V_{PP}
DJ17	1kHz Audio Level on J17 de-emphasis output Pins 18 and 21	Load as in Application Diagram, input and settings as APA50		1.45		V_{PP}
R50	Internal resistor for 50/75µs switching		30	44	58	kΩ
AUTOMATIC NOISE REDUCTION SYSTEM						
LRS	Left + Right Summer output Pin 40	$1V_{PP}$ on left and right channel	0.9	1	1.1	V_{PP}
NDRT	PIN 37 Level Detector Rise Time Constant	External 22nF load		110		µs
NDFT	PIN 37 Level Detector Fall Time Constant	External 22nF to GND and 1.2MΩ to Pin 27		26.4		ms
NDLL	Pin 37 Bias Level	No audio in		2.44		V
NDML	Pin 37 Max. Level (internal clamp)	$3V_{PP}$ 1kHz on Pins 23 and 29	2.7	3	3.2	V
LLCF	Noise Reduction Cut-off Frequency for Low Level Audio	$100mV_{PP}$ on Pin 23 and 29		0.85		kHz
HLCF	Noise Reduction Cut-off Frequency at High Level	$1V_{PP}$ on Pin 23 and 29		7		kHz
AUDIO OUTPUT (Pins 42 and 43)						
DCOL	DC Output Level Measured on Pins 42, 43	Aux. input Pins 16 and 19 connected to V_{REF}		4.7		V
AOLN	Audio Output Level at nominal input at 0dB attenuation setting, measured on Pins 42 and 43	FM input as for APA50 No de-emphasis No noise reduction	1.57	1.9	2.25	V_{PP}
AOL50	Audio Output Level at nominal input at 0dB attenuation setting, Measured on Pins 42 and 43	FM input as for APA50 50µs de-emphasis as for D50i No noise reduction	1.75	2.5	3.25	V_{PP}
AOL50B	Audio Output Level at nominal input at 0dB attenuation setting, Measured on Pins 42 and 43	FM input as for APA50 50µs de-emphasis as for D50i No noise reduction	1.55	2.5	3.45	V_{PP}

0030-06.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO OUTPUT (Pins 42 and 43) (continued)						
AOL17	Audio Output Level at nominal input at 0dB attenuation setting, Measured on Pins 42 and 43	FM input as for APA50, J17 de-emphasis No noise reduction	1.90	2.75	3.60	V_{PP}
AMA1	Audio Output Attenuation with mute on	$1V_{PP}$ - 1kHz from Aux input Pins 16, 19 to Pins 42, 43		60		dB
MXAT	Max. Attenuation before mute	1kHz, from Aux input Pins 16 and 19 to Pins 42 and 43	30.7	32.7	34.7	dB
MXAG	Max. Audio Gain	1kHz, from Aux input Pins 16 and 19 to Pins 42 and 43		1.9		
ASTP	Attenuation of each of the 31 steps	1kHz		1.25		dB
THDA1	THD at 0dB Attenuation Setting Measured on Pins 42, 43	$1V_{PP}$ - 1kHz from Aux. Input Pins 16, 19 to Pins 42, 43		0.15		%
THDA2	THD at 0dB Attenuation Setting Measured on Pins 42, 43	$2V_{PP}$ - 1kHz from Aux. Input Pins 16, 19 to Pins 42, 43		0.3	1	%
THDFM	THD at 0dB Attenuation Setting Measured on Pins 42, 43	FM Input as for APA50 50µs de-emphasis, no ANRS		0.3	1	%
ACS	Audio Channel Separation Measured on Pins 42, 43	$1V_{PP}$ - 1kHz from Aux. Input Pins 16, 19		80		dB
ACSFM	Audio Channel Separation at 1kHz - Measured on Pins 42, 43	- $0.5V_{PP}$ 50kHz deviation FM input on one channel - $0.5V_{PP}$ no deviation FM input on the other channel - Chip deviation set to 50kHz - 50µs de-emphasis, no ANRS		60		dB
SNFM	Signal to Noise Ratio Measured on Pins 42, 43	FM input as for APA50 50µs de-emphasis, no ANRS weighted noise curve A		62		dB
SNFMNR	Signal to Noise Ratio Measured on Pins 42, 43	FM input as for APA50 No de-emphasis, ANRS ON weighted noise curve A		80		dB
AUXILIARY AUDIO OUTPUT (Pins 6 and 7)						
DCOLAO	DC Output Level Measured on Pins 6, 7	Aux. Input Pins 16 and 19 connected to V_{REF}		2.35		V
AGAO	Audio Gain Measured on Pins 6, 7	1kHz from Aux. Inputs Pins 16, 19 to Pins 6, 7		1		
ZAO	Pins 6 and 7 Output Impedance		0.7	1	1.3	kΩ
THDA02	THD on Pins 6, 7	$2V_{PP}$ - 1kHz from Aux. Input Pins 16, 19 to Pins 6, 7		0.01	0.1	%
THDAOFM	THD on Pins 6, 7	FM input as for APA50 50µs de-emphasis, no ANRS		0.15		%
I/O's (Pins 2, 3, 4, 9 and 10)						
SCIL	Pin 2, 3 or 4 Low Level Input				2	V
SCIH	Pin 2, 3, or 4 High Level Input		9.5			V
SCOH	Pin 2, 3 or 4 High Level Output	10kΩ load to ground	9.5	11		V
SCOL	Pin 2, 3 or 4 Low Level Output	10kΩ load to ground		0.1	2	V
V_{IL}	Pin 9 or 10 Low Level Input				0.8	V
V_{IH}	Pin 9 or 10 High Level Input		2.4			V
V_{OL}	Pin 9 or 10 Low Level Output	I_{Sink} = 2mA		0.2	0.4	V
V_{OH}	Pin 9 or 10 High Level Output	I_{Source} = 2mA	3.2	4.6		V

0030-07.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RESET						
RSR	Reset Internal Pull-up Resistor	Reset high		10		kΩ
RSI	Reset Internal Sink Current	Reset low		2		mA
RTCCU	End of Reset for V_{CC}	V_{DD} = 5V, V_{CC} going up		9.2		V
RTCCD	Start of Reset Threshold for V_{CC}	V_{DD} = 5V, V_{CC} going down		7.5		V
RTDDU	End of Reset Threshold for V_{DD}	V_{CC} = 12V, V_{DD} going up		3.8		V
RTDDD	Start of Reset Threshold for V_{DD}	V_{CC} = 12V, V_{DD} going down		3.2		V
D/A CONVERTER (see Figure 1)						
DA00	Min. Output Voltage on Pin 15 for 00_{HEX}	Sense input Pin 44 connected to output Pin 15, I_{LOAD} <2mA	0	30	70	mV
DAFF	Max. Output Voltage on Pin 15 for FF_{HEX}	As for DA00	2.15	2.35	2.55	V
ILE	Integral Linearity			0.5	2	LSB
COMPOSITE SIGNAL PROCESSING (see Figure 2)						
VIDC	Pin 61 DC Level	External load current <1µA	2.15	2.35	2.55	V
ZVI	Pin 61 Input Impedance			10		kΩ
DEODC	Pin 59 DC Output Level	1.2kΩ from Pin 59 to Pin 60, 2kΩ and 3kΩ in series to 1µF from Pin 60 to GND	3.3	3.7	4.1	V
DEOAC	Pin 59 AC Level for GV = 0 dB	Pin 61 level = $1V_{PP}$, 100kHz	1.87	2	2.13	V_{PP}
DEOMX	Pin 59 Max. AC Level before clipping	GV = 0 dB	5	6		V_{PP}
DEOISC	Pin 59 Max. Source Current			8		mA
DEOISK	Pin 59 Max. Sink Current			2		mA
ZDEO	Pin 59 Output Impedance @ 5MHz			2		Ω
DGV	Gain Error vs GV @ 100kHz	For GV = 0 to 12.7dB	-0.5	0	0.5	dB
DINV	Gain Variation when using inverter	@ 100kHz	-0.5	0	0.5	dB
DEBW	Bandwidth at Pin 59 for $1V_{PP}$ input measured on Pin 59	@ - 3dB with GV = 0dB	10	20		MHz
DFG	Differential Gain on sync pulses measured on Pin 59	$1V_{PP}$ CVBS + $0.5V_{PP}$ 25Hz sawtooth input Pin 61, GV=0			1	%
CLAMP STAGES						
ISKC	Clamp Input Sink Current Pins 45, 46, 47, 48 49 and 58	V_{IN} = 3V	0.6	1	1.4	µA
ISCC	Clamp Input Source Current same pins as ISKC	V_{IN} = 2V	30	50	70	µA
VCL	Sync Tip Level on selected output pin (Pins 51, 52, 53 or 54)	$1V_{PP}$ CVBS through 10nF on input (45,46,47 or 58)	1.1	1.22	1.34	V
VCL5	Sync Tip Level on Pin 55	Same as for VCL	1.38	1.46	1.54	V
VIDEO MATRIX						
XTK	Output Level on any output when $1V_{PP}$ CVBS input is selected for any other output	@ 5MHz		60		dB
BGT	Background Graphics Threshold Pin 50		0.8	1	1.5	V
CGT	Character Foreground Threshold Pin 50		2.5	3	3.5	V
BMN	Background Level for 000 selection	Measured on selected output Pin 52 or 53		1.7		V
BMX	Background Level for 111 selection	Same as BMN		3.1		V
FMN	Foreground Level for 000 selection	Same as BMN		1.7		V
FMX	Foreground Level for 111 selection	Same as BMN		3.1		V
BFG	Output buffer gain Pins 45,46,47,48,58	@ 100kHz	1.87	2	2.13	
BFG5	Output buffer gain Pin 55	@ 100kHz	1.77	1.9	2.03	

0030-08.TBL

CIRCUIT DESCRIPTION : VIDEO SECTION

The composite video is first set to a standard level by means of a 64 step gain controlled amplifier. In the case that the modulation is negative, an inverter can be switched in. The deemphasis network is fed by a wide bandwidth amplifier and energy dispersal is removed by a sophisticated sync tip clamping circuit. This circuit is used on all inputs to a video switching matrix, thus making sure that no DC steps occur when switching video sources.

The matrix can be used to feed video to and from decoders such as D2MAC or scrambled analog video.

Two special inputs allow insertion of graphics on video or clean sync, or a mix of both even when only noise is present at the tuner output.

CIRCUIT DESCRIPTION : AUDIO SECTION

The two audio channels are totally independent except for the possibility given to output on both channels only one of the selected input audio channels.

To allow a very cost effective application, each channel uses PLL demodulation. Except for the overall high pass filter removing the video of the composite signal, no complex filter is needed.

The frequency of the demodulated subcarrier is chosen by a frequency synthesiser which sets the frequency of the internal local oscillator by comparing its phase with the internally generated reference. When the frequency is reached, the microprocessor switches in the STV0030 PLL and the demodulation starts. At any moment the microprocessor can read from the device the actual frequency to which the PLL is locked. It can also verify that a carrier is present at the given frequency, thanks to an amplitude demodulator which is also used for the audio input AGC.

In order to maintain constant amplitude of the recovered audio regardless of variations between satellites or subcarriers, the PLL loop gain may be programmed from 28 values, with coarse (four values) and fine (7 steps) adjustment.

Two different networks can be permanently connected for either 75µs or J17 de-emphasis. If 50µs de-emphasis is required, this can be inserted by an internal switch, thus allowing a worldwide application.

A dynamic noise reduction system (ANRS) is used using a lowpass filter, the cutoff frequency of which is controlled by the amplitude of the audio after insertion of a bandpass filter.

Two audio outputs are provided : one is a fixed $1V_{PP}$ and the other is a gain controlled $2V_{PP}$. These outputs are chosen by an audio matrix between non de-emphasised, 50 or 75µs de-emphasised, J17 deemphasised audio channel. In each case the dynamic noise reduction system can be used. Alternatively the selected outputs can receive the auxilliary audio inputs without processing. The gain controlled amplifier has a gain range from + 6dB to - 32dB with 1.25dB steps. This can also be muted.

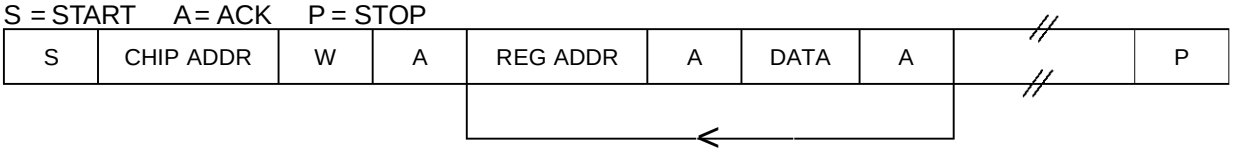
The 8-bit Digital to Analog Converter outputs a voltage ranging from 0 and 2.35V via a differential amplifier for digital words from 00 to FF. By adding a suitable output buffer/converter, this DAC can be used to control LNB voltages (or polariser currents) with a range exceeding 0 to 2.35V.

IIC PROTOCOL

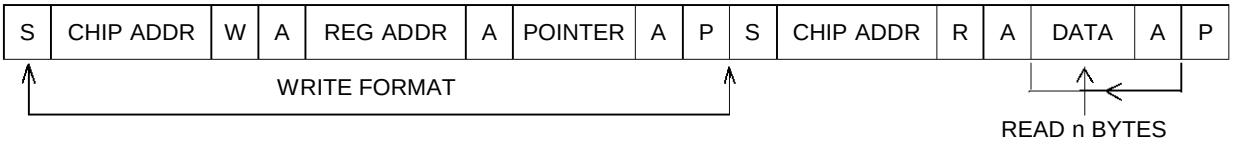
The chip address is 06_H if Pin 8 to ground and 46_H if Pin 8 to V_{DD}.

Transmit to Chip

S = START A = ACK P = STOP



Receive from Chip



In read mode a pointer is written to register 0. This pointer addresses a particular register whose contents can be read any number of Times. There are 19 registers in Total.

IIC CONTROL REGISTERS

Reg 1 IIC → reg

bit

0	L	Not used	
1	L	Not used	
2	L	Not used	
3	L	Select video invert	(H = inverted, L = non-inverted)
4	L	Select input	(H = Pin 47, L = Pin 48)
5	L	Select sync source	bits 6 5 X 0 digital sync input (Schmitt Trigger) 0 1 analogue sync input 1 1 Pin 49 clamp input
6	L	Select clamp Pin 49	
7		Not used	

Reg 2 IIC → reg

bit

0	L	Select source for SCART 1 O/P	See Pin 53 description
1	H	Select source for SCART 1 O/P	
2	L	Select source for SCART 1 O/P	
3	H	Select Left/Right/Stereo (see audio mux truth table)	
4	H	Select Left/Right/Stereo (see audio mux truth table)	
5	L	Test multiplex control VCOCLK1/Div1000	
6	L	Test multiplex control VCOCLK2/Div1000	
7	L	Test multiplex control RESET	

Reg 3 IIC → reg

bit

0	L	Select source for SCART 2 O/P	See Pin 52 description
1	H	Select source for SCART 2 O/P	
2	L	Select source for SCART 2 O/P	
3	L	Select OSD effect for SCART 2 (background)	
4	L	Select OSD effect for SCART 2 (text)	
5	L	Select OSD ”background” level (LSB)	
6	L	Select OSD ”background” level	
7	L	Select OSD ”background” level (MSB)	

Reg 4 IIC → reg

bit

0	L	Select source for SCART 3 O/P	See Pin 51 description
1	H	Select source for SCART 3 O/P	
2	L	Select source for SCART 3 O/P	
3	L	Select OSD effect for SCART 3 O/P (background)	
4	L	Select OSD effect for SCART 3 O/P (text)	
5	H	Select OSD ”text” level (LSB)	
6	H	Select OSD ”text” level	
7	H	Select OSD ”text” level (MSB)	

Reg 5 IIC → reg

bit			
0	L	Select source for decoder 1 O/P	See Pin 55 description
1	H	Select source for decoder 1 O/P	
2	L	Select source for decoder 1 O/P	
3	L	Not used	
4	L	Not used	
5	H	Select de-emphasis (see audio mux truth table)	
6	L	Select de-emphasis (see audio mux truth table)	
7		Not used	

Reg 6 IIC → reg

bit			
0	L	Select source for decoder 2 O/P	See Pin 54 description
1	H	Select source for decoder 2 O/P	
2	L	Select source for decoder 2 O/P	
3	H	Select frequency synth 1 OFF/ON (L=OFF)	
4	H	Select frequency synth 2 OFF/ON (L=OFF)	
5	L	Select RF source (L=OFF) to FM Det 1	
6	L	Select RF source (L=OFF) to FM Det 1	
7	L	Select aux audio input for both channels (see audio mux truth table)	

Reg 7 Reg → IIC

bit	
0	Status of Amp_lock 1 (subcarrier presence)
1	Status of Amp_lock 2 (subcarrier presence)
2	Not used
3	Not used
4	Not used
5	Not used
6	Not used
7	Not used

Reg 8 IIC → reg

bit		
0	L	Not used
1	L	Not used
2	L	Not used
3	L	Select data direction for I/O 1 (H = output)
4	L	Select data direction for I/O 2 (H = output)
5	L	Not used
6	L	Select frequency for det 1, LSB (bit 0) of 10 bit value
7	H	Select frequency for det 1

Reg 9 IIC → reg

bit		
0	H	Select frequency for det 1, Note : bit 3 of 10 bit value
1	H	Select frequency for det 1
2	H	Select frequency for det 1
3	H	Select frequency for det 1
4	L	Select frequency for det 1
5	H	Select frequency for det 1
6	L	Select frequency for det 1
7	H	Select frequency for det 1 bit 9, MSB (10th bit) of 10 bit value

Reg 10 (Reg 0Ahex) IIC → reg

bit
0 L Select data direction for S1 (L = input state)
1 L Select data direction for S2 (L = input state)
2 L Select data direction for S3 (L = input state)
3 L Text mux contril for LD1 (lock detect channel 1) test only!
4 L Text mux contril for LD2 (lock detect channel 1) test only!
5 Not used
6 L Select frequency for det 2, LSB (bit 0) of 10 bit value
7 L Select frequency for det 2

Reg 11 (Reg 0Bhex) IIC → reg

bit
0 L Select frequency for det 2, Note : bit 3 of 10-bit value
1 L Select frequency for det 2
2 H Select frequency for det 2
3 L Select frequency for det 2
4 H Select frequency for det 2
5 H Select frequency for det 2
6 L Select frequency for det 2
7 H Select frequency for det bit 9, MSB (10th bit) of 10 bit value

Reg 12 (Reg 0Chex) IIC → reg (read/write), Note : bits 6, 7 are Read only

bit
0 L Select 20kHz or REG12<4> (Pin 10 i/02)
1 L Not used
2 L Not used
3 L Select/Status of I/O 1
4 L Select/Status of I/O 2
5 L Not used
6 Read frequency of watchdog 1, LSB (bit 0) of 10 bit value
7 Read frequency of watchdog 1

Reg 13 (Reg 0Dhex) Reg → IIC (The watchdog is the vco frequency monitor)

bit Read frequency of watchdog 1, Note : bit 3 of 10 bit value.
0 Read frequency of watchdog 1
1 Read frequency of watchdog 1
2 Read frequency of watchdog 1
3 Read frequency of watchdog 1
4 Read frequency of watchdog 1
5 Read frequency of watchdog 1
6 Read frequency of watchdog 1
7 Read frequency of watchdog 1, MSB (10th bit) of 10 bits

Reg 14 (Reg 0Ehex) IIC → reg (read/write,) Note : bits 6, 7 are Read only

bit
0 L Select/Status of S1
1 L Select/Status of S2
2 L Select/Status of S3
3 Not used
4 Not used
5 Not used
6 Read frequ of Watchdog 2, Note : bit 0 of 10 bit value
7 Read frequ of Watchdog 2

Reg 15 (Reg 0Fhex) Reg → IIC (The watchdog is the vco frequency monitor)

bit	Read frequency of watchdog 2, Note : bit 3 of 10 bit value
0	Read frequency of watchdog 2
1	Read frequency of watchdog 2
2	Read frequency of watchdog 2
3	Read frequency of watchdog 2
4	Read frequency of watchdog 2
5	Read frequency of watchdog 2
6	Read frequency of watchdog 2
7	Read frequency of watchdog 2, MSB (10th bit) of 10 bits

Reg 16 (Reg 10hex) IIC → reg

bit			
0	L	Select 5 bit audio volume control	00H = mute 01H = -32.75dB : : : 1.25dB steps up to 1FH = +6db
1	L	Select 5 bit audio volume control	
2	L	Select 5 bit audio volume control	
3	L	Select 5 bit audio volume control	
4	L	Select 5 bit audio volume control	
5	L	Not used	
6	L	Select 4.000MHz or 8.000MHz clock speed (L = 8MHz)	
7	L	Select ANRS defeat (L = no ANRS, H = ANRS)	

Reg 17 (Reg 11hex) IIC → reg

bit			
0	L	Select LNB voltage. 8 bit value. LSB = bit 0	00H = 0 volts ref FFH = 2.4 volts ref 256 linear steps
1	L	Select LNB voltage. 8 bit value	
2	L	Select LNB voltage. 8 bit value	
3	L	Select LNB voltage. 8 bit value	
4	L	Select LNB voltage. 8 bit value	
5	L	Select LNB voltage. 8 bit value	
6	L	Select LNB voltage. 8 bit value	
7	L	Select LNB voltage. 8 bit value	

Reg 18 (Reg 12hex) IIC → reg (read/write)

bit		Not used	
0	L	Select video gain bits	00H = 0dB 01H = +0.202dB 02H = +0.404dB n = +0.202dB x n 3FH = +12.73dB
1	L	Select video gain bits	
2	L	Select video gain bits	
3	L	Select video gain bits	
4	L	Select video gain bits	
5	L	Select video gain bits	
6	L	Sync enable (for noisy video Pin 52 only H = enabled)	
7		Not used	

Reg 19 (Reg 13hex) IIC → reg (read/write)

bit		
0	L	Select PLL loop gain bits, default value for 50kHz modulation
1	H	Select PLL loop gain bits
2	H	Select PLL loop gain bits
3	L	Select PLL loop gain bits
4	H	Select PLL loop gain bits
5	L	Not used
6	L	Not used
7	L	Not used

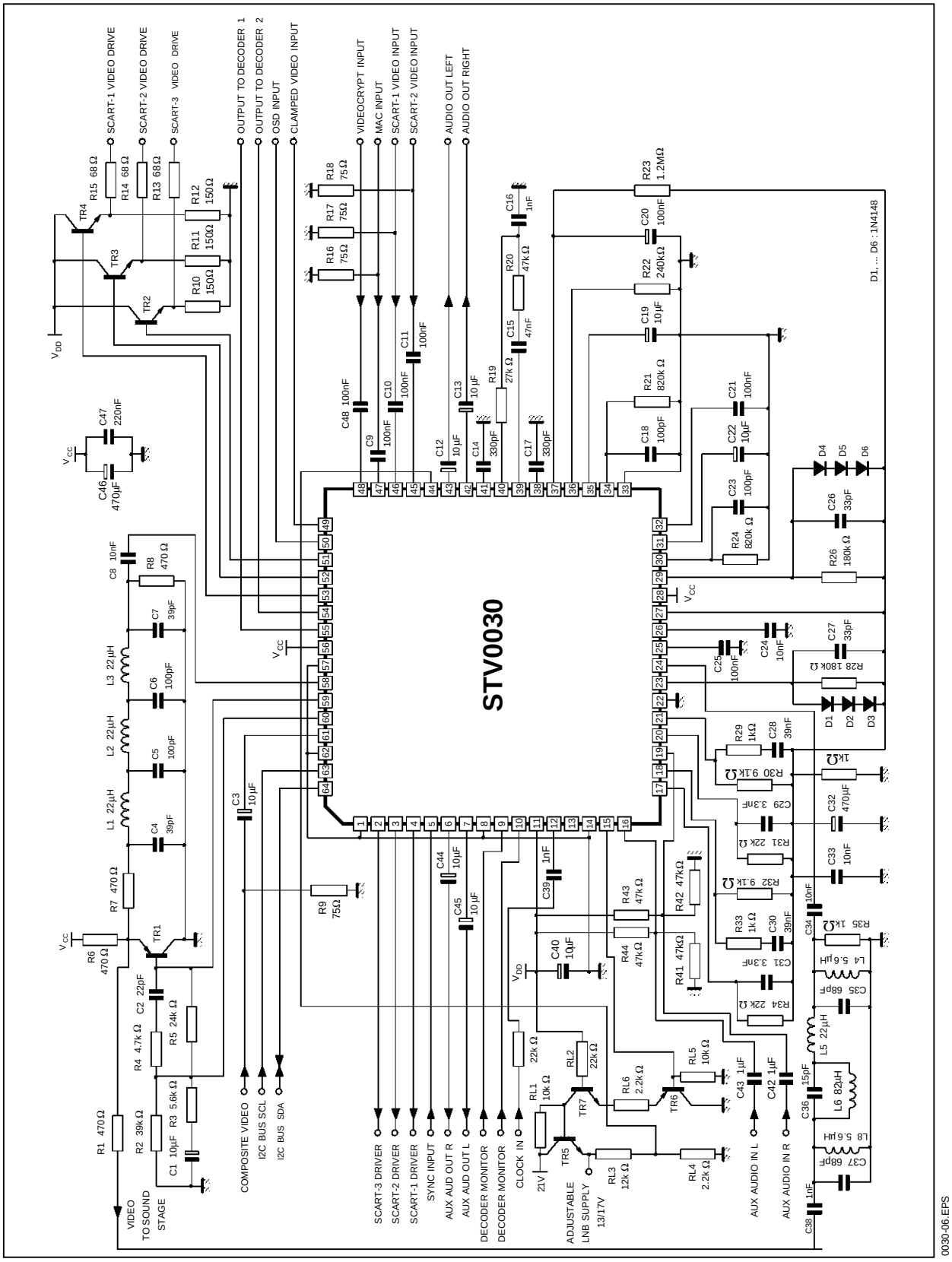
Audio Mux Table

Register	2		5		6	
Bits	**4**	**3**	**6**	**5**	**7**	**Function Selected**
	0	0	X	X	X	mono left / channel 1
	1	0	X	X	X	mono right / channel 2
	1	1	X	X	X	stereo left & right
	X	X	0	0	0	PLL audio 50µs de-emphasis
	X	X	X	0	1	Aux audio - no de-amphasis
	X	X	0	1	X	PLL audio J17 de-emphasis
	X	X	1	0	0	PLL audio 75µs de-emphasis
	X	X	1	1	X	PLL audio no de-emphasis

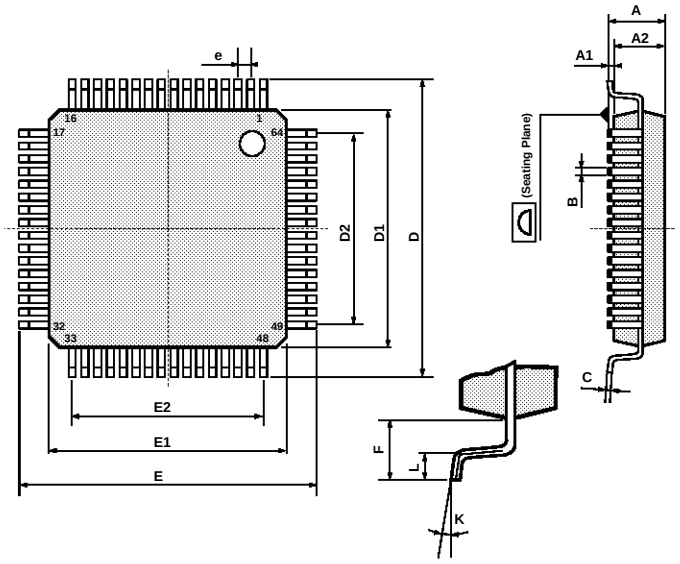
Register 19 Truth Table for Programmable PLL Gain

4	3	2	1	0	**Selected Nominal Carrier Modulation** (Example 49.1kHz means ±49.1kHz)
0	0	0	0	0	cal : do not use = 0.3373V offset on VCO
0	0	0	0	1	cal : do not use = 0.3053V offset on VCO
0	0	0	1	0	cal : do not use = 0.2763V offset on VCO
0	**0**	**0**	**1**	**1**	**calibration setting = 0.25V offset on VCO**
0	0	1	0	0	296kHz modulation
0	0	1	0	1	267kHz modulation
0	0	1	1	0	242kHz
0	0	1	1	1	218kHz
0	1	0	0	0	198kHz
0	1	0	0	1	179kHz
0	1	0	1	0	161kHz
0	1	0	1	1	146kHz
0	1	1	0	0	133kHz
0	1	1	0	1	120kHz
0	1	1	1	0	109kHz
0	1	1	1	1	98.3kHz
1	0	0	0	0	89.7kHz
1	0	0	0	1	80.9kHz
1	0	0	1	0	73.1kHz
1	0	0	1	1	66.0kHz
1	0	1	0	0	60.0kHz
1	0	1	0	1	54.4kHz
1	**0**	**1**	**1**	**0**	**49.1kHz = default power-up state**
1	0	1	1	1	44.3kHz
1	1	0	0	0	39.8kHz
1	1	0	0	1	35.9kHz
1	1	0	1	0	32.4kHz
1	1	0	1	1	29.1kHz
1	1	1	0	0	26.7kHz
1	1	1	0	1	24.3kHz
1	1	1	1	0	21.9kHz
1	1	1	1	1	19.7kHz

APPLICATION CIRCUIT



PACKAGE MECHANICAL DATA
64 PINS - PLASTIC QUAD FLAT PACK



PMPQFP64.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		12.00			0.472	
e		0.80			0.031	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		12.00			0.472	
F		1.60			0.063	
K	0° (min.), 7° (max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

PQFP64.TBL