CAT24C128

128-Kb I^2C CMOS Serial EEPROM

FEATURES

- **Supports Standard and Fast I^2C Protocol**
- **1.8V to 5.5V Supply Voltage Range**
- **64-Byte Page Write Buffer**
- **Hardware Write Protection for entire memory**
- **Schmitt Triggers and Noise Suppression Filters on I^2C Bus Inputs (SCL and SDA).**
- **Low power CMOS technology**
- **1,000,000 program/erase cycles**
- **100 year data retention**
- **Industrial temperature range**
- **RoHS-compliant 8-lead PDIP, SOIC and TSSOP packages**

For Ordering Information details, see page 14.

DEVICE DESCRIPTION

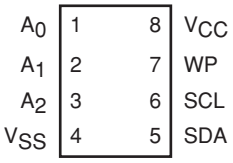
The CAT24C128 is a 128-Kb Serial CMOS EEPROM, internally organized as 256 pages of 64 bytes each, for a total of 16,384 bytes of 8 bits each.

It features a 64-byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I^2C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

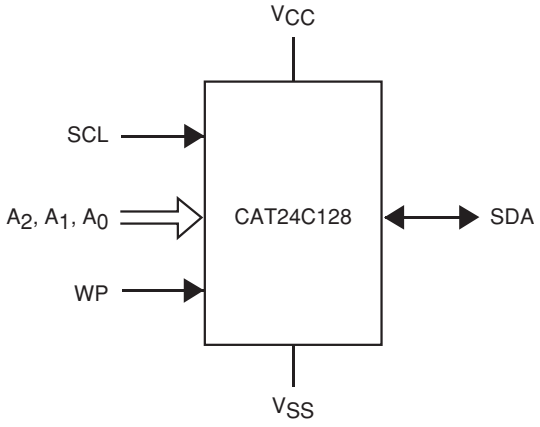
PIN CONFIGURATION

PDIP (L)
SOIC (W)
TSSOP (Y)



For the location of Pin 1, please consult the corresponding package drawing.

FUNCTIONAL SYMBOL



PIN FUNCTIONS

A_0, A_1, A_2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground

* Catalyst carries the I^2C protocol under a license from the Philips Corporation.

Doc. No. 1103, Rev. G

ABSOLUTE MAXIMUM RATINGS(1)

Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground(2)	-0.5 V to +6.5 V

RELIABILITY CHARACTERISTICS(3)

Symbol	Parameter	Min	Units
N_{END}(4)	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read at 400 kHz		1	mA
I_{CCW}	Write Current	Write		3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		1	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		1	μA
V_{IL}	Input Low Voltage		-0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Units
C_{IN}(3)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN}(3)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}(5)	WP Input Current	$V_{IN} < V_{IH}$	200	μA
		$V_{IN} > V_{IH}$	1	μA

Note:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5 V, 25°C

(5) When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x VCC), the strong pull-down reverts to a weak current source.

A.C. CHARACTERISTICS[1]

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C.

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		µs
$t_{HD:DAT}$	Data Hold Time	0		0		µs
$t_{SU:DAT}$	Data Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F[2]	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		µs
t_{AA}	SCL Low to SDA Data Out		3.5		0.9	µs
t_{DH}	Data Out Hold Time	100		100		ns
T_i[2]	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		µs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		µs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU}[2, 3]	Power-up to Ready Mode		1		1	ms

Note:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this paramete.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

POWER-ON RESET (POR)

The CAT24C128 incorporates Power-On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The CAT24C128 will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address pins accept the device address. When not driven, these pins are pulled LOW internally.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

FUNCTIONAL DESCRIPTION

The CAT24C128 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C128 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

I^2C BUS PROTOCOL

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 1). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 2). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices and must match the state of the external address pins. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 3). The Slave will also acknowledge all address bytes and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 4.

Figure 1. START/STOP Conditions

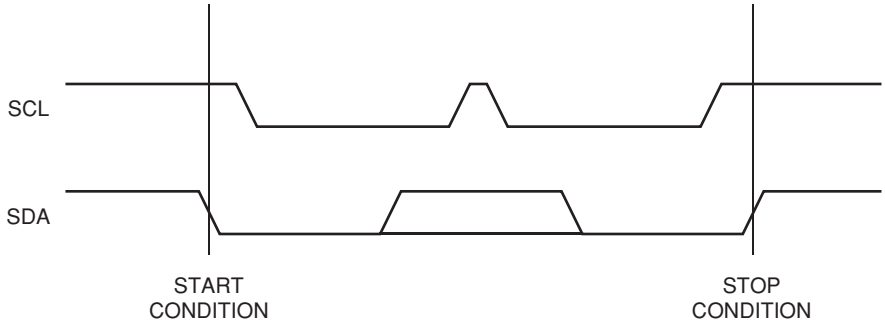


Figure 2. Slave Address Bits

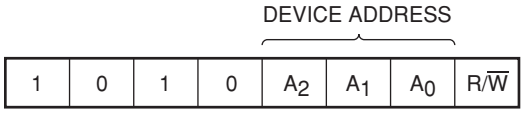


Figure 3. Acknowledge Timing

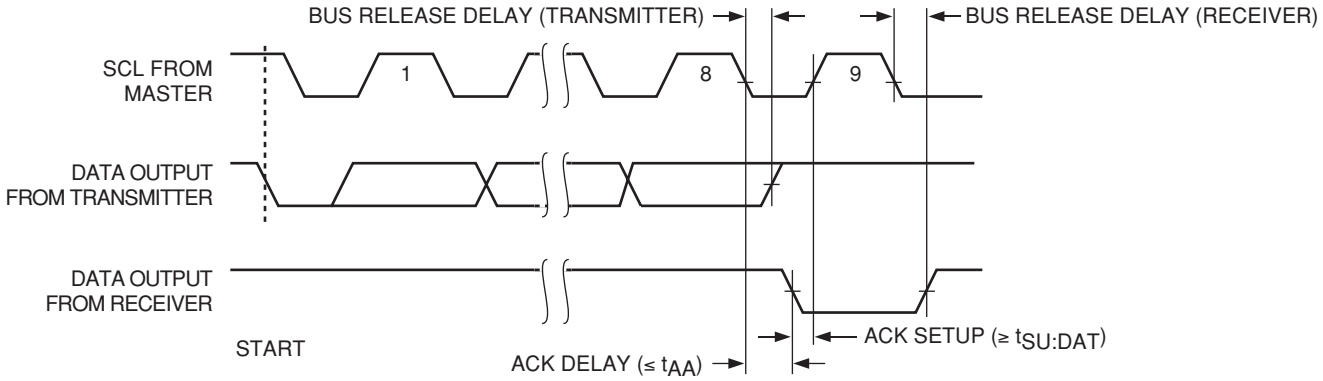
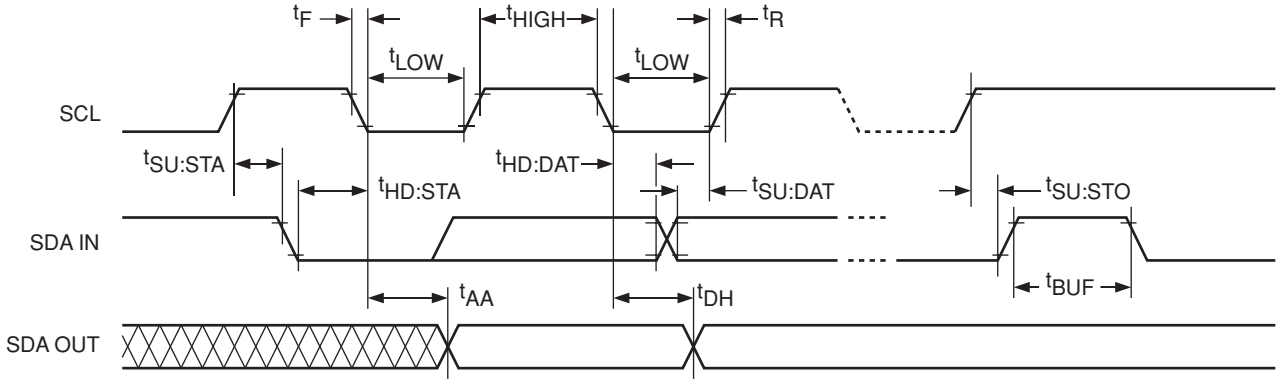


Figure 4. Bus Timing



WRITE OPERATIONS

Byte Write

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '0', the CAT24C128 will interpret the next two bytes as address bytes These bytes are used to initialize the internal address counter; the 2 most significant bits are 'don't care', the next 8 point to one of 256 available pages and the last 6 point to a location within a 64 byte page. A byte following the address bytes will be interpreted as data. The data will be loaded into the Page Write Buffer and will eventually be written to memory at the address specified by the 14 active address bits provided earlier. The CAT24C128 will acknowledge the Slave address, address bytes and data byte. The Master then starts the internal Write cycle by issuing a STOP condition (Figure 5). During the internal Write cycle (t_{WR}), the SDA output will be tri-stated and additional Read or Write requests will be ignored (Figure 6).

Page Write

By continuing to load data into the Page Write Buffer after the 1st data byte and before issuing the STOP condition, up to 64 bytes can be written simultaneously during one internal Write cycle (Figure 7). If more data bytes are loaded than locations available to the end of page, then loading will continue from the beginning of page, i.e. the page address is latched and the address count automatically increments to and then wraps-around at the page boundary. Previously loaded data can thus be overwritten by new data. What is eventually written to memory reflects the latest Page Write Buffer contents. Only data loaded within the most recent Page Write sequence will be written to memory.

Acknowledge Polling

The ready/busy status of the CAT24C128 can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the CAT24C128 will not acknowledge the Slave address.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C128. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 8). If the WP pin is HIGH during the strobe interval, the CAT24C128 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C128 is shipped erased, i.e., all bytes are FFh.

Figure 5. Byte Write Sequence

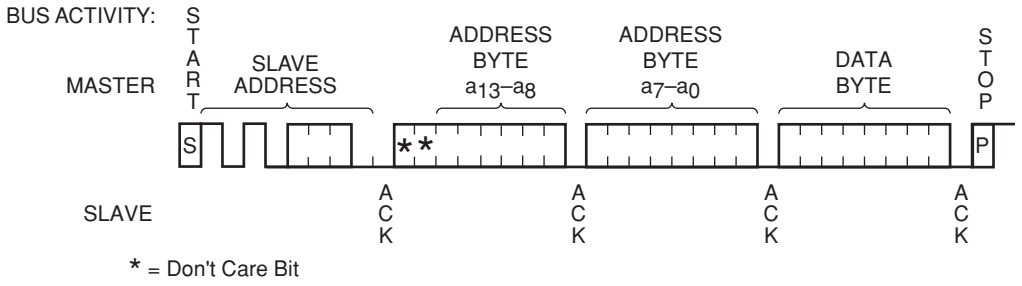


Figure 6. Write Cycle Timing

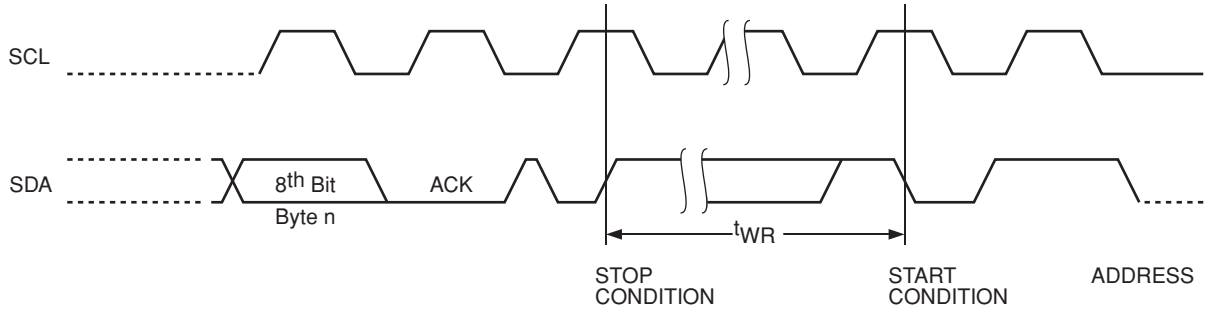


Figure 7. Page Write Sequence

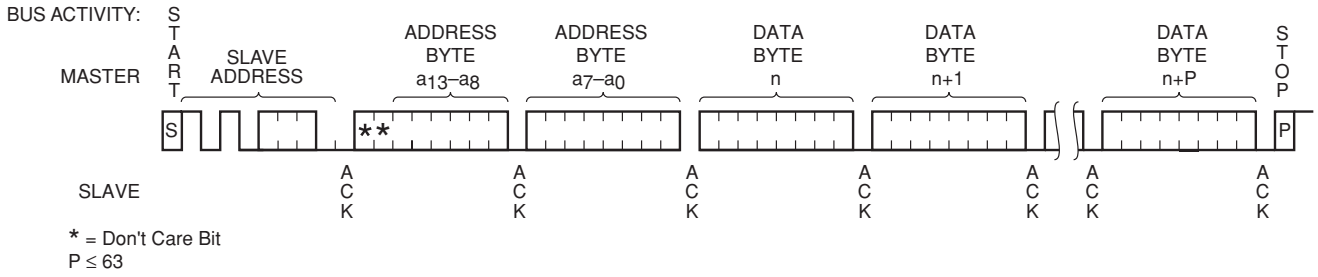
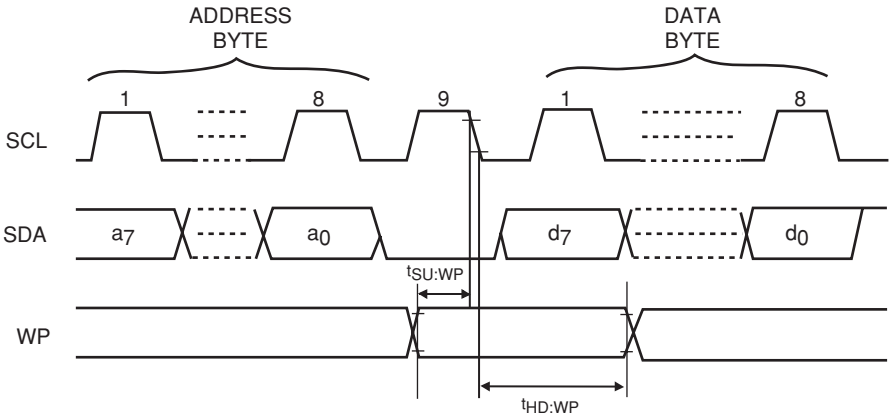


Figure 8. WP Timing



READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '1', the CAT24C128 will interpret this as a request for data residing at the current byte address in memory. The CAT24C128 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 9), the CAT24C128 returns to Standby mode.

Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes with data, the Master instead follows up with an Immediate Read sequence, then the CAT24C128 will use the 14 active addres bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24C128 returns to Standby mode.

Sequential Read

If during a Read session the Master acknowledges the 1st data byte, then the CAT24C128 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 11). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

Figure 9. Immediate Read Sequence and Timing

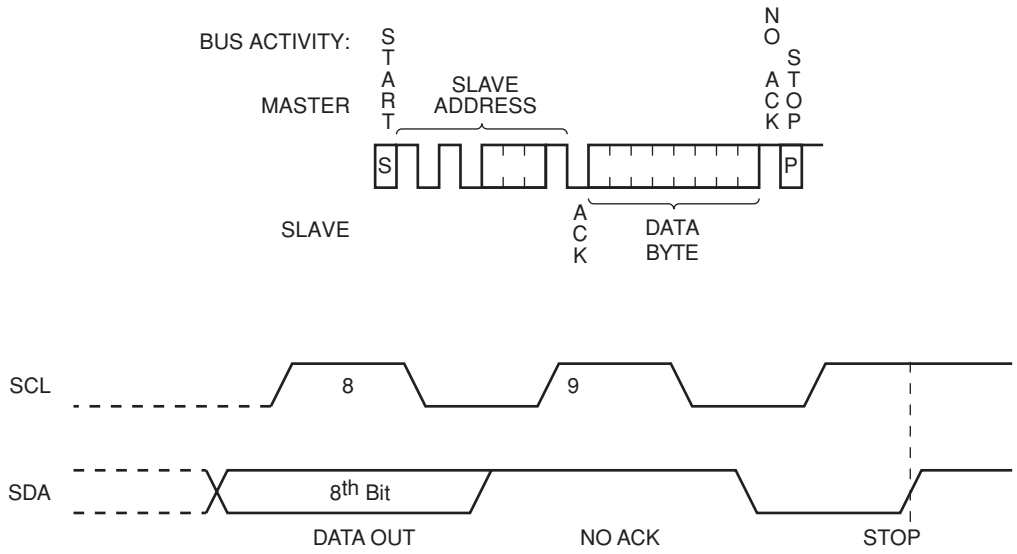


Figure 10. Selective Read Sequence

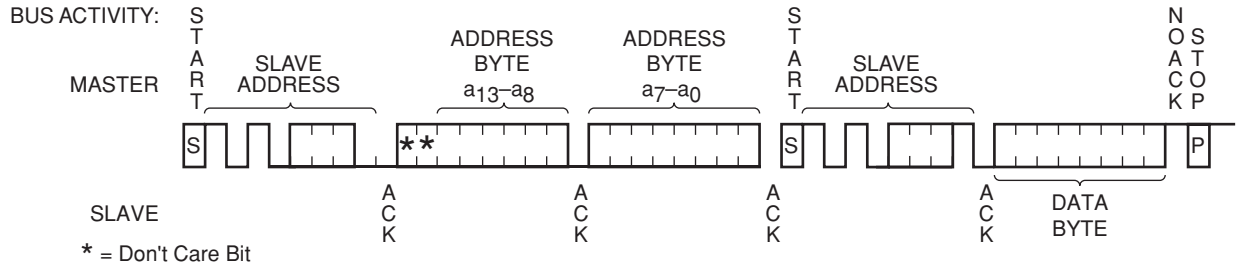
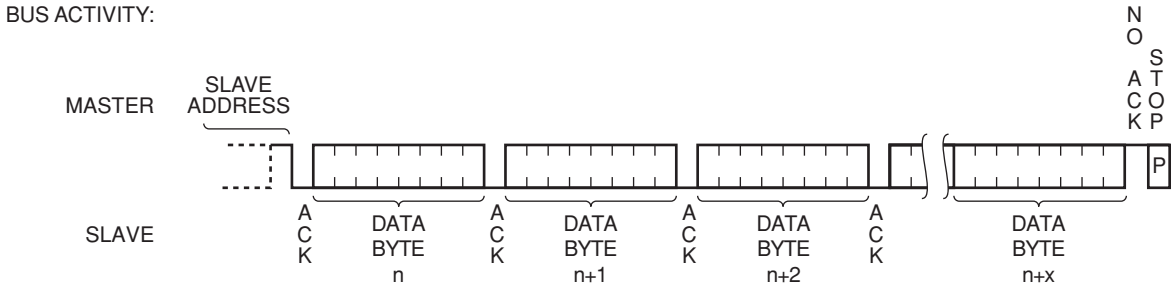
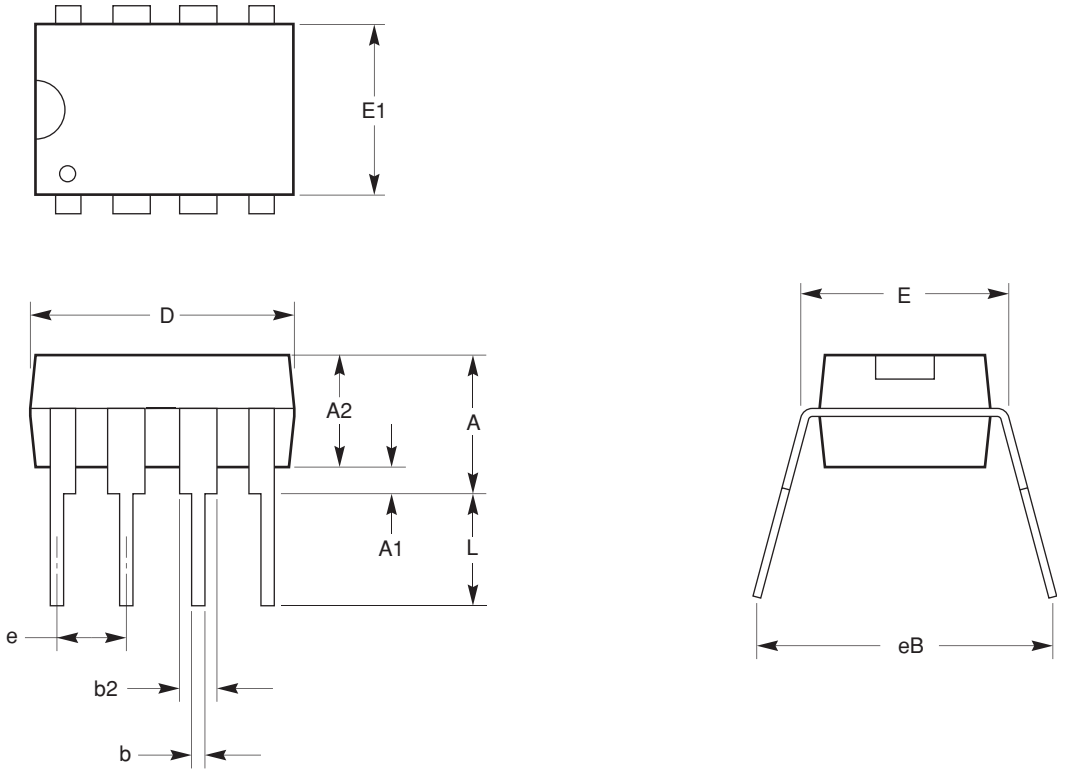


Figure 11. Sequential Read Sequence



8-LEAD 300 MIL WIDE PLASTIC DIP (L)



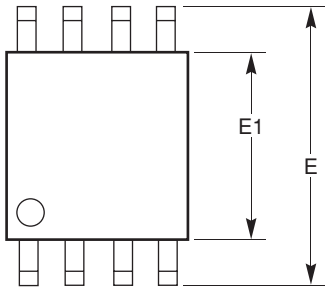
SYMBOL	MIN	NOM	MAX
A			4.57
A1	0.38		
A2	3.05		3.81
b	0.36	0.46	0.56
b2	1.14		1.77
D	9.02		10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54 BSC	
eB	7.87		9.65
L	0.115	0.130	0.150

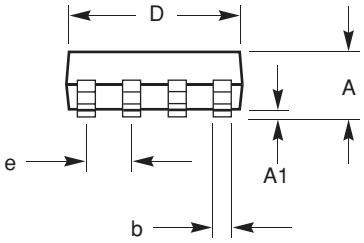
24C16_8-LEAD_DIP_(300P).eps

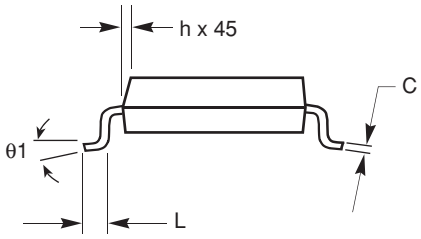
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MS001.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982

8-LEAD 150 MIL WIDE SOIC (W)







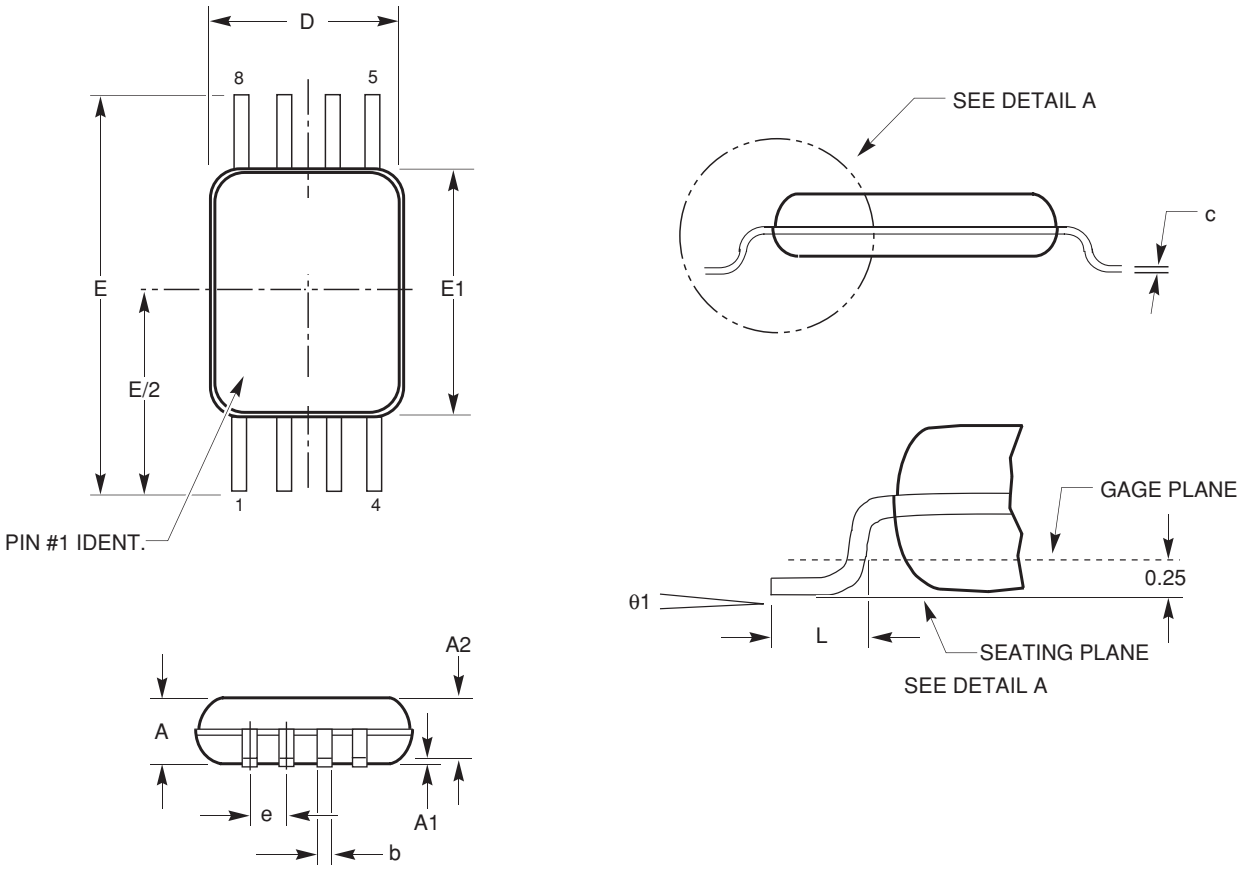
SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ1	0°		8°

24C16_8-LEAD_SOIC.eps

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MS-012.

8-LEAD TSSOP (Y)



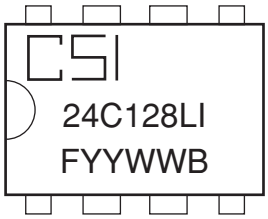
SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.4	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.75
θ1	0.00		8.00

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-153.

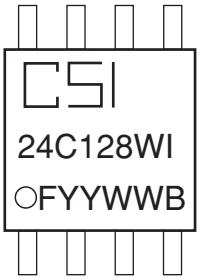
PACKAGE MARKING

8-Lead PDIP



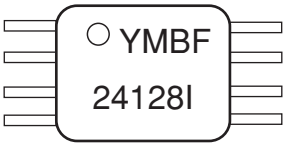
CSI = Catalyst Semiconductor, Inc.
24C128L = Device Code
I = Temperature Range
YY = Production Year
WW = Production Week
B = Product Revision
F = Lead Finish
4 = NiPdAu

8-Lead SOIC



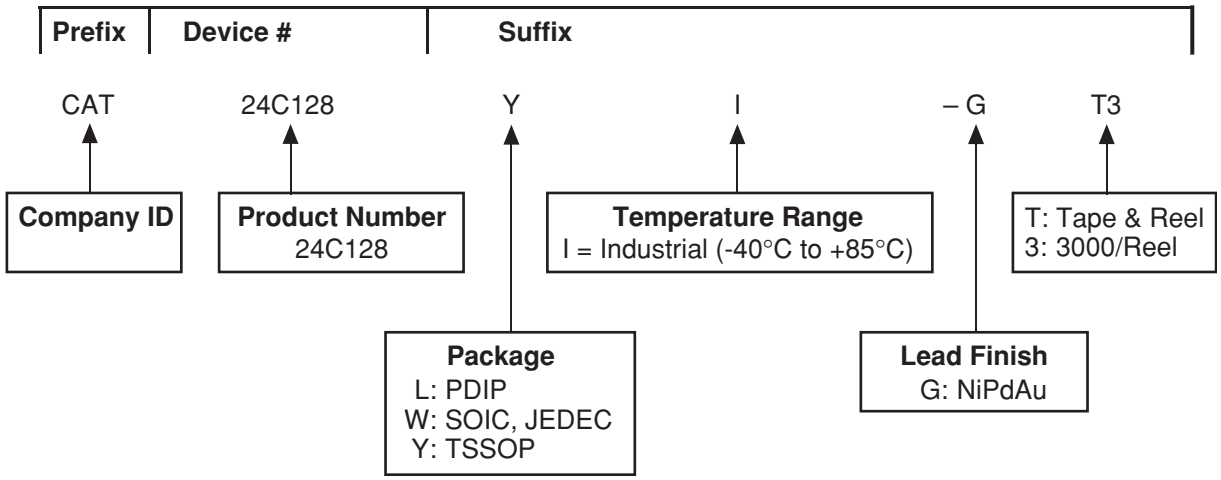
CSI = Catalyst Semiconductor, Inc.
24C128W= Device Code
I = Temperature Range
YY = Production Year
WW = Production Week
B = Product Revision
F = Lead Finish
4 = NiPdAu

8-Lead TSSOP



Y = Production Year
M = Production Month
B = Product Revision
24128 = Device Code
I = Temperature Range
F = Lead Finish
4 = NiPdAu

ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

(3) The device used in the above example is a CAT24C128YI-GT3 (TSSOP, Industrial Temperature, NiPdAu, Tape & Reel).

(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Revision	Comments
10/07/05	A	Initial Issue
11/16/05	B	Update Ordering Information Add Tape and Reel Specifications
02/02/06	C	Update A.C. Characteristics Update Ordering Information
03/13/06	D	Update A.C. Characteristics
04/26/06	E	Update Features Update Device Description Update Pin Configuration Update A.C. Characteristics Update Hardware Write Protecttion Add Figure 6a Add 8-Lead TSSOP Package Drawing Update Ordering Information Add 8-Lead TSSOP Package Marking
05/19/06	F	Update Features Update Device Description Update Pin Configuration Update Ordering Information Update D.C. Operating Characteristics Update Pin Impedance Characteristics Update A.C. Characteristics Add Power-On Reset (POR) Update 8-Lead PDIP Package Drawing Update 8-Lead SOIC Package Drawing Update 8-Lead TSSOP Package Drawing Update Tape and Reel
08/11/06	G	Update Features Update D.C. Operating Characteristics Update Pin Impedance Characteristics Update A.C. Test Conditions Update Power-On Reset (POR) Update Pin Description Update I^2C Bus Protocol Update Device Addressing Update Acknowledge Update Write Operations Update Byte Write Update Page Write Update Acknowledge Polling Add Delivery State Update Read Operations Update Selective Read Update Sequential Read Update Figure 1, 2, 3, 5, 6, 6a, 7, 8, 9 and 10 Update Part Marking Update Ordering Information

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