CMOS 8-BIT MICROCONTROLLER

TMP87PH40N, TMP87PH40F, TMP87PM40N, TMP87PM40F
TMP87PH40AN, TMP87PH40AF, TMP87PM40AN, TMP87PM40AF

The 87PH40/PH40A are a One-Time PROM microcontroller with low-power 128K bits (16K bytes) electrically programmable read only memory for the 87C840/CC40/CH40 system evaluation. The 87PM40/PM40A are a One-time PROM microcontroller with low-power 256K bits (32K bytes) electrically programmable read only memory for the 87CK40/M40A system evaluation. The 87PH40/PH40A/PM40/PM40A are pin compatible with the 87C840/CC40/CH40/CK40/CM40A. The operations possible with the 87C840/CC40/CH40/CK40/CM40A can be performed by writing programs to PROM. The 87PH40/PH40A/PM40/PM40A can write and verify in the same way as the TMM27256AD using an adaptor socket BM1136/BM1137 and an EPROM programmer.

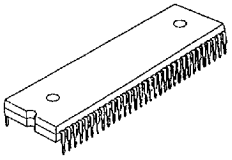
PART No	OTP	RAM	PACKAGE
TMP87PH40N TMP87PH40AN	16K × 8-bit	512 × 8-bit	SDIP64
TMP87PH40F TMP87PH40AF			QFP64
TMP87PM40N TMP87PM40AN	32K × 8-bit	1K × 8-bit	SDIP64
TMP87PM40F TMP87PM40AF			QFP64

PIN ASSIGNMENTS (TOP VIEW)

SDIP64

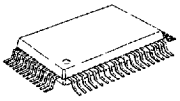
QFP64

SDIP64-P-750



TMP87PH40N
TMP87PM40N
TMP87PH40AN
TMP87PM40AN

QFP64-P-1420A



TMP87PH40F
TMP87PM40F
TMP87PH40AF
TMP87PM40AF

PIN FUNCTION

The 87PH40/PH40A/PM40/PM40A have two modes: MCU and PROM.

(1) MCU mode

In this mode, the 87PH40/PH40A/PM40/PM40A are pin compatible with the 87C840/CC40/CH40/CK40/CM40A (fix the TEST pin at low level).

(2) PROM mode

PIN NAME (PROM mode)	INPUT/OUTPUT	FUNCTIONS	PIN NAME (MCU mode)
A14 ~ A8 A7 ~ A0	Input	PROM address inputs	P76 ~ P70 P67 ~ P60
D7 ~ D0	I/O	PROM data input/outputs	P07 ~ P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
GND		0V	VSS
P37 ~ P30 P47 ~ P40 P54 ~ P50	I/O	Pull-up with resistance for input processing	
P11 P21 P77 P17 ~ P15		PROM mode setting pins. Be fixed at high level.	
P12, P10 P22, P20 $\overline{RESET}$		PROM mode setting pins. Be fixed at low level.	
XIN	Input	Connect an 8MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF VASS	Power Supply	0V (GND)	

OPERATIONAL DESCRIPTION

The following explains the 87PH40/PH40A/PM40/PM40A hardware configuration and operation. The configuration and functions of the 87PH40/PH40A are the same as those of the 87C840/CC40/CH40, 87PM40/PM40A are the same as those of the 87CK40/CM40A, except in that a one-time PROM is used instead of an on-chip mask ROM.

The 87PH40/PH40A/PM40/PM40A are placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. OPERATING MODE

The 87PH40/PH40A/PM40/PM40A have two modes: MCU and PROM.

1.1 MCU mode

The MCU mode is activated by fixing the TEST / VPP pin at low level.

In the MCU mode, operation is the same as with the 87C840/CC40/CH40/CK40/CM40A (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The 87PH40/PH40A have a 16K × 8-bit (addresses $C000_H$-$FFFF_H$ in the MCU mode, addresses 4000_H-$7FFF_H$ in the PROM mode), the 87PM40/PM40A have a 32K × 8-bit (address 8000_H-$FFFF_H$ in the MCU mode, address 0000_H-$7FFF_H$ in the PROM mode) of program memory (OTP).

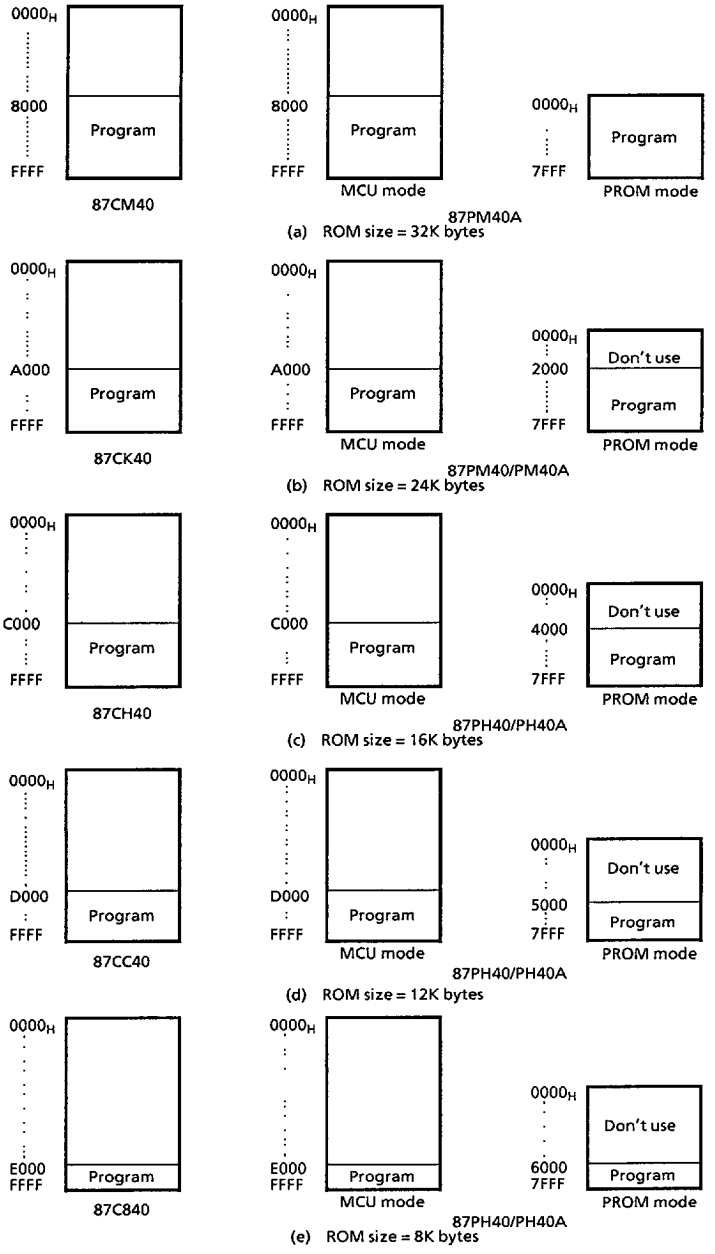


Figure 1-1. Program Memory Area

Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

1.1.2 Data Memory

The 87PH40/PM40A have an on-chip 512 × 8-bit data memory (static RAM). The 87PM40/PM40A have an on-chip 1K × 8-bit data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the 87PH40/PH40A/PM40/PM40A are the same as those of the 87C840/CC40/CH40/CK40/CM40A except that the TEST pin has is no built-in pull-down resistance.

(2) I/O ports

The I/O circuitries of 87PH40/PH40A/PM40/PM40A I/O ports the are the same as the code A type I/O circuitries of the 87C840/CC40/CH40/CK40/CM40A.

When using as an evaluator of other I/O codes (B, C, G), external pull-up resistors are required.

(a) In the case of code **C, G** (b) In the case of code **B**

Figure 1-2. I/O Circuitry Code and External Circuitry

1.2 PROM mode

The PROM mode is activated by setting the TEST, $\overline{RESET}$ pin and the ports P17-P10, P22-P20 and P77 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer. The high-speed programming mode can be used for program operation.

The 87PH40/PH40A/PM40/PM40A is not supported an *electric signature* mode, so the ROM type must be set to TMM27256 AD.

Set the adaptor socket switch to "P".

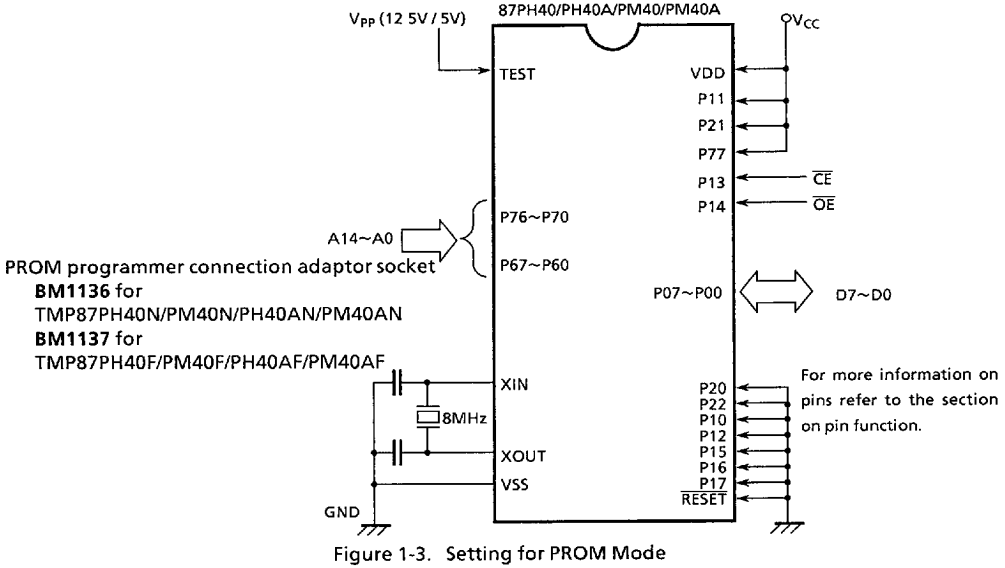


Figure 1-3. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed Programming Mode)

The high-speed programming mode is achieved by applying the program voltage (+ 12.5V) to the VPP pin when Vcc = 6V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (number of programmed times x 1ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

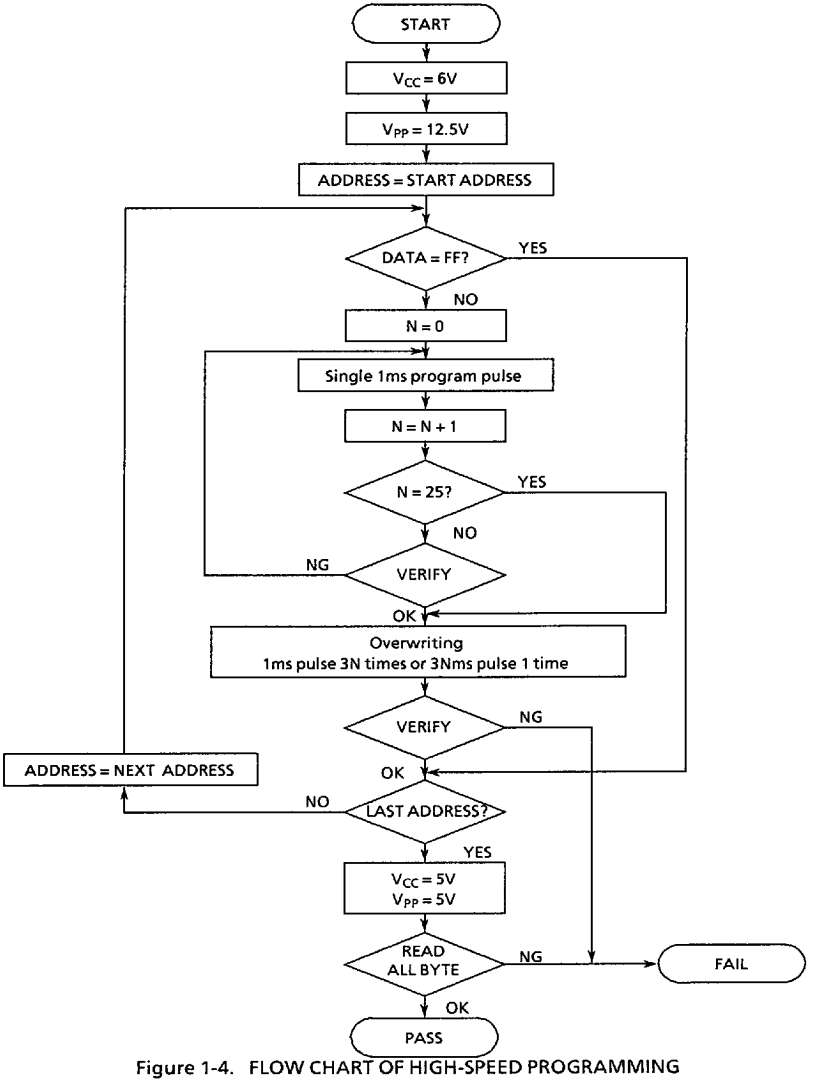


Figure 1-4. FLOW CHART OF HIGH-SPEED PROGRAMMING

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}		– 0 3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin , but include P2 and $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except port P2, $\overline{RESET}$	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P3, P4, P5, P6, P7	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	Σ I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	120	mA
	Σ I_{OUT2}	Port P3	120	
Power Dissipation [Topr = 70°C]	PD	TMP87PH40N/PM40N/PH40AN/PM40AN	600	mW
		TMP87PH40F/PM40F/PH40AF/PM40AF	350	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 8MHz	NORMAL1, 2 mode	4.5	6.0	V
				IDLE1, 2 mode			
			fc = 4 2MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32 768kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2 0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq$ 4 5V		V_{DD} × 0.70	V_{DD}	V
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		V_{DD} < 4.5V		V_{DD} × 0.90		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq$ 4 5V		0	V_{DD} × 0.30	V
	V_{IL2}	Hysteresis input				V_{DD} × 0 25	
	V_{IL3}		V_{DD} < 4.5V			V_{DD} × 0 10	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 6V		0.4	8.0	MHz
			V_{DD} = 2.7 to 6V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

D.C. CHARACTERISTICS

(V_{SS} = 0V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5V, V_{IN} = 5.5V/0V	–	–	± 2	μA
	I_{IN2}	Open drain ports and tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Low Current	I_{IL}	Push-pull ports	V_{DD} = 5.5V, V_{IN} = 0.4V	–	–	– 2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	KΩ
Output Leakage Current	I_{LO1}	Open drain ports	V_{DD} = 5.5V, VOUT = 5.5V	–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5V, VOUT = 5.5V/0V	–	–	± 2	
Output High Voltage	V_{OH1}	Push-pull ports	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	–	–	V
	V_{OH2}	Tri- state ports	V_{DD} = 4.5V, I_{OH} = – 0.7mA	4.1	–	–	
Output Low Voltage	V_{OL}	Except XOUT and port P3	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
Output Low Current	I_{OL3}	Port P3	V_{DD} = 4.5V, V_{OL} = 1.0V	–	20	–	mA
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5V, fc = 8MHz, fs = 32.768KHz, V_{IN} = 5.3V/0.2V; 87PH40/87PH40A	–	9	14	mA
			87PM40/87PM40A	–	12	18	
Supply Current in IDLE 1, 2 mode			87PH40/87PH40A	–	4	6	mA
			87PM40/87PM40A	–	4.5		
Supply Current in SLOW mode			V_{DD} = 3.0V, fs = 32.768KHz, V_{IN} = 2.8V/0.2V	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5V, V_{IN} = 5.3V/0.2V	–	0.5	10	μA

Note 1 : Typical values show those at Topr = 25°C, V_{DD} = 5V

Note 2 : Input Current ; The current through pull-up or pull-down resistor is not included.

A / D CONVERSION CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS		Min.	TIPE	Max.	UNIT
Analog Reference Voltage	V_{AREF}			87PH40/PM40: V_{DD} – 1.5; 87PH40A/PM40A: 2.7	–	V_{DD}	V
	V_{ASS}			V_{SS}	–	1.5	
Analog Reference Voltage Range	ΔV_{AREF}				2.5	–	V
Analog Input Voltage	V_{AIN}			V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}			–	0.5	1.0	mA
Nonlinearity Error		87PH40, 87PM40	V_{DD} = 5.0V, V_{SS} = 0.0V, V_{AREF} = 5.000V, V_{ASS} = 0.000V	–	–	± 1	LSB
Zero Point Error				–	–	± 1	
Full Scale Error		87PH40A, 87PM40A	V_{DD} = 2.7 to 5.0V, V_{SS} = 0.0V, V_{AREF} = 2.700V, 5.000V, V_{ASS} = 0.000V	–	–	± 1	
Total Error				–	–	± 1	

Note : $\Delta V_{AREF} = V_{AREF} - V_{ASS}$

A.C. CHARACTERISTICS

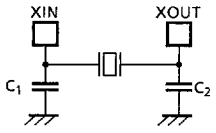
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8MHz	62.5	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

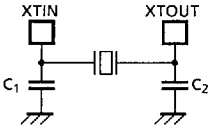
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, Topr = – 30 to 70°C)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8MHz	KYOCERA	KBR8.0M	30pF	30pF
		4MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8MHz	TOYOCOM	210B 8.0000	20pF	20pF
		4MHz	TOYOCOM	204B 4 0000		
Low-frequency Oscillation	Crystal Oscillator	32.768kHz	NDK	MX-38T	15pF	15pF



(1) High-frequency Oscillation



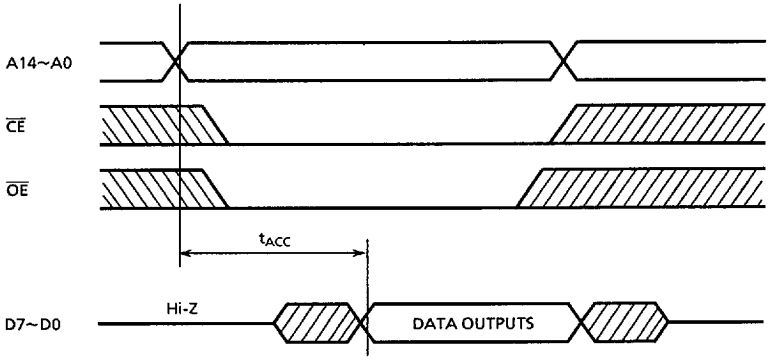
(2) Low-frequency Oscillation

D.C./A.C. CHARACTERISTICS (PROM mode) (V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	V_{CC} × 0.12	V
Power Supply Voltage	V_{CC}		4.75	–	6.0	V
Program Power Supply Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	–	1.5tcyc + 300	–	ns

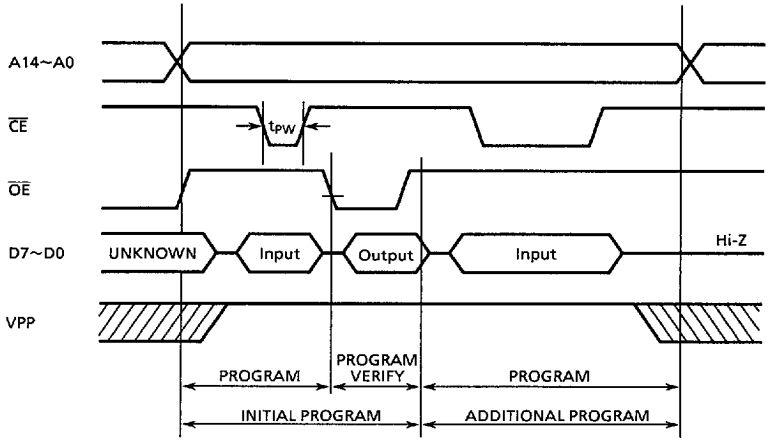
Note : tcyc = 500ns at 8MHz



TIMING WAVEFORMS OF READ OPERATION

(2) High-Speed Programming Operation

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	V_{CC} × 0.12	V
Power Supply Voltage	V_{CC}		5.75	–	6.0	V
Program Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0V	0.95	1.0	1.05	ms



TIMING WAVEFORMS OF PROGRAMMING OPERATION