Ultra-Low Distortion, High Speed Audio Operational Amplifier

SSM-2131

FEATURES

- **Low Distortion – DC to 40kHz, A_V = +10 ..... 0.01% Typ**
- **High Slew Rate ..... 40V/μs Min**
- **Gain-Bandwidth Product ..... 10MHz Typ**
- **High Gain ..... 200,000 Typ**
- **Common-Mode Rejection ..... 80dB Min**

APPLICATIONS

- **Power Amplifier Driver**
- **Active Filter Circuits**
- **Parametric Equalizers**
- **Graphic Equalizers**
- **Mixing Consoles**
- **Voltage Summers**
- **Active Crossover Networks**

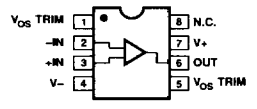
GENERAL DESCRIPTION

The SSM-2131 is a fast JFET input operational amplifier intended for use in audio applications. The SSM-2131 offers a symmetric 50V/μs slew rate for low distortion and is internally compensated for unity gain operation. Power supply current is less than 6.5mA. Unity-gain stability, a wide full-power bandwidth of 800kHz, and excellent ability to handle transient overloads make the SSM-2131 an ideal amplifier for use in high performance audio amplifier circuits.

The SSM-2131's common-mode rejection of 80dB minimum over a ±11 range is exceptional for a high-speed amplifier. High CMR, combined with a minimum 500V/mV gain into a 10kΩ load ensures excellent linearity in both noninverting and inverting gain configurations. This means that distortion will be very low over a wide range of circuit configurations. The low offset provided by the JFET input stage often eliminates the need for AC coupling or for external offset trimming.

The SSM-2131 conforms to the standard 741 pinout with nulling to V–. The SSM-2131 upgrades the performance of circuits using the TL071 by direct replacement.

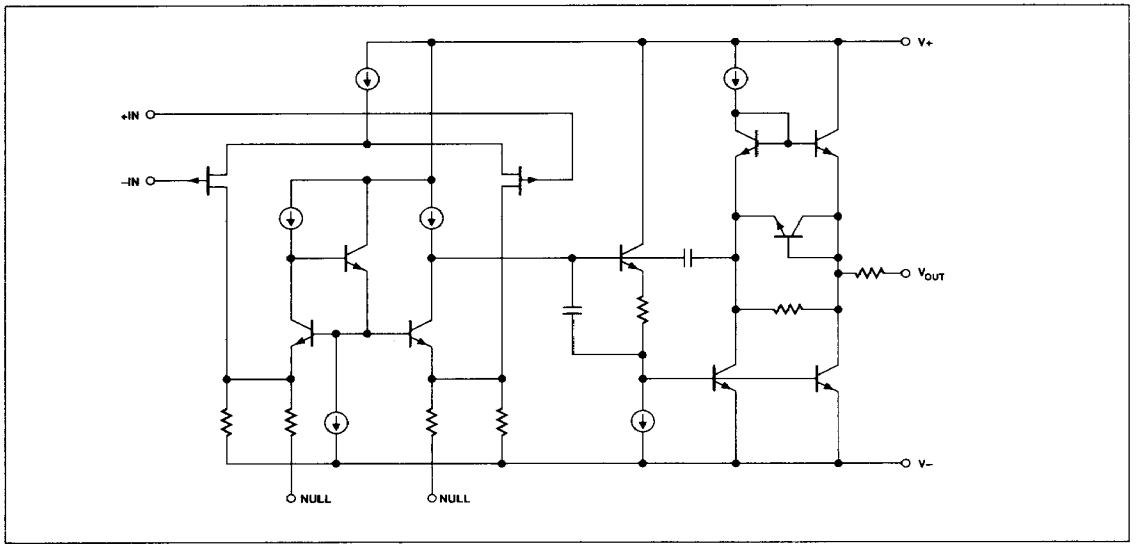
PIN CONNECTIONS



PLASTIC MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)

SIMPLIFIED SCHEMATIC



ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN	
SSM2131P	SSM2131S	XIND*

*XIND = –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Input Voltage (Note 1) ..... ±20V
Differential Input Voltage (Note 1) 40V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range ..... –40°C to +85°C
Junction Temperature ..... –65°C to +175°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			SSM-2131			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR		40	50	–	V/µs
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	MHz
Full-Power Bandwidth	BW_p	(Note 2)	600	800	–	kHz
Total Harmonic Distortion	THD	DC to 40kHz, R_L = 10kΩ, A_V = +10	–	0.01	–	%
Voltage Noise Density	e_n	f_O = 10Hz f_O = 1kHz	– –	38 13	– –	nV/√Hz
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	pA/√Hz
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ, V_O = ±10V R_L = 2kΩ, T_j = 25°C R_L = 1kΩ	500 200 100	900 260 170	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	V
Offset Voltage	V_{OS}		–	1.5	6.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_j = 25°C	–	130	250	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_j = 25°C	–	6	50	pA
Input Voltage Range	IVR	(Note 1)	±11.0	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	92	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	12	50	µV/V
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.5	mA
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	mA
Settling Time	t_s	10V Step 0.01% (Note 3)	–	0.9	1.2	µs
Overload Recovery Time	t_{OR}		–	700	–	ns

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	SSM-2131 TYP	SSM-2131 MAX	UNITS
Phase Margin	ϕ_O	0dB Gain	–	47	–	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	pF
Supply Voltage Range	V_S		±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling time is guaranteed but not tested.
4. Guaranteed but not tested.

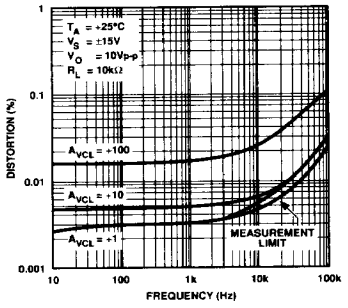
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	SSM-2131 TYP	SSM-2131 MAX	UNITS
Slew Rate	SR	$R_L = 2k\Omega$	40	50	–	V/µs
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1) $R_L = 2k\Omega$ $V_O = \pm 10V$	200 100	500 160	– –	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±11.0	+12.3 −11.8	–	V
Offset Voltage	V_{OS}		–	2.0	7.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	8	–	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.6	2.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.06	0.4	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 −12.0	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	–	6	50	µV/V
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.1	6.5	mA
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	mA

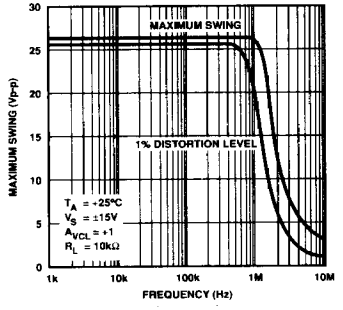
NOTES:
1. $T_J = 85°C$.
2. Guaranteed by CMR test.

TYPICAL PERFORMANCE CHARACTERISTICS

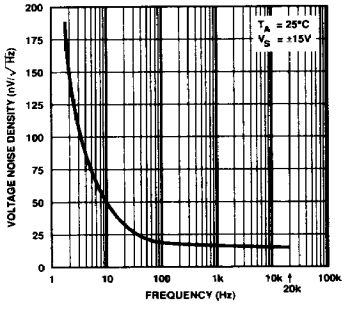
DISTORTION vs FREQUENCY



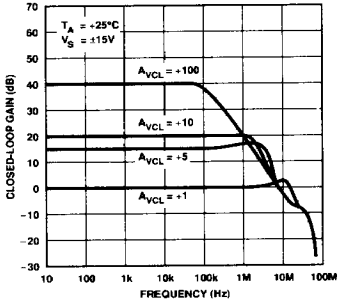
MAXIMUM OUTPUT SWING vs FREQUENCY



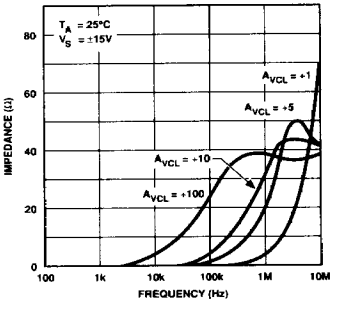
VOLTAGE NOISE DENSITY vs FREQUENCY



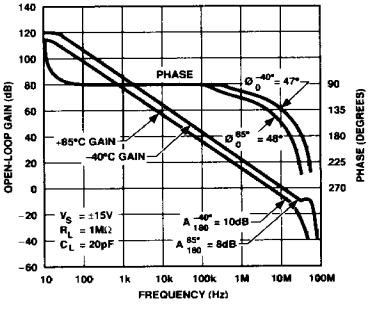
CLOSED-LOOP GAIN vs FREQUENCY



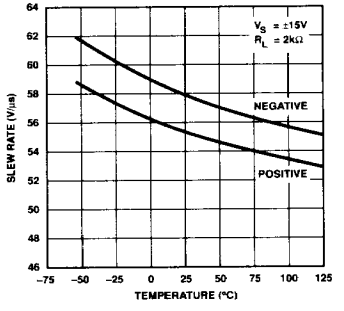
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



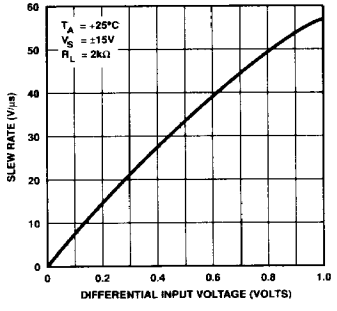
OPEN-LOOP GAIN, PHASE vs FREQUENCY



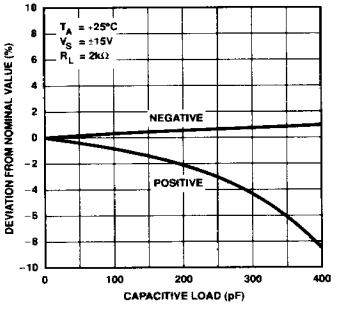
SLEW RATE vs TEMPERATURE



SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

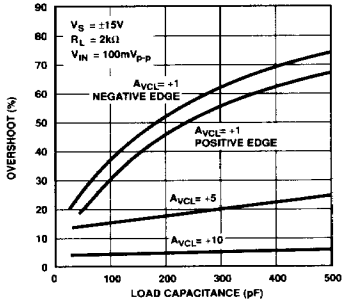


SLEW RATE vs CAPACITIVE LOAD

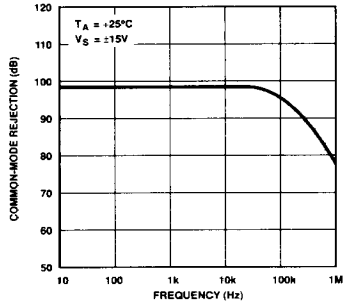


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

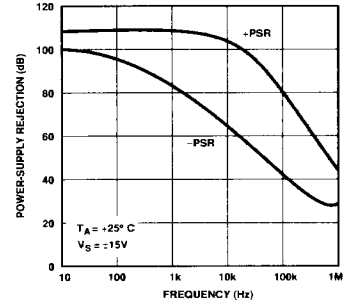
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



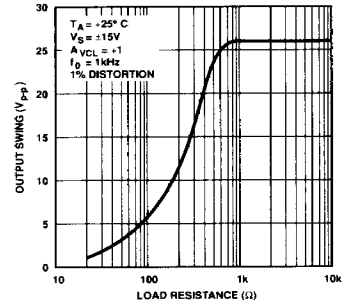
COMMON-MODE REJECTION vs FREQUENCY



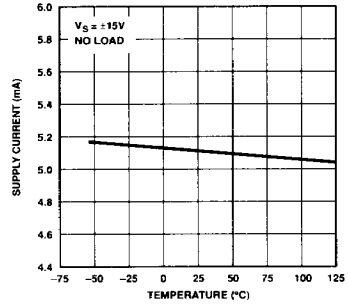
POWER-SUPPLY REJECTION vs FREQUENCY



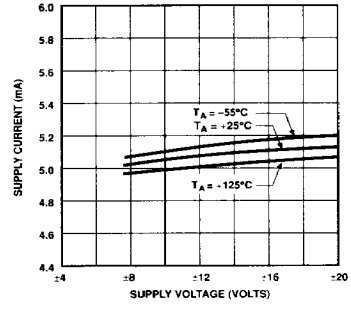
OUTPUT SWING vs LOAD RESISTANCE



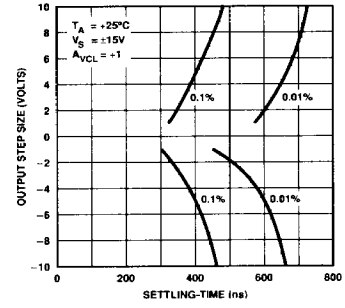
SUPPLY CURRENT vs TEMPERATURE



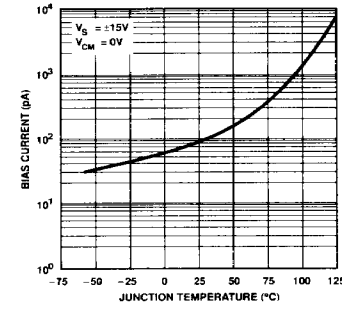
SUPPLY CURRENT vs SUPPLY VOLTAGE



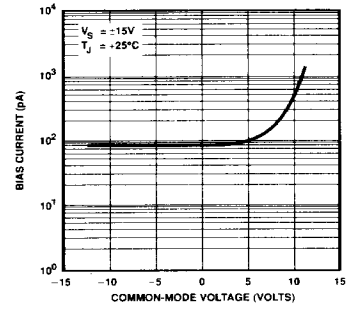
SETTLING-TIME vs STEP SIZE



BIAS CURRENT vs JUNCTION TEMPERATURE



BIAS CURRENT vs COMMON-MODE VOLTAGE



APPLICATIONS INFORMATION

The SSM-2131 combines speed with a high level of input precision usually found only with slower devices. Well-behaved AC performance in the form of clean transient response, symmetrical slew rates and a high degree of forgiveness to supply decoupling are the hallmarks of this amplifier. AC gain and phase response are quite independent of temperature or supply voltage. Figure 1 shows the SSM-2131's small-signal response. Even with 75pF loads, there is minimal ringing in the output waveform. Large-signal response is shown in Figure 2. This figure clearly shows the SSM-2131's exceptionally close matching between positive and negative slew rates. Slew rate symmetry decreases the DC offset a system encounters when processing high-frequency signals, and thus reduces the DC current necessary for load driving.

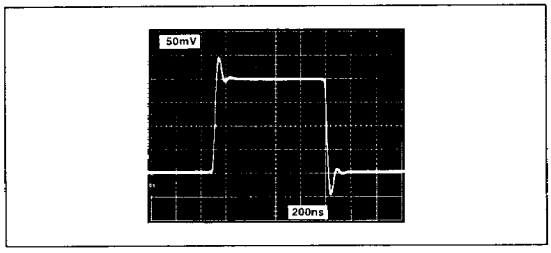


FIGURE 1: *Small-Signal Transient Response, Z_L = 2kΩ//75pF*

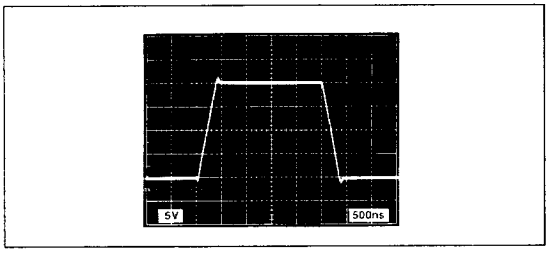


FIGURE 2: *Large-Signal Transient Response, Z_L = 2kΩ//75pF*

As with most JFET-input amplifiers, the output of the SSM-2131 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier.

For most applications, a 0.1µF to 0.01µF capacitor should be placed between each supply pin and ground.

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 10kΩ to 100kΩ potentiometer as shown in Figure 3. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V– supply.

Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a 1MΩ resistor to the positive supply rail.

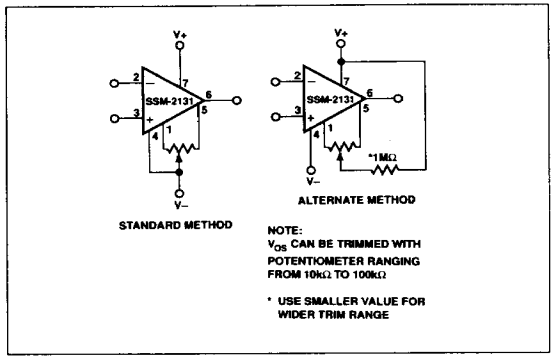


FIGURE 3: *Input Offset Voltage Nulling*

VOLTAGE SUMMING

Because of its extremely low input bias current and large unity-gain bandwidth, the SSM-2131 is ideal for use as a voltage summer or adder.

The following figures show both an inverting and noninverting voltage adder.

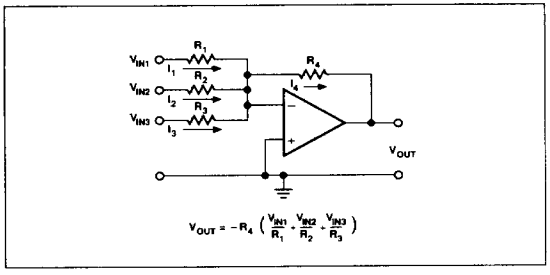


FIGURE 4: *Inverting Adder*

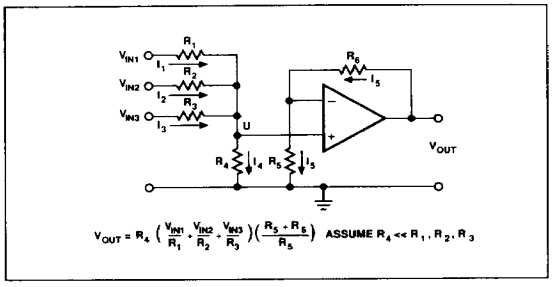


FIGURE 5: *Noninverting Adder*

CURRENT FEEDBACK

AUDIO POWER AMPLIFIER

The SSM-2131 can be used as the input buffer in a current feedback audio power amplifier as shown in Figure 6. This design is capable of very good performance as shown in Figures 7, 8 and 9. At 1kHz and 50 watts output into an 8Ω load, the amplifier generates just 0.002% THD, and is flat to 1MHz. The slew rate for the overall amplifier is more than adequate at 300V/μs and is responsible for the very low dynamic intermodulation distortion (DIM-100) that was measured at just 0.0017% at 50 watts output into 8 ohms. The total amplifier idling current for all tests was approximately 300mA; the V+/V++ and V–/V— power supplies were both ±40V; and the gain was set to 24.0.

In a current feedback amplifier, a unity or low gain input buffer drives a low impedance network. Any differential current that flows in the collectors of the buffer (SSM-2131) output transistors is fed, via the two complementary Wilson current mirrors A and B, to a high impedance gain node where the high output voltage is generated.

This voltage is then buffered by a double emitter follower driver stage and fed to the complementary power MOSFET output stage. No RC compensation network to ground or output inductor is required at the output of this amplifier to make it stable. As the 100kHz square wave response shows, there's no evidence of any instability in the circuit. Capacitive load compensation can be provided by the components marked TBD on the amplifier schematic. These were not used in the test, however.

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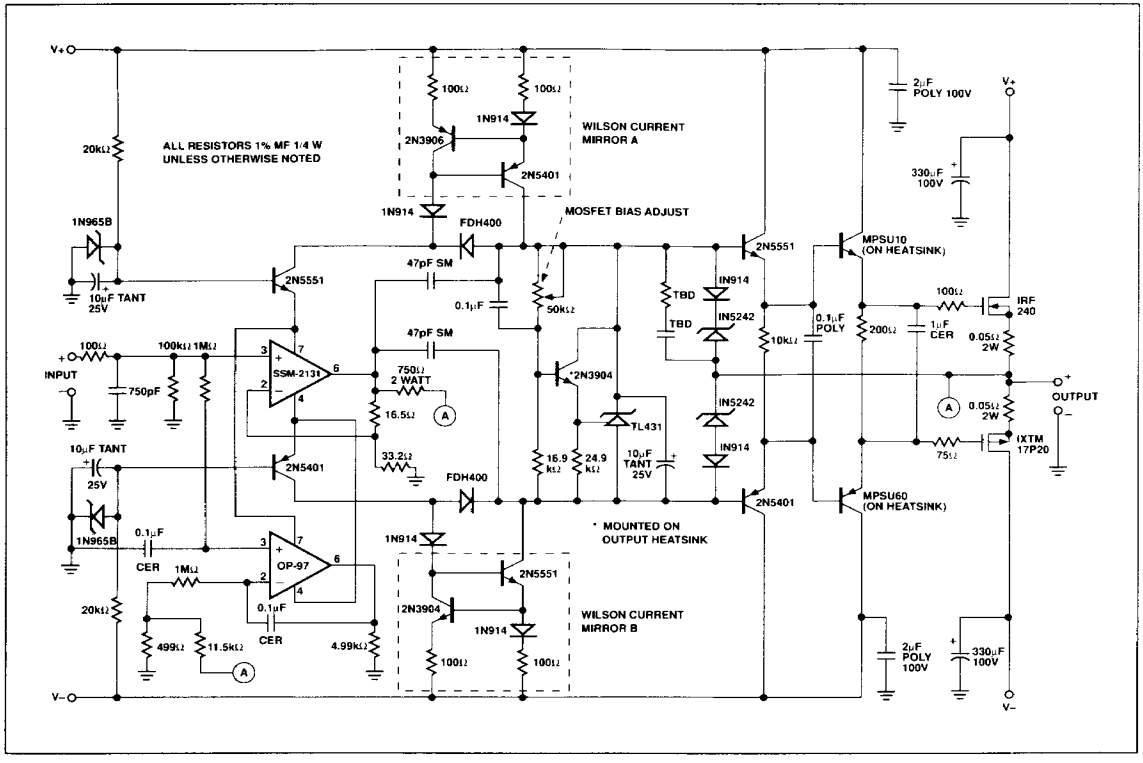

FIGURE 6: *Audio Power Amplifier Schematic*

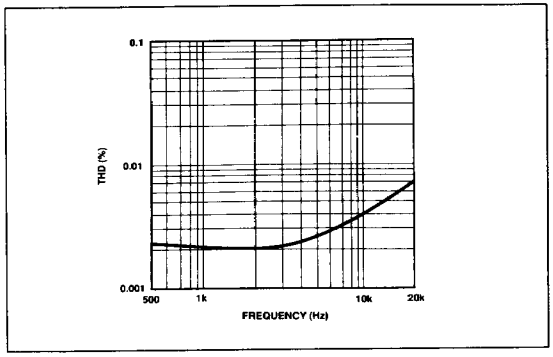

FIGURE 7: *THD vs. Frequency (at 50W into 8Ω).*

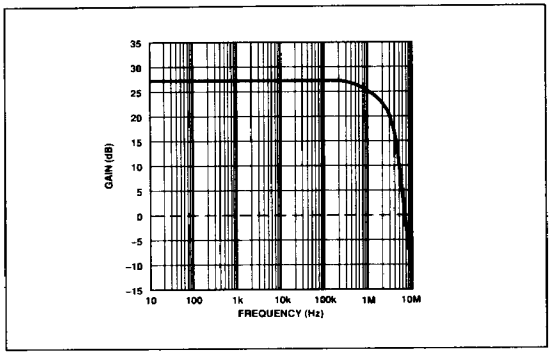

FIGURE 8: *Frequency Response*

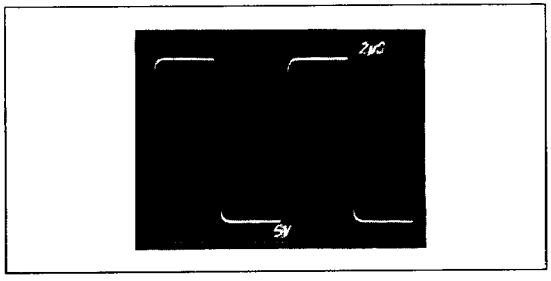

FIGURE 9: *100kHz Square Wave into 8Ω.*

One problem that is commonly encountered with current feedback amplifiers is that the mismatch between the two current mirrors A and B forces a small bias current to appear at the input buffer's output terminal. This bias current (usually in the range of 1-100μA) is multiplied by the feedback resistor of 750Ω and generates an output offset that could be tens of millivolts in magnitude. Matched transistors could be used in the current mirrors, but these do not completely eliminate the output offset problem.

An inexpensive solution is to use a low power precision DC op amp, such as the OP-97, to control the amplifier's DC characteristics, thus overriding the DC offset due to mismatch in the current feedback loop. The OP-97 acts as a current output DC-servo amplifier that injects a compensating current into the emitters of the low voltage regulator transistors (that power the SSM-2131) to correct for current mirror mismatch. Since the OP-97 is set for an overall input-to-output gain of 24.0 as well, the DC output offset is equal to the OP-97's V_{OS} x 24.0, which is roughly 1 millivolt. Thus, any offset trimming can be completely eliminated. Together, the SSM-2131 and OP-97 provide a level of performance that exceeds most of the requirements for audio power amplifers. The driver circuit can handle several pairs of power MOSFETs in the output stage if required. This topology can be used in circuits that must deliver several hundreds of watts to a load by using higher voltage transistors in the driver stage. Operation with rail voltages in excess of ±100V is possible. If more gain is desired, the SSM-2131 input buffer can have its gain increased from the nominal value of 1.5 used in this example to as much as 10 before its bandwidth drops below that of the current feedback section.

DRIVING A HIGH-SPEED ADC

The SSM-2131's open-loop output resistance is approximately 50Ω. When feedback is applied around the amplifier, output resistance decreases in proportion to closed-loop gain divided by open-loop gain (A_{VCL}/A_{VOL}). Output impedance increases as open-loop gain rolls-off with frequency. High-speed analog-to-digital converters require low source impedances at high frequency. Output impedance at 1MHz is typically 5Ω for an SSM-2131 operating at unity-gain. If lower output impedances are required, an output buffer may be placed at the output of the SSM-2131.

HIGH-CURRENT OUTPUT BUFFER

The circuit in Figure 10 shows a high-current output stage for the SSM-2131 capable of driving a 75Ω load with low distortion. Output current is limited by R_1 and R_2. For good tracking between the output transistors Q_1, Q_2, and this biasing diodes D_1 and D_2, thermal contact must be maintained between the transistor and its associated diode. If good thermal contact is not maintained, R_1 and R_2 must be increased to 5-6Ω in order to prevent thermal runaway. Using 5Ω resistors, the circuit easily drives a 75Ω load (Figure 11). Output resistance is decreased and heavier loads may be driven by decreasing R_1 and R_2.

Base current and biasing for Q_1 and Q_2 are provided by two current sources, the SSM-2131 and the JFET. The 2kΩ potentiometer in the JFET current source should be trimmed for optimum transient performance. The case of the SSM-2210 should be connected to V–, and decoupled to ground with a 0.1μF capacitor. Compensation for the SSM-2131's input capacitance is provided by C_C. The circuit may be operated at any gain, in the usual op amp configurations.

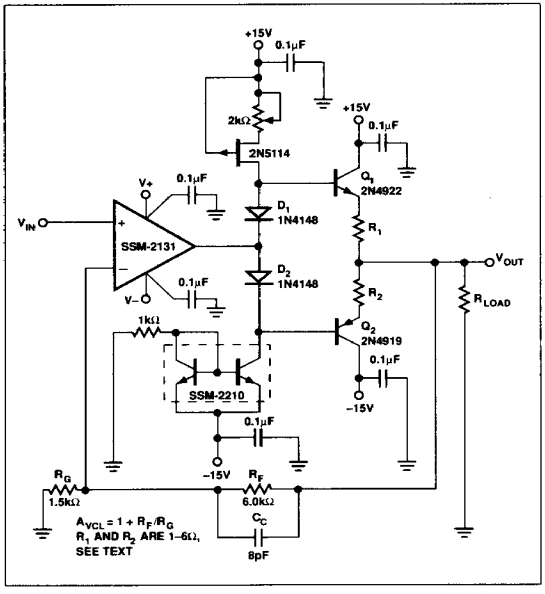

FIGURE 10: *High-Current Output Buffer*

DRIVING CAPACITIVE LOADS

Best performance will always be achieved by minimizing input and load capacitances around any high-speed amplifier. However, the SSM-2131 is guaranteed capable of driving a 100pF capacitive load over its full operating temperature range while operating at any gain including unity. Typically, an SSM-2131 will drive more than 250pF at any temperature. Supply decoupling does affect capacitive load driving ability. Extra care should be given to ensure good decoupling when driving capacitive loads; between 1μF and 10μF should be placed on each supply rail.

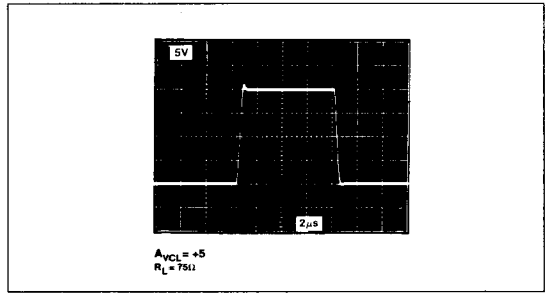

FIGURE 11: *Output Buffer Large-Signal Response*

Large capacitive loads may be driven utilizing the circuit shown in Figure 12. R_1 and C_1 introduce a small amount of feedforward compensation around the amplifier to counteract the phase lag induced by the ouput impedance and load capacitance. At DC and low frequencies, R_1 is contained within the feedback loop. At higher frequencies, feedforward compensation becomes increasingly dominant, and R_1's effect on output impedance will become more noticeable.

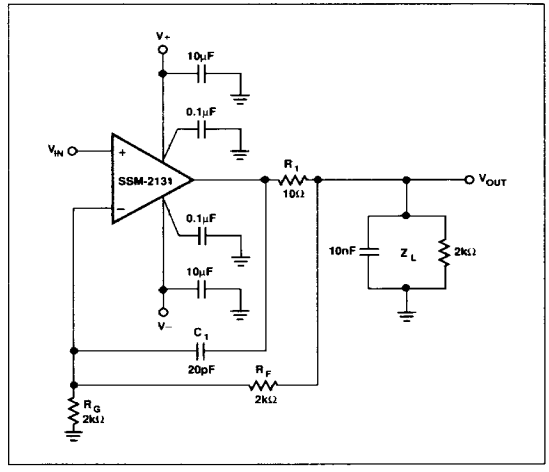

FIGURE 12: *Compensation for Large Capacitive Loads*

When driving very large capacitances, slew rate will be limited by the short-circuit current limit. Although the unloaded slew rate is insensitive to variations in temperature, the output current limit has a negative temperature coefficient, and is asymmetrical with regards to sourcing and sinking current. Therefore, slew rate into excessive capacities will decrease with increasing temperature, and will lose symmetry.

DAC OUTPUT AMPLIFIER

The SSM-2131 is an excellent choice for a DAC output amplifier, since its high speed and fast settling-time allow quick transitions between codes, even for full-scale changes in output level. The DAC output capacitance appears at the operational amplifier inputs, and must be compensated to ensure optimal settling speed. Compensation is achieved with capacitor C in Figure 13. C must be adjusted to account for the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance at the inputs. With a bipolar DAC, an additional shunt resistor may be used to optimize response. This technique is described in PMI's application AN-24.

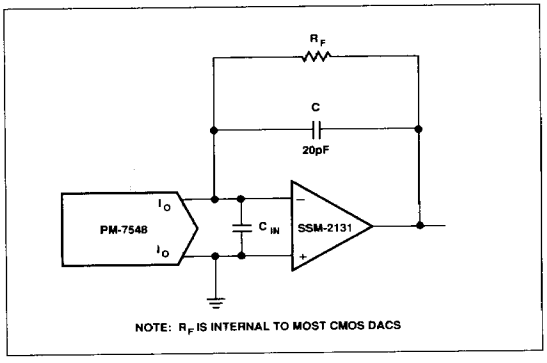

FIGURE 13: *DAC Output Amplifier Circuit*

Highest speed is achieved using bipolar DACs such as PMI's DAC-08, DAC-10 or DAC-312. The output capacitances of these converters are up to an order of magnitude lower than their CMOS counterparts, resulting in substantially faster settling-times. The high output impedance of bipolar DACs allows the output amplifier to operate in a true current-to-voltage mode, with a noise gain of unity, thereby retaining the amplifier's full bandwidth. Offset voltage has minimal effect on linearity with bipolar converters.

CMOS digital-to-analog converters have higher output capacitances and lower output resistances than bipolar DACs. This results in slower settling-times, higher sensitivity to offset voltages and a reduction in the output amplifier's bandwidth. These tradeoffs must be balanced against the CMOS DAC's advantages in terms of interfacing capability, power dissipation, accuracy levels and cost. Using the internal feedback resistor which is present on most CMOS converters, the gain applied to offset voltage varies between 4/3 and 2, depending upon output code. Contributions to linearity error will be as much as 2/3 V_{OS}. In a 10-volt 12-bit system, this may add up to an additional 1/5LSB DNL with the SSM-2131. Amplifier bandwidth is reduced by the same gain factor applied to offset voltage, however the SSM-2131's 10MHz gain-bandwidth product results in no reduction of the CMOS converter's multiplying bandwidth.

Individual DAC data sheets should be consulted for more complete descriptions of the converters and their circuit applications.

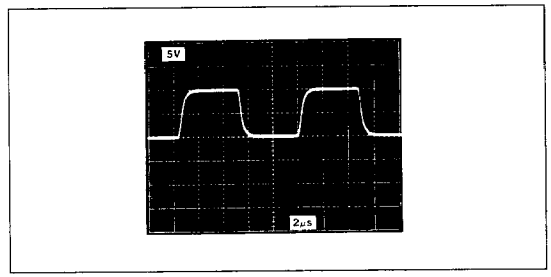

FIGURE 14: *DAC Output Amplifier Response (PM-7545 DAC)*

COMPUTER SIMULATIONS

The following pages show the SPICE macro-model for the SSM-2131 high-speed audio operational amplifier. This model was tested with, and is compatible with PSpice* and HSPICE**. The schematic and net-list are included here so that the model can easily be used. This model can accommodate multiple frequency poles and multiple zeroes, which is an advanced concept that results in more accurate AC and transient responses necessary for simulating the behavior of today's high-speed op amps. For example, 8 poles and 2 zeroes are required to sufficiently simulate the SSM-2131, which this advanced model can easily accommodate.

Throughout the SSM-2131 macro-model, RC networks produce the multiple poles and zeroes which simulate the SSM-2131's AC behavior. Each stage contains a pole or a pole-zero pair. The stages are separated from each other by voltage-controlled current sources so that the poles and zero locations do not interact. The only nonlinear elements in the entire model are two p-channel JFETs which comprise the input stage. Limiting the model to almost entirely linear circuit elements significantly reduces simulation time and simplifies model development.

*PSpice is a registered trademark of MicroSim Corporation.
**HSPICE is a tradmark of Meta-Software, Inc.

```
SSM-2131 MACRO-MODEL  © PMI 1989
*
* subckt SSM-2131  1  2 32  99  50
*
* INPUT STAGE & POLE AT 15.9 MHz
*
r1   1   3        5E11
r2   2   3        5E11
r3   5   50       707.36
r4   6   50       707.36
cin  1   2        5E-12
c2   5   6        7.08E-12
i1   99  4        1E-3
ios  1   2        4E-12
eos  7   1        poly(1) 20 26 1E-3 1
j1   5   2   4    jx
j2   6   7   4    jx
*
* SECOND STAGE & POLE AT 45 Hz
*
r5   9   99       176.84E6
r6   9   50       176.84E6
c3   9   99       20E-12
c4   9   50       20E-12
g1   99  9        poly(1) 5 6 3.96E-3 1.4137E-3
g2   9   50       poly(1) 6 5 3.96E-3 1.4137E-3
v2   99  8        2.5
v3   10  50       3.1
d1   9   8        dx
d2   10  9        dx
*
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
*
r7   11  99       1E6
r8   11  50       1E6
r9   11  12       4.5E6
r10  11  13       4.5E6
c5   12  99       16.1E-15
c6   13  50       16.1E-15
g3   99  11       9  26  1E-6
g4   11  50       26  9  1E-6
*
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
*
r11  14  99       1E6
r12  14  50       1E6
r13  14  15       4.5E6
r14  14  16       4.5E6
c7   15  99       16.1E-15
c8   16  50       16.1E-15
g5   99  14       11 26 1E-6
g6   14  50       26 11 1E-6
*
* POLE AT 53 MHz
*
r15  17  99       1E6
r16  17  50       1E6
c9   17  99       3E-15
c10  17  50       3E-15
g7   99  17       14 26 1E-6
g8   17  50       26 14 1E-6
*
* POLE  AT 53 MHz
*
r17  18  99       1E6
r18  18  50       1E6
c11  18  99       3E-15
c12  18  50       3E-15
g9   99  18       17 26 1E-6
g10  18  50       26 17 1E-6
*
* POLE AT 53 MHz
*
r19  19  99       1E6
r20  19  50       1E6
c13  19  99       3E-15
c14  19  50       3E-15
g11  99  19       18 26 1E-6
g12  19  50       26 18 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 100 kHZ
*
r21  20  21       1E6
r22  20  23       1E6
l1   21  99       1.5915
l2   23  50       1.5915
g13  99  20       3  26 1E-11
g14  20  50       26  3 1E-11
*
*POLE AT 79.6 MHz
*
r24  25  99       1E6
r25  25  50       1E6
c15  25  99       2E-15
c16  25  50       2E-15
g15  99  25       19 26 1E-6
g16  25  50       26 19 1E-6
*
*OUTPUT STAGE
*
r26  26  99       111.1E3
r27  26  50       111.1E3
r28  27  99       90
r29  27  50       90
l3   27  32       2.5E-7
g17  30  50       25 27 11.1111E-3
g18  31  50       27 25 11.1111E-3
g19  27  99       99 25 11.1111E-3
g20  50  27       25 50 11.1111E-3
v6   28  27       0.7
v7   27  29       0.7
d5   25  28       dx
d6   29  25       dx
d7   99  30       dx
d8   99  31       dx
d9   50  30       dy
d10  50  31       dy
*
* MODELS USED
*
.model jx PJF(BETA=999.3E-6 VTO=-2.000 IS=4E-11)
.model dx  D(IS=1E-15)
.model dy  D(IS=1E-15 BV=50)
.ends SSM-2131
```