SGS-THOMSON MICROELECTRONICS

ST5410

2B1Q U INTERFACE DEVICE

ADVANCE DATA

GENERAL FEATURES

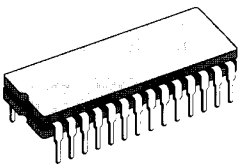
- SINGLE CHIP 2B1Q LINE CODE TRANSCEIVER
- SUITABLE FOR BOTH ISDN AND PAIR GAIN APPLICATIONS
- MEETS OR EXCEEDS ANSI T1.601-1988 U.S. STANDARD
- MEETS OR EXCEEDS ST/LAA/ELR/822 FRENCH SPECIFICATIONS
- SINGLE 5V SUPPLY
- 28 PINS PACKAGE
- 300mW ACTIVE AND 10mW INACTIVE POWER DISSIPATION
- HCMOS3A SGS-THOMSON ADVANCED DOUBLE-METAL SINGLE-POLY CMOS PROCESS

TRANSMISSION FEATURES

- 160 KBIT/S FULL DUPLEX TRANSCEIVER
- 2B1Q LINE CODING WITH SCRAMBLER/DESCRAMBLER
- 18KFT (5.5KM) ON 26AWG/24AWG TWISTED PAIR CABLES
- SUPPORTS BRIDGE TAPS, SPLICES AND MIXED GAUGES
- >70DB ADAPTIVE ECHO-CANCELLATION
- DIGITAL FEEDBACK EQUALIZATION
- ON CHIP TIMING RECOVERY WITHOUT EXTERNAL PRECISION COMPONENTS
- DIRECT CONNECTION TO SMALL LINE TRANSFORMER

SYSTEM FEATURES

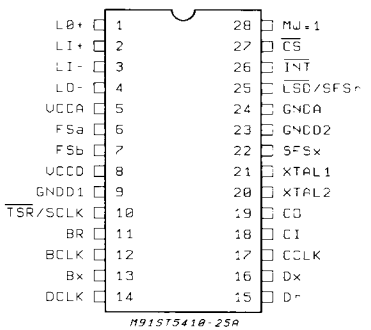
- ACTIVATION/DEACTIVATION CONTROLLER
- ON CHIP CRC CALCULATION AND VERIFICATION INCLUDING PROGRAMMABLE BLOCK ERROR COUNTER
- EOC CHANNEL AND OVERHEAD-BITS TRANSMISSION WITH AUTOMATIC MESSAGE CHECKING
- GCI AND MW/DSI MODULE INTERFACES COMPATIBLE
- DIGITAL LOOPBACKS
- ELASTIC DATA BUFFERS AND BACKPLANE CLOCK DE-JITTERIZER



Ceramic DIP28

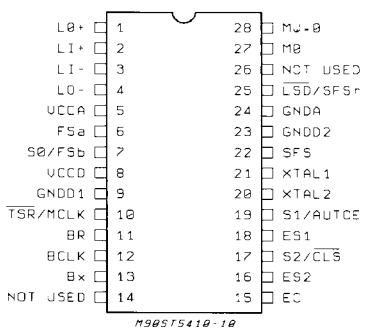
PIN CONNECTIONS (Top views)

MICROWIRE MODE



M91ST5410-25A

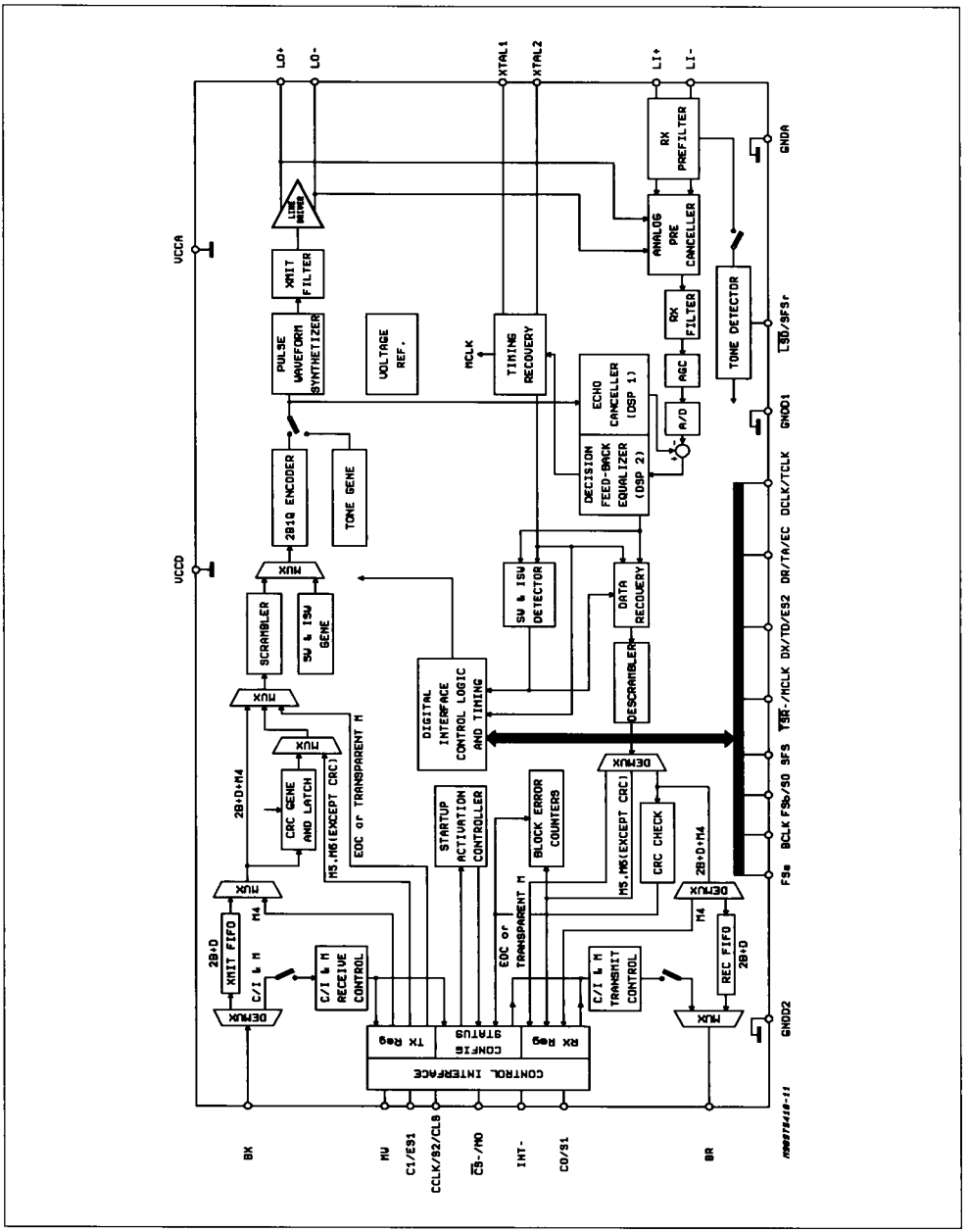
GCI MODE



M90ST5410-1B

INDEX

Figure 1: ST5410 Block Diagram.



GENERAL DESCRIPTION

ST5410 is a complete monolithic transceiver for ISDN Basic access data transmission on twisted pair subscriber loops typical of public switched telephone networks. The device is fully compatible with both ANSIT1.601-1988 U.S. and ST/LAA/ELR/822 French specifications.

The equivalent of 160 kbit/s full-duplex transmission on a single twisted pair is provided, according to the formats defined in the a.m. spec. Frames include two B channels, each of 64 kbit/s, one D channel of 16 kbit/s plus an additional 4 kbit/s M channel fcr loop maintenance and other user functions. 12 kbit/s bandwidth is reserved for framing. 2B1Q Line coding is used, where pairs of bits are coded into one of 4 quantum levels. This technique results in a low frequency spectrum (160 kbit/s turn into 80 kband), thereby reducing both line attenuation and crosstalk and achieving long range with low Bit Error Rates.

The system is designed to operate on any of the standard types of cable pairs including mixed gauges (26AWG, 24 AWG and 22 AWG) linking the loop by means of one simple transformer. Good noise margins are achieved even when bridged taps are present. On 26AWG cable, the transmission range is in excess of 5.5 km (18 kft) in presence of crosstalk and noise as specified by ANSI standard. ST 5410 is designed to operate with Bit Error Rate less than 10^{-6} on 45 dB loss loops with near-end Crosstalk (NEXT) of 52 dB as specified in european ETSI recommendation.

To meet these very demanding specifications, the device includes two Digital Signal Processors, one configured as an adaptive Echo-Canceller to cancel the near end echoes resulting from the transmit/recive hybrid interface, the other as an adaptive line equalizer. A Digital Phase-Locked Loop (DPLL) timing recovery circuit is also included that provides in NT1 a 15.36 MHz synchronized clock to the rest of the system. Scrambling and descrambling are performed as specified in the US and French specifications.

On the system side, ST5410 can be linked to two bus configuration simply by pin MW bias.

MICROWIRE(μW)/DSI mode (MW= 5V): 144 kbit/s 2B+D basic access data is transferred on a multiplex Digital System Interface with 4 different interface formats (see fig. 2 and 3) providing maximum flexibility with a limited pin count (BCLK, Bx, Br, FSa, FSb). Three pre-defined 2B+D formats plus an internal time slot assigner allows direct connection of the UID to the most common multiplexed digital interfaces (TDM/IDL). Bit and Frame Synchronisation signals are inputs or outputs depending on the configuration selected. Data buffers allow any phase shift between the line and the digital interface. That permits building of slave-slave configurations e.g. in NT12 trunk-cards.

It is possible to separate the D from the B channels and to transfer it on a separate digital interface (Dx, Dr) using the same bit and frame clocks as for the B channels or in a continuous mode using an internally generated 16 kHz bit clock output (DCLK).

All the Control, Status and Interrupt registers are handled via a control channel on a separate serial interface MICROWIRE compatible (CI, CO, $\overline{CS}$, CCLK, $\overline{INT}$) supported by a number of microcontroller including the ST6, ST9 and COPS families from SGS-THOMSON

GCI mode (MW= 0V). Control/maintenance channels are multiplexed with 2B+D basic access data in a GCI compatible interface format (see fig. 4a) requiring only 4 pins (BCLK, Bx, Br, FSa). On chip GCI channel assignement allows to multiplex on the same bus up to 8 GCI channels, each supporting data and controls of one device. Bit and Frame Synchronisation signals can be inputs or ouputs depending on the configuration selected. Data buffers, again, allow to have any phase between the line interface and the digital interface.

Through the M channel and its protocol allowing to check both direction exchanges, internals register can be configurated, the EOC channel and the Overhead-bits can be monitored. Associated to the M channel, there are A and E channels for enabling the exchanged messages and to insure the flow control. The C/I channel allows the primitive exchanges following the standard protocol.

In both mode (μW and GCI) CRC is calculated and checked in both directions internally.

In LT mode, the superframe can be synchronized by an external signal (SFS) or be self running. In NT mode the SFS is always output synchronized by the transmit superframe.

Line side or Digital Interface side loopbacks can be selected for each B1, B2 or D channel independently without restriction in transparent or in non-transparent mode.

Activation and deactivation procedures, which are automatically processed by UID, require only the exchange of simple commands as Activation Request, Deactivation Request, Activation Indication. Cold and Warm start up procedures are operated automatically without any special instruction.

PIN FUNCTIONS

Pin	Name	Description
1, 4	LO+, LO-	Transmit 2B1Q signal differential outputs to the line transformer. When used with an appropriate 1:1.5 step-up transformer and the proper line interface circuit the line signal conforms to the output specifications in ANSI standard with a nominal pulse amplitude of 2.5 Volts.
2, 3	LI+, LI-	Receive 2B1Q signal differential inputs from the line transformer.
5, 8	VCCD, VCCA	Positive power supply input for the analog and digital sections, which must be +5 Volts +/-5% and must be directly connected together.
6	FSa	When the Digital Interface clocks are selected as inputs, this signal must be a 8 kHz clock input which indicates the start of the frame on the Digital Interface data input pin Bx. In microwire mode two phases between the rising edge of FSa and the first slot of the frame can be selected by means of bit DDM in CR1: Delayed timing mode or non Delayed timing mode. When GCI Format is selected, FSa defines the frame begining for both Tx and Rx directions and non delayed timing mode is automatically selected. When the Digital Interface clocks are selected as outputs, FSa is a 8KHz output pulse conforming with the selected Interface format.
9, 23, 24	GNDD1, GNDD2, GNDA	Negative power supply pins, which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system Ground.
10	$\overline{TSR}$	(LT configuration only) This pin is an open drain output normally in the high impedance state which pulls low when B1 and B2 time-slots are active. It can be used to enable the Tristate control of a backplane line-driver.
	MCLK	(NT mode only) 15.36 MHz clock output which is frequency locked to the received line signal (unlike the XTAL pins, it is not freerunning) .
11	Br	Data output: 2B+D basic access data received from the line can be shifted out from the TRISTATE output Br at the BCLK frequency on the rising edges during the assigned time slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only BI & B2 data is shifted out from Br on the rising edges of BCLK. In Format 4 and GCI mode, data is shifted out at half the BCLK frequency on the transmit rising edges. When GCI mode is selected, 2B+D data is combined with the GCI Control channels and output Br becomes open drain. There is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

PIN FUNCTIONS (Continued)

in	Name	Description
12	BCLK	Bit Clock: This signal determines the data shift rate on the Digital Interface.When slave mode is selected,,BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz. When master mode is selected , BCLK is an output at 256 kHz, 512 kHz, 1536 kHz, 2048 kHz or 2560 kHz depending on the selection in Command Register 1. BLCK is synchronous with FSa/b Frame syncsignals and phase locked to the recovered clock received from the line. In formats 1-3, data is shifted in and out at the BCLK frequency. In format 4 and in GCI mode, data is shifted in and out at half the BCLK frequency.
1 3	Bx	Data input: 2B+D basic access data to transmit to the line can be shifted in at the BCLK frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in at the BCLK frequency on the falling edges during the assigned time slots. In format 4 and in GCI mode, data is shifted in at half the BCLK frequency on the receive falling edges. When GCI mode is selected, 2B+D data is combined with the GCI Control channels.
20	XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, if used. Otherwise, this pin must be left no connected.
21	XTAL1	The master clock input, which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a logic level clock input from a stable source. This clock does not need to be synchronized to the digital interface clocks (FSa, BCLK).Crystal specifications: 15.36 MHz +/-50ppm parallel resonant; Rs ≤ 20 ohms; load with 33pF to GND each side.
22	SFS	Super Frame synchronization I/O: When LT configuration is selected, the rising edge of SFS indicates the beginning of the Transmit Super Frame on the line. Two modes can be selected. In the first mode, SFS is an input that synchronizes the Transmit Frame counter of the UID core. SFS must be synchronous with FSa but with any phase . In the second mode, SFS is a square wave output issued from the free-running Transmit Frame counter. When NT configuration is selected, SFS is always a square wave output which indicates the beginning of the Transmit Superframe. There is no direct phase-relation between the data on the line and the data on the digital interface.
25	$\overline{\text{LSD}}$	Line Signal Detect output (default conf.): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The $\overline{\text{LSD}}$ output goes back in the high impedance state when the device is powered up.
	SFSr	Super Frame Synchronization output. When LT configuration is selected, it is possible to configurate pin 25 as SFSr that provides a square wave output indicating the beginning of the received Super Frame from the line. As for SFSx, there is no direct phase-relation between the data on the line and the data on the digital interface.
28	MW	MICROWIRE selection: When set high, MICROWIRE control interface is selected. All the internal registers can be accessed through it. When set low, GCI interface is selected. All the internal registers can be accessed through the GCI Monitor and Command/Indicate Control channels.

PIN FUNCTIONS (Specific to MICROWIRE MODE ONLY (MW = 1))

Pin	Name	Description
	FSb	This is a 8 kHz clock input which define the start of the frame on the Digital Interface data ouput pin Br. Two phases between the rising edge of FSb and the first slot of the frame can be selected with the same command as for FSa; Delayed timing mode or non Delayed timing mode. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse conforming with the selected format.
14	DCLK	(D channel port enabled, continuous mode selected) D channel Clock output: when the D channel port is enabled in continuous mode, data are shifted in and out at 16 kHz on the falling and rising edges of DCLK respectively. DCLK is synchronous with the BCLK frequency. When DCLK is disabled, it must be tied to GNDD.
15	Dr	(D channel port enabled) D channel data output: when the D channel port is enabled, D channel data is shifted out from the UID on this pin in two selectable modes: In multiplexed mode, data is shifted out at the BCLK frequency on the rising edges when the assigned time slot is active. In continuous mode, data is shifted out at the DCLK frequency on the rising edge continuously.
16	Dx	(D channel port enabled) D channel data input: When the channel port is enabled, D channel data is shifted in the UID on this pin in two selectable modes: In multiplexed mode, data is shifted in at the BCLK frequency on the falling edges when the selected receive time slots are active. In continuous mode, data is shifted in at the DCLK frequency on the falling edge continuously. When the D channel port is disabled, Dx must be tied to GNDD.
17	CCLK	Clock input for the MICROWIRE control channel: data is shifted in and out on the rising and falling edges of CCLK respectively. CCLK may be asynchronous with the digital interface clock.
18	CI	MICROWIRE control channel serial input: two bytes data is shifted into the UID on this pin on the rising edges of CCLK.
19	CO	MICROWIRE control channel serial output: two bytes data is shifted out from the UID on the falling edges of CCLK. When not enabled by $\overline{CS}$, CO is high-impedance.
26	$\overline{INT}$	Interrupt output: Latched open-drain output signal which is normally high impedance and goes low to request a read cycle. Pending interrupt data is shifted out from CO at the following read-write cycle. Several pending interrupts may be queued internally and may provide several interrupt requests. $\overline{INT}$ is freed upon receiving of $\overline{CS}$ low and can goes low again when $\overline{CS}$ is freed.
27	$\overline{CS}$	Chip Select input: When this pin is pulled low, data can be shifted in and out from the UID through CI & CO pins. When high, this pin inhibits the MICROWIRE interface. For normal read or write operation, $\overline{CS}$ has to be pulled low for 16 CCLK periods of time.

PIN FUNCTIONS (Specific to GCI MODE ONLY (MW = 0))

Pin	Name	Description
15	EC	External Control Output: controlled by the bit LEC in the TxM56 register.
18, 16	ES1,ES2	External Status inputs: during full synchronization the status of ES1, ES2 is loaded in the LES1, LES2 bits of the RxM56 register at each status change and an interrupt is issued. In NT mode, with AUTOE = 1, ES1/ES2 status are automatically sent on the line as ps1/ps2.
27	M0	GCI clocks I/O selection: when M0 is set low, BCLK and FSa clocks are inputs. BCLK can have any value between 512 kHz and 6176 kHz. GCI is selected in slave mode. When M0 is set high, BCLK and FSa clocks are outputs. FSa is a 8 kHz clock signal while BCLK is a 512 kHz or a 1536 kHz depending on CLS pin polarization. GCI channel 0 is automatically selected.In addition, when M0 is set high, NT configuration is also selected. When M0 is set low, NT or LT configuration must be selected through Configuration Register 2.
7,19,17	S0/FSb, S1/AUTOE, S2/CLS	(M0 = 0: slave mode) GCI number selection: these 3 pins S0, S1, S2 are significant when GCI is selected in slave mode only. A GCI channel constituted of 32 bits and relative to one basic access can be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection among 8 available GCI channels is made by programming the S0-S2 pins. (M0 = 1: master mode) S0 becomes FSb (output pulse indicating 2nd 64Kbit time slot.) S1 becomes AUTOE (input) S2 becomes $\overline{CLS}$ (input) GCI Clock Selection: while M0 is set high, $\overline{CLS}$ high selects the 1536 kHz frequency on BCLK and $\overline{CLS}$ low selects the 512 kHz frequency on BCLK.

FUNCTIONAL DESCRIPTION

Digital Interfaces

ST5410 provides a choice between two types of digital interface for both control data and (2 B + D) basic access data.

These are:
a) General Circuit Interface: GCI.
b) Microwire/Digital System Interface: µW/DSI

The device will automatically switch to one of them by sensing the MW input pin at the Power up.

µW/DSI MODE

Microwire control interface
The MICROWIRE interface is enabled when pin MW equal one. Internal registers can be written or read through that control interface.
It is constituted of 5 pins:

CI: data in
CO: data ouput
CCLK: data clock input
$\overline{CS}$: Chip Select input
$\overline{INT}$: Interruption output

Transmission of data onto CI & CO is enabled when $\overline{CS}$ input is low.

A Write cycle or a Read cycle is always constituted of two bytes. CCLK must be pulsed 16 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial Receive input register on the rising edge of each CCLK pulse. At the same time, data from the Transmit output register is shifted out onto the CO ouput on the falling edge of each CCLK pulse. The bit 7 (the first) is available as soon as $\overline{CS}$ goes low.

You can write in the UID on CI while the UID send back a register content to the microprocessor. If the UID has no message to send, it forces the CO output to all zero's.

If the UID is to be read (status change has occured in the UID or a read-back cycle has been requested by the controller), it pulls the $\overline{INT}$ output low until $\overline{CS}$ is provided. $\overline{INT}$ high to low transition is not allowed when $\overline{CS}$ is low (the UID waits for $\overline{CS}$ high if a pending interrupt occurs while $\overline{CS}$ is low) .

When $\overline{CS}$ is high, the CO pin is in the high impedance state.

Note: Special format is used for EOC channels.

Write cycle
The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: Write/Read Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the adressed register.
A0 set high indicates a read-back cycle request and the byte following is not significant. The UID will respond to the request with an interrupt cycle. It is than possible for the micro to receive the required register content after several other pending interrupts.

Read cycle
When UID has a register content to send to the microprocessor, it pulls low the $\overline{INT}$ output to request $\overline{CS}$ and CCLK signals. Note that the data to send can be the content of a Register previously requested by the microprocessor by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: forced to 1 if read back
forced to 0 if spontaneous
D7-D0: Register Content

Digital System Interface
Two B channels, each at 64 kbit/s and one D channel at 16 kbit/s form the Basic access data. Basic access data is transferred on the Digital System Interface with several different formats selectable by means of the configuration register CRI.
The DSI is basically constituted of 5 wires (see fig.2 and 3):

BCLK bit clock
Bx data input to transmit to the line
Br data output received from the line
FSa Transmit Frame sync
FSb Receive Frame sync

It is possible to separate the D channel from the B channels and to transfer it on a separate Digital Interface constituted of 2 pins:

Dx D channel data input
Dr D channel data ouput

The multiplexed mode uses the same bit and frame clocks as for the B channels. The continuous mode

uses an internally generated 16 kHz bit clock output:

DCLK D channel clock output.

ST5410 provides a choice of four multiplexed formats for the B and D channels data as shown in fig.2 and 3.

Format 1: the 2B+D data transfer is assigned to the first 18 bits of the frame on Br and Bx I/0 pins. Channels are assigned as follows: B1(8 bits), B2(8 bits), D(2 bits), with the remaining bits ignored until the next Frame sync pulse.

Format 2: the 2B+D data transfer is assigned to the first 19 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows: B1(8 bits), D(1 bit), 1 bit ignored, B2(8 bits), D(1 bit), with the remaining bits ignored until the next frame sync pulse.

Format 3: B1 and B2 Channels can be independently assigned to any 8 bits wide time slot among 64 (or less) on the Bx and Br pins. The transmit and receive directions are also independent. When multiplexed mode is selected, the D channel can be assigned to any 2 bits wide time slot among 256 on the Bx and Br pins or on the Dx and Dr pins (D port disabled or enabled in multiplexed mode continuous respectively).

Format 4: is a GCI like format excluding Monitor channel and C/I channel. The 2B+D data transfer is assigned to the first 26 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows. B1(8 bits) B2(8 bits), 8 bits ignored, D(2 bits), with remaining bits ignored up to the next frame sync pulse.

For all formats when D channel part is enabled "continuous mode" is possible. When the D channel port is enabled in multiplexed mode, only the 2 B channels use the Bx and Br pins. D bits are assigned according to the related format.

When the Digital Interface clocks are selected as inputs, FSa must be a 8 kHz clock input which indicates the start of the frame on the data input pin Bx. When the Digital Interface clocks are selected ae outputs, FSa is an 8 kHz output pulse conforming to the selected format which indicates the frame beginning for both Tx and Rx directions.

When the Digital Interface clocks are selected as inputs, FSb is a 8 kHz clock input which defines the start of the frame on the data ouput pin Br. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse indicating the second 64Kbit slot.

Two phase-relations between the rising edge of FSa/FSb and the first (or second for FSb as output) slot of the frame can be selected depending on format selected: Delayed timing mode or non Delayed timing mode.

Non delayed data mode is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa is coincident with the first 8 bits wide time-slot while FSb is coincident with the second 8 bits wide time-slot. Non delayed mode is not available in format 2.

Delayed timing mode, which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, Fsa (1bit wide pulse) indicates the first 8 bits time-slot beginning while FSb indicates the second. Delayed mode is not available in format 4.

2B+D basic access data to transmit to the line can be shifted in at the BCLX frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in during the assigned time slots. In format 4, data is shifted in at half the BCLK frequency on the receive falling edges.

2B+ D basic access data received from the line can be shifted out from the Br output at the BCLK frequency on the rising edges during the assigned time-slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only B1 & B2 data is shifted out from Br. In Format 4, data is shifted out at half the BCLK frequency on the transmit rising edges; there is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

Bit Clock BCLK determines the data shift rate on the Digital Interface. Depending on mode selected, BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz or an output at a frequency depending on the format and the frequency selected. Possible frequencies are:

256 KHz, 512 KHz, 1536 KHz,
2048 KHz, 2560 KHz.

In format 4 the use of 256kHz is forbidden.

BCLK is synchronous with FSa/b frame sync signal. When output, BCLK is phased locked to the recovered clock received from the line.

Figure 2: DSI interface formats: MASTER mode.

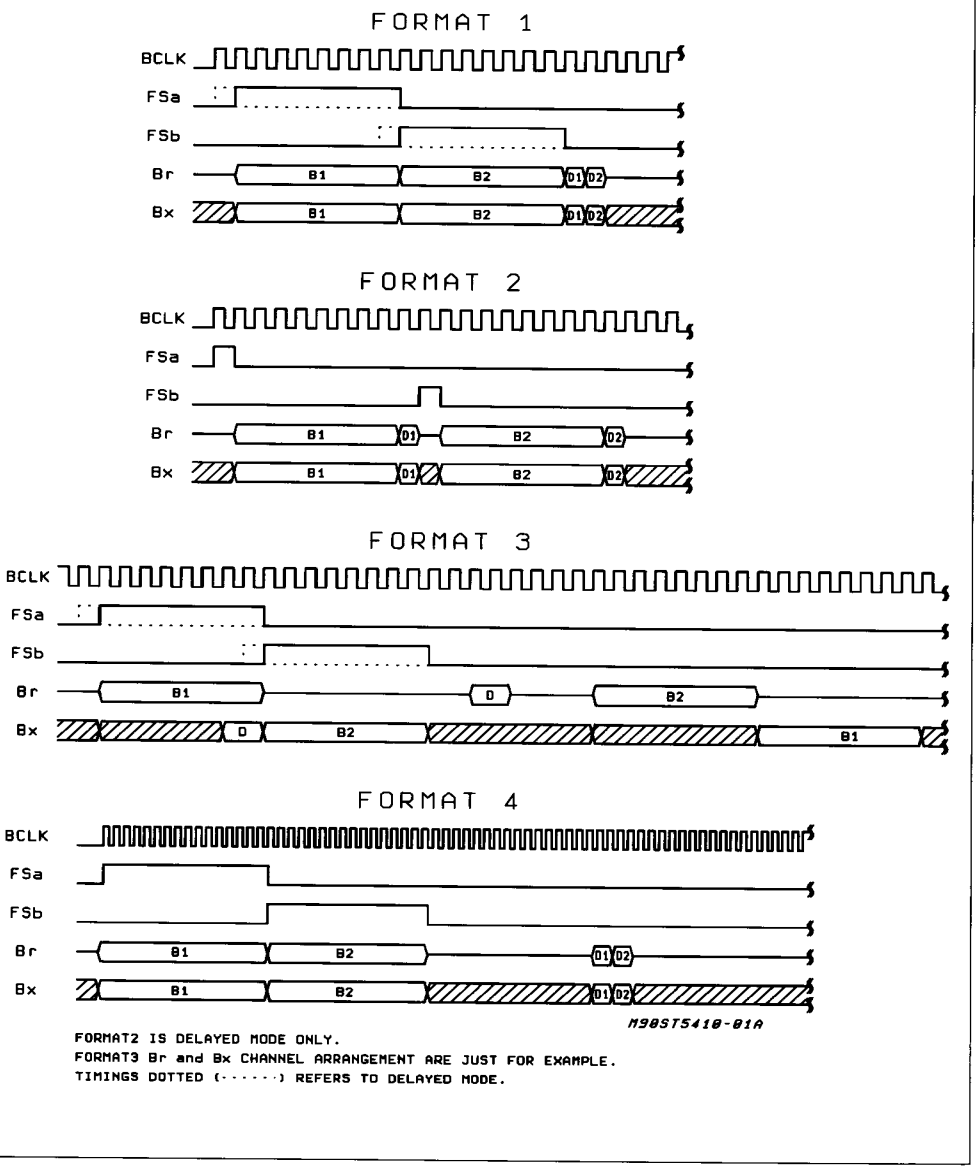
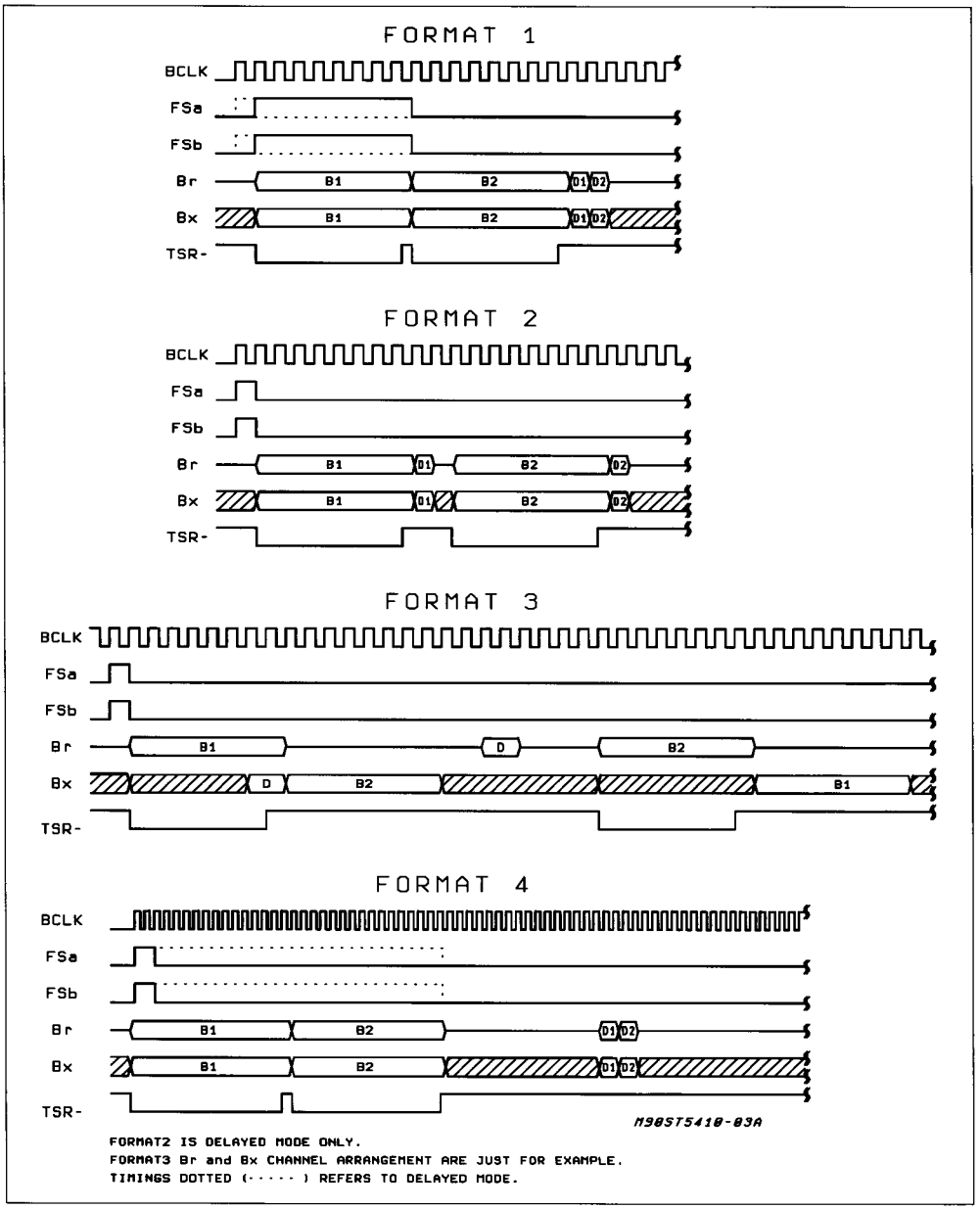


Figure 3: DSI interface formats: SLAVE mode.



GCI MODE

The GCI is a standard interface for the interconnection of dedicated ISDN components in the different equipments of the subscriber loop :
In a Terminal, GCI interlinks the S interface transceiver, the ISDN layer 2 (LAPD) controller and the voice/data processing components as an audio-processor or a Terminal Adaptor module.

In NT1-2, PABX subscriber line card, or central office line card (LT), GCI interlinks the UID, the ISDN Layer 2 (LAPD) controllers and eventually the backplane where the channels are multiplexed.

Frame Structure

2B+D data and control interface is transferred in a time-division multiplexed mode based on 8 kHz frame structure and assigned to four octets per frame and direction.(see fig.4a).
The 64 kbit/s channels B1 and B2 are conveyed in the first two octets; the third octet (M: Monitor) is used for transferring most of the control and status registers; the fourth octet (SC: Signalling & Control) contains the two D channel bits, the four C/I (command/Indicate) bits controlling the activation/deactivation procedures, and the E & A bits which support the handling of the Monitor channel.
These four octets per frame serving one ISDN

Figure 4a: GCI interface format.

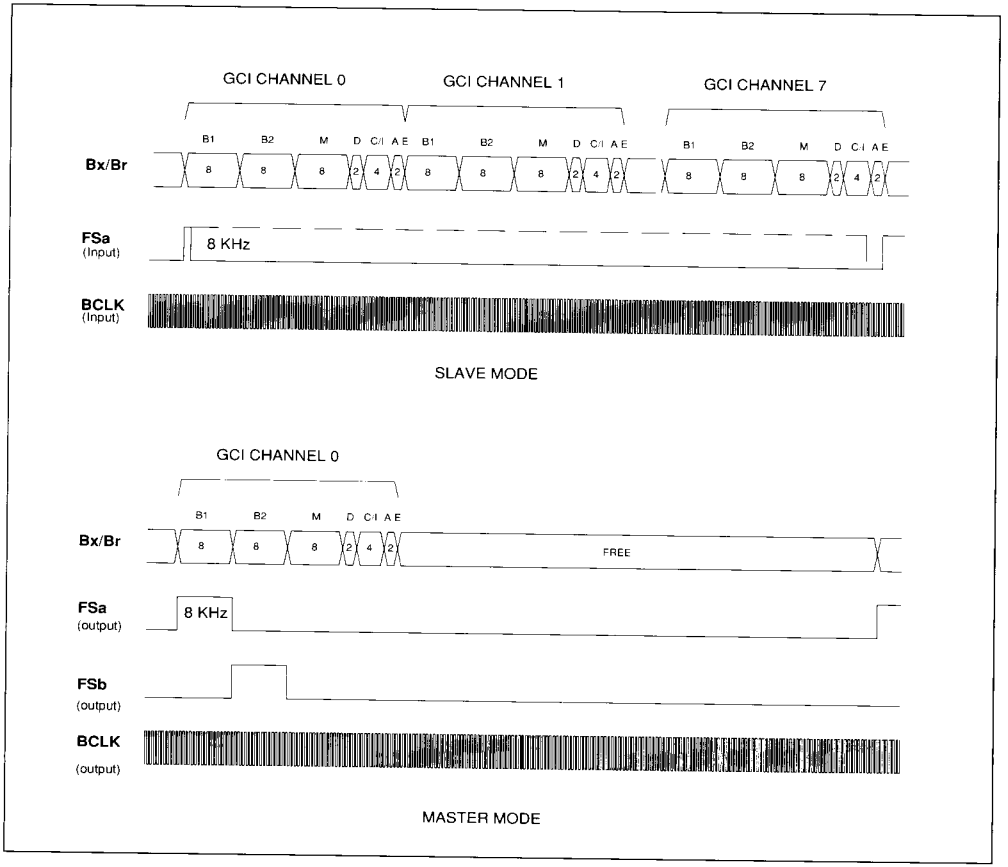
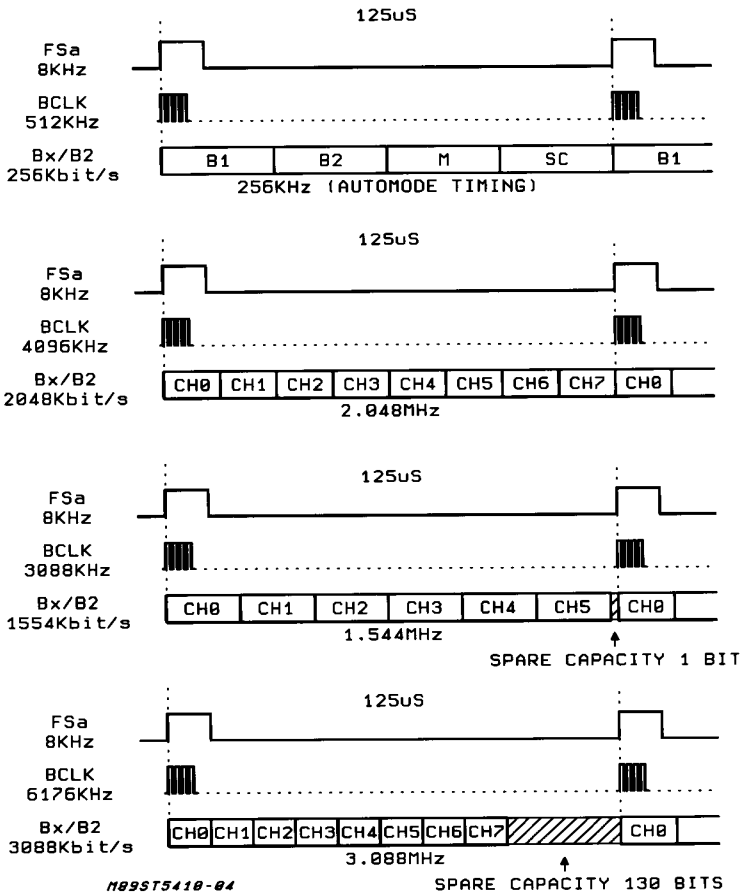


Figure 4b: GCI Multiplex Examples.



subscribers line form a GCI Channel. One GCI channel calls for a bit rate of 256 kbit/s.

In NT1-2s or subscriber Line Cards up to 8 GCI channels may be carried in a frame of a GCI multiplex. The bit rate of a GCI multiplex may be from 256 kbit/s and up to 3088 kbit/s. Adjacent 4-octet slots from the frame start are numbered 0 to 7. The GCI channel takes the number of the slot it occupies. Spare bits in the frame beyond 256 bits from the frame start will be ignored by GCI compatible devices but may be used for other purposes if required (see Fig.4b). GCI channel number is selected by biasing pins S0,S1,S2.

Physical Links.

Four physical links are used in the GCI.

Transmitted data to the line: Bx
Received data from the line: Br
Data clock: BCLK
Frame Synchronization clock: FSa

GCI is always synchronized by frame and data clocks derived by any master clock source. These two clock signals are provided to each component linked by GCI.

A device used in NT mode can deliver clock sources able to synchronize GCI, either directly, or via a local Clock Generator synchronized on the line by means of the MCLK 15.36 MHz output clock.Frame clock and data clock could be independent of the internal devices clocks. Logical one on the Br output is the high impedance state while logical zero is low voltage. For E and A bits, active state is voltage Low while inactive state is high impedance state.

Data is transmitted in both directions at half the data clock rate. The information is clocked by the transmitter on the front edge of the data clock and can be accepted by the receiver after 1 to 1.5 period of the data clock.

The data clock (BCLK) is a square wave signal at twice the data transmission frequency on Bx and Br with a 1 to 1 duty cycle. The frequency can be choosen from 512 to 4096 kHz with 16 kHz modularity. Data transmission rate depends only on the data clock rate.

The Frame Clock is a 8 kHz signal for synchronization of data transmission. The front edge of this signal gives the time reference of the first bit in the first GCI input and output channel, and reset the slot counter at the start of each frame

When some GCI channels are not selected on devices connected to the same GCI link, these time slots are free for alternative uses.

GCI configuration select is done by bias of input pins according to TABLE 1.

Table 1: GCI Configuration selection.

Pin name	TE/NT1	NT12/LT*
MW	0	0
M0	1	0
S2/CLS	CLS = 0: 512 KHz CLS = 1: 1536 KHz	S2
S0/FSb	FSb	S0
S1/AUTOE	AUTOE	S1

* Differentiation between NT and LT mode is done by configuration register 2 (NTS bit)

Monitor channel

The Monitor channel is used to write and read all ST5410 internal registers. Protocol on the Monitor channel allows a bidirectional transfer of bytes between UID and a control unit with acknowledgement at each received byte. Bytes are transmitted on the Br output and received on the Bx input in the Monitor channel slot.
A write or read cycle is always constituted of two bytes.(see fig. 5)

Note: Special format is used for EOC channel.

Write cycle

The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read Indicator set low
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the addressed register.

A0 set high indicates a read-back cycle request. the second byte content is not significative. ST5410 will respond to the request by sending back a message with the register content associated with its own address. It is than possible for the micro to receive the required register content after several other pending messages.

Read cycle

When UID has a register content to send to the controller, it send it on the monitor channel directly. Note that the data to send can be the content of a Register previously requested by the controller by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: forced to 1
D7-D0: Register Content

Exchange Protocol

ST5410 validates a received byte if it is detected two consecutive times identical. (see fig. 5)

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses A bit to acknowledge the received byte.When no message is transferred, E bit and A bit are forced to inactive state.

A transmission is started by the sender (Transmit section of the Monitor channel protocol handler) by putting the E bit from inactive to active state and by sending the first byte on Monitor channel in the same frame. Transmission of a message is allowed only if A bit sent from the receiver has been set inactive for at least two consecutive frames.

When the receiver is ready, it validates the incoming byte when received identical in two consecutive frames. Then, the receiver set A bit from the inactive to the active state (preacknowledgement) and maintain active at least in the following frame (acknowledgement).

If validation is not possible (two last bytes received are not identical) the receiver aborts the message by setting the A bit active for only a single frame.

The second byte can be transmitted by the sender putting the E bit from the active to the inactive state and sending the second byte on the Monitor channel in the same frame . The E bit is set inactive for only one frame.

If it remains inactive more than one frame, it is an end of message.

The second byte may be transmitted only after receiving of the pre-acknowledgement of the previous byte . Each byte has to be transmitted at least in two consecutive frames.

The receiver validates the current received byte as for the first one and then set the A bit in the next two frames first from the active state to the inactive state (pre-acknowledgement) and back to the active (acknowledgement). If the receiver cannot validates the received current byte (two bytes received not identical)it pre-acknowledges normally but let the A bit in the inactive state in the next frame which indicates an abort request .

If a message sent by the UID is aborted, the UID will send again the complete message until receiving of an acknowledgement .

A message received by the UID can be acknowledged or aborted with flow Control.

The most significant bit (MSB) of Monitor byte is sent first on the Monitor channel. E & A bits are active low and inactive state on DOUT is 5 V. When no byte is transmitted, Monitor channel slot on Br is in the high impedance state.

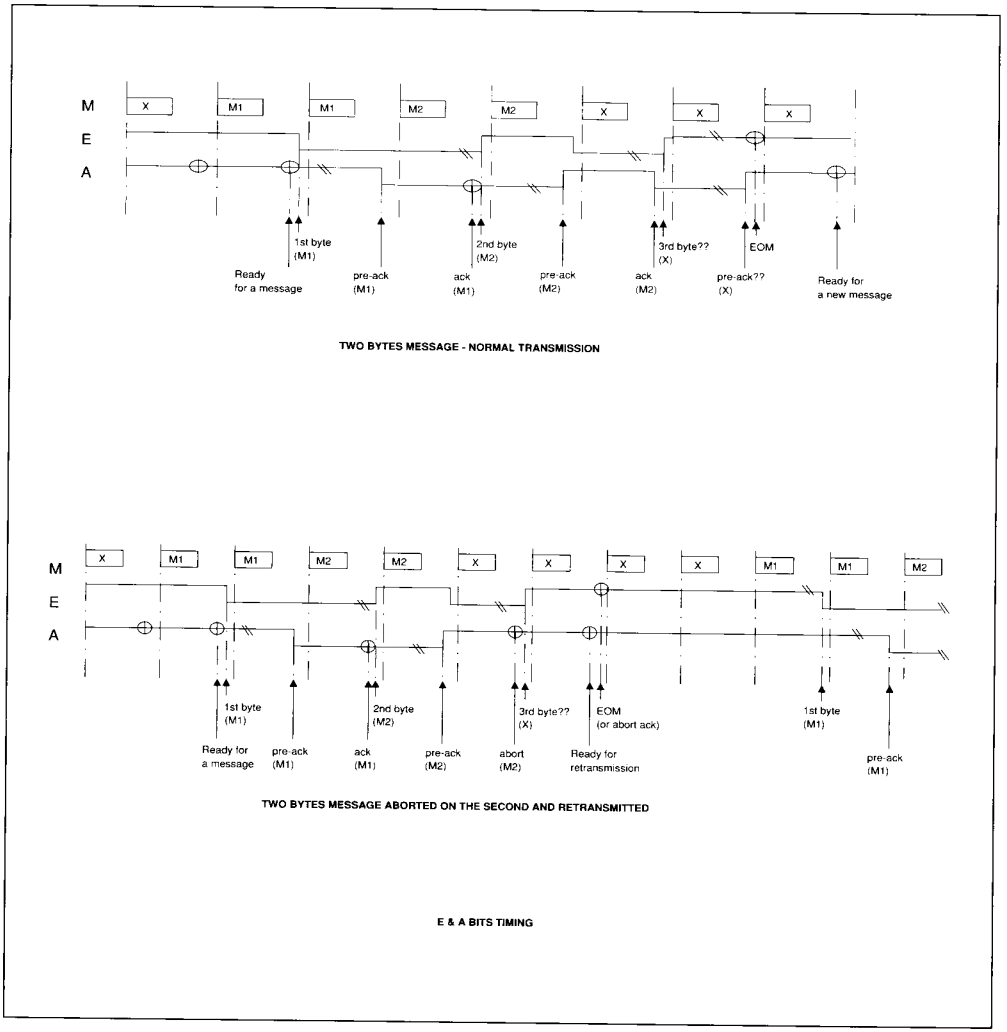
C/I channel

The C/I channel is used to load the Activation Control Register and to read the Activation Indication Register.

A four bits code (C1, C2, C3, C4) is transmitted on the Br output in the C/I channel of the GCI channel. The code is sent permanently at a 8 kHz frequency as long as the content the transmitted register remains unchanged. C1 bit is transmitted first.

A four bits code (C1, C2, C3, C4) is received on the Bx input in the C/I channel of the GCI channel . A change in the receive C/I channel code is validated if it has been received identical in two consecutive frames.

Figure 5: GCI Monitor channel messaging examples.



TURNING ON AND OFF THE DEVICE

ST5410 contains an automatic sequencer for the complete control of the start-up activation sequences specified by the ANSI and French specifications. Interactions with an external control unit requires only Activate Request and Deactivate Request commands, with the option of inserting breakpoints. Automatic control of act and dea bits in the M4 bit positions is provided, along with the specified 40 ms, 480 ms and 15 s timers used during the sequencing.

By default, during ACT procedure, the 15s timer is enabled, to force the device to abandon the sequence where the time limit is reached.

Except the Power up and Power down control that is slightly different, the Activation/Deactivation procedures are identical in GCI and Microwire modes. Same command codes or indication codes are used. In Microwire mode, Activation Control is done by writing in the Activation Control Register ACT. In GCI mode, these registers are accessed directly by the Command/Indicate channels.

Power on initialization

Following the initial application of power, ST5410 enters the power down deactivated state in MICROWIRE mode or in GCI mode depending on the polarization of the MW input.
All the internal circuits including the master oscillator are inactive and in a low power state except for the 10 kHz Tone signal detector. The line outputs LO+/LO- are low impedance and all digital outputs are high impedance. All programmable registers and the activation controller are reset to their default value.

In µW/DSI mode, configuration programming has to be completed before a power up instruction.

In GCI mode, GCI configuration is done by means of pins polarization and register programming.
In NT1 and TE equipments, GCI configuration is defined fully by means of the configuration pins M0, and CLS at Power On Reset.
For LT and NT1-2 equipments, GCI configuration is first defined by means of the configuration pins M0, S2, S1, S0 and must be completed by means of Control Register Programming prior the Power Up instruction.

Power up control

µW/DSI: control instruction PUP in ACT register is required to power up the UID.

GCI: when in TE/NT1 mode (M0=1), the UID provides the GCI clocks needed for control channel transfer; PUP control instruction is provided to the UID by pulling low the Bx data input; ST5410 then reacts sending GCI clocks. It is possible to operate an automatic power up of the UID when a wake up tone is detected from the line by connecting the $\overline{LSD}$ output directly to the Bx input.

GCI: when in LT/NT12 mode (M0=0), the UID powers up after that PUP code (0000) on C/I Control Channel has been sent.

When UID is in the power down state and a 10 kHz tone TN or TL is detected from the line, $\overline{LSD}$ and $\overline{INT}$(µW/DSI only) open drain outputs are forced to zero.

In NT configuration, code LSD (0000) is loaded in the activation indication register RXACT.

In LT configuration, code AP (1000) is loaded in the activation indication register.
In µW/DSI these indications are sent onto CO at the following access even if the UID is still in power down mode.
In GCI, these indications are sent onto the C/I channel as soon as GCI clocks are available.

$\overline{LSD}$ open drain output is set back in the high impedance state as soon as the UID is powered up.

$\overline{INT}$ open drain output is set back in the high impedance state when the $\overline{CS}$ input is detected at zero.

Power up transition enables all analog and digital circuitry, starts the Crystal oscillator and internal clocks. The LSD output is in the high impedance state even if a tone is detected from the line. As for the PDN instruction, PUP has no influence on the content of the internal registers.

Power down control

A control instruction PDN in ACT register is required to power down the device after a period of activity. PDN forces directly the device to the low power state. It should therefore only be used after the UID has been put in the line deactivated state. PDN has no influence on the content of the internal registers, but immediately stops the output clocks when UID is in master mode.

When line is fully deactivated DI code put UID in power down. UID waits for 2 frames (250µs) before entering power down state. During this time on GCI bus the code DI (1111) is sent an C/I. The clocks are stopped as soon as UID is in power down. The DI command is recommended in GCI mode.

Configuration Registers remain in their current state and can be changed either by the µW control interface or the CGI Monitor channel (if M0 = 0 only) depending on mode selected. It is then possible, for instance, after a normal deactivation procedure followed by a power down command, to power up again the device in order to operate directly a Warm Start procedure. In Power Down mode low impedance (with Typical value of 12Ω) between Li+ and Li- is ensured to maintain adaptation to the line impedance.

Software Reset
When the device is either powered-up or down, a control instruction RES resets the activation controller ready for a cold start. That feature can be used if the far-end equipment fails to warm start, for example if the line card or NT has been replaced or if in a regenerator, the loss of synchronisation of the second section imply the reset of the first section for a further cold start. The configuration registers remain in their selected value.

COMMAND/INDICATION (C/I) CODING

The Command/Indication codes are given in Table 2. For each mode a list of recognized Control codes and generated Indicate codes is given. Here after you have a detailed description depending on mode selected.

The C/I codes can be used:

a) in GCI mode, according to the already described rules.

b) in µW/DSI, using the register ACT described in chapter 'Internal register description'

NT mode: Control.

0000 (PUP) Power Up Request.
In GCI configuration with clocks selected as outputs, when UID is in Power down state, Power Up request is done by pulling low the Bx data input; UID reacts sending GCI clocks; code PUP enters no other change. In the other configurations, the PUP instruction powers up the device.

0001 (RES) RESET.
This code resets UID for a cold start. Configuration registers remain in their current value. Can be operated with the device either powered up or down.

0100 (EI) Error Indication.
EI code indicates that a transmission error has been detected on the TE side of the loop relative to UID. act bit is forced to 0 in the SN3 signal transmitted to the line.

0101 (PDN) Power Down Request.
PDN instruction forces the device to Power down state. It should normally only be used in µW/DSI mode after the ST5410 has been put in a known state, e.g. in an NT after a DI status indication has been reported.

1000 (AR) Activation Request.
Being in inactive Power Up state, AR instruction forces UID through the appropriate sequence to activate the line by sending TN and SN1.

1100 (AI) Activation Indication.
The AI code indicates that TE side of the loop relative to UID has been activated. act bit is sent equal 1 in the SN3 signal transmitted to the line.

1111 (DI) Deactivation Indication. (GCI only)
The DI instruction allows the UID to automatically enter the Power down state if the line is deactivated. When the line is not deactivated, DI has no effect.

NT mode : Indication.

0000 (DR/LSD) Deactivation Request.
When in the deactivated state either powered up or down, the LSD code is sent if a 10 kHz wake-up tone is detected. If the device is powered down, the $\overline{LSD}$ pin is also pulled low.
When in activated state, DR code indicates that network has decided to deactivate the line. dea bit has been received equal 0. UID enters the normal deactivate state waiting for a further Warm Start.

0100 (EI) Error Indication.
The EI code indicates that a transmission error has been detected on the loop for more than 480 ms (loss of synchro or loss of signal). UID enters the receive RESET state. EI also indicate that act bit has been received equal 0, or that 15sec timer has expired.

TABLE 2: C/I channel codes.

CODE	TE/NT1/NT12		LT	
C1C2C3C4	Ind	Com	Ind	Com
0000	DR/LSD	PUP	TIM*	PUP/DR
0001	—	RES	—	RES
0100	EI	EI	EI	FAO
0101	—	PDN	—	PDN
0110	—	—	SYNC	—
1000	AP	AR	AP	AR
1100	AI	AI	AI	AI
1111	DI	DI	DI	DI

(*) GCI code only for power up/power down control.

1000 (AP) Activation Pending.
Indicates that the network has decided to activate the loop. SL2/SL3 signal is received with the act bit set to 0.

1100 (AI) Activation Indication.
AI code indicates that network side of the loop relative to UID is activated. SL3 signal is received with the act bit equal 1.

1111 (DI) Deactivation Indication.The DI code indicates that the UID has entered the deactivated state H1.

LT mode: Control.

0000 (PUP/DR) Power Up Request/Deactivation Request.
When in the Power down state, the PUP code powers up the UID. When in the Power Up state, the DR code forces the UID through the appropriate deactivation sequence where the dea bit is set to 0 in four consecutive superframes before ceasing transmission.

0001 (RES) RESET.
This code resets the UID ready for a cold start. Configuration registers remain in their current value. Can be operated with the device either powered up or down.

0100 (FAO) Force act bit to 0.
The act bit is forced to 0 in the SL3 signal transmitted to the line. Is intended to reflect either a transmission error detected on the network side of the loop relative to UID or to acknowledge receiving of an act bit set to 0 from the line.

0101 (PDN) Power Down Request.
PDN instruction forces ST5410 to Power down state. It should normally only be used in µW/DSI mode after the ST5410 has been put in a known state, e.g. in an LT after a DI status indication has been reported.

1000 (AR) Activation Request.
Being in inactive Power Up state, AR instruction forces UID through the appropriate sequence to activate the line.

1100 (AI) Activation Indication.
The AI code is an optional command recognised only when the second break point BP2 is enabled giving the authorization to set the act bit equal one

1111 (DI) Deactivation Indication.
When line is fully deactivated the DI command allows UID to enter power down state. DI is recommended in GCI mode.

LT mode: Indication.

0000 (TIM) Timing required (GCI only)
The TIM code acnowledges PUP command in the case where the UID was previously in the Power Down state.

0100 (EI) Error Indication.
EI code indicates that a transmission error or a act bit equal zero has been received on the loop. In the first case, UID will enter automatically RESET state waiting for a further Cold Start and a DI primitive will be sent. EI also indicate that act bit has been received equal 0, UID being in the activate state.

0110 (SYNC) Synchronization Indication.
SYNC code is sent to indicate that ST5410 is superframe synchronized.

1000 (AP) Activation Pending.
AP code indicates that TE side is attempting to activate the loop. UID waits AR command to send SL1.

1100 (AI) Activation Indication.
The AI code indicates that the UID has received SN3 signal with act bit set to one. That means that the TE side of the loop relative to the UID is activated.

1111 (DI) Deactivation Indication.
The DI code indicates that the UID has entered the Deactivated state .

Activation/deactivation sequencing
Activation/deactivation signals onto the line are in accordance with the activation/deactivation state matrix given in Appendix A.
The startup procedures are in accordance with the T1.601-1988 and ST/LAA/ELR/822 procedures. All the timers defined in the standard are on chip. It is possible in any case to disable the 15sec timer replacing it with an external soft timing.
Refer to T1.601-1988 document for standard procedures description.

Table 3.

INTERNAL REGISTERS																	
COMMAND REGISTERS																	
FUNCTION		**BYTE 1**								**BYTE 2**							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
No Operation (NOP)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPR	W	0	0	1	0	0	0	0	0	CIE	EIE	FIE	OB1	OB0	OC1	OC0	0
	R	0	0	1	0	0	0	0	1	X	X	X	X	X	X	X	X
CR1	W	0	0	1	0	0	0	1	0	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
	R	0	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X
CR2	W	0	0	1	0	0	1	0	0	SFS	NTS	DMO	DEN	DD	0	BP2	0
	R	0	0	1	0	0	1	0	1	X	X	X	X	X	X	X	X
CR3	W	0	0	1	0	0	1	1	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
	R	0	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X
TXB1 TSA	W	0	0	1	1	0	0	0	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	0	0	1	X	X	X	X	X	X	X	X
TXB2 TSA	W	0	0	1	1	0	0	1	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X
RXB1 TSA	W	0	0	1	1	0	1	0	0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X
RXB2 TSA	W	0	0	1	1	0	1	1	0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	1	1	1	X	X	X	X	X	X	X	X
TXD	W	0	0	1	1	1	0	0	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
	R	0	0	1	1	1	0	0	1	X	X	X	X	X	X	X	X
RXD	W	0	0	1	1	1	0	1	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
	R	0	0	1	1	1	0	1	1	X	X	X	X	X	X	X	X
TXM4	W	0	1	0	0	0	0	0	0	ACT	M42	M43	M44	M45	M46	M47	M48
TXM56	W	0	1	0	0	0	0	1	0	0	0	LEC	M51	M61	M52	FEB	CTC
ACT Register	W	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
EC01	W	0	1	0	0	0	1	1	0	07	06	05	04	03	02	01	00
BEC1	R	0	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X
Tx EOC Register	W	0	1	0	1	E	F	G	H	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: bit 7 of byte 1 is always the first bit clocked into the device.
Note 2: In the Tx EOC Register:
E = ea1, the msb of the EOC destination address;
F = ea2, bit 2 of the EOC destination address;
G = ea3, the lsb of the EOC destination address;
H = dm, the EOC data/message mode indicator.

Note 3: X= don't care (it is recommended that these bits be set = 0).

Note 4: M42 in TXM4 only significant in LT mode.

Table 3: (continued)

STATUS REGISTERS											
FUNCTION	**BYTE 1**								**BYTE 2**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
READABLE CONFIGURATION REGISTERS																
Default (No Change on a Write cycle)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPR Contents	0	0	1	0	0	0	0	0	NBE	ECE	FBE	OB1	OB0	OC1	OC0	0
CR1 Contents	0	0	1	0	0	0	1	0	FF1	FF0	CK2	CK1	CK0	DDM	CLK	BEX
CR2 Contents	0	0	1	0	0	1	0	0	SFS	NTS	DMO	DEN	DD	BP1	BP2	0
CR3 Contents	0	0	1	0	0	1	1	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
TXB1 Contents	0	0	1	1	0	0	0	0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
TXB2 Contents	0	0	1	1	0	0	1	0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB1 Contents	0	0	1	1	0	1	0	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB2 Contents	0	0	1	1	0	1	1	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
TXD Contents	0	0	1	1	1	0	0	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
RXD Contents	0	0	1	1	1	0	1	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
REGISTERS WHICH GENERATE SPONTANEOUS INTERRUPTS (NOTE 2)																
RXM4	0	1	0	0	0	0	0	0	M41	M42	M43	M44	M45	M46	M47	M48
RXM56 Spare Bits	0	1	0	0	0	0	1	0	0	ES2	ES1	M51	M61	M52	feb	neb
ACT Indication Reg	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
BEC1 (Note 3)	0	1	0	0	0	1	1	0	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
Rx EOC Register (Note 4)	0	1	0	1	E	F	G	H	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: bit 7 of byte 1 is always the first bit clocked out from the device.

Note 2: All these Registers, with the exception of the EOC Register, set bit 0 of byte 1 as follows: bit 0=0 when the register is read in response to an Interrupt; bit 0=1 when reading back the register in response to a readback command.

Note 3: BEC1 may be polled, via the appropriate read command (see Table 1), at any time to read the current error count. When reading in response to a spontaneous interrupt, the data byte is always X'00.

Note 4: In the Rx EOC Register:
E = ea1, the msb of the EOC destination address;
F = ea2, bit 2 of the EOC destination address;
G = ea3, the lsb of the EOC destination address;

Note 5: ES1, ES2 (RXM56) not significant in µW mode.

INTERNAL REGISTERS DESCRIPTION.

Here following a detailed description of ST5410 internal registers.

Internal registers can be accessed:

a) In GCI mode, according to the monitor channel exchange rules.

b) in µW/DSI mode, using the MICROWIRE interface according to the rules described in section "µW control interface".

By default:
1) When not stated the registers are read-write.
2) Superframe formats (according to AN51 Std) are reported in table 2 and 3.

Overhead bits programmable register (OPR)

After reset: 00H

CIE	EIE	FIE	OB1	OB0	OC1	OC0	0

CIE Near-End CRC Interrupt Enable:

CIE = 1: the RXM56 register is queued in the interrupt register stack with nebe bit set to zero each time the CRC result is not identical to the corresponding CRC received from the line. If in two or more consecutive superframes, an error is detected, two or more interrupt cycles are issued.

CIE = 0: no interrupt is issued but the error detection remains active for instance for on chip error counting.

EIE Error counting Interrupt Enable:

EIE = 1: an interrupt is provided for the counter which goes in overflow (FF).

EIE= 0: no interrupt is issued. It is feasible to read the counters even if no relevant interrupt has been provided.

FIE FEBE Interrupt Enable:

FIE = 1: the RXM56 register is queued into the interrupt register stack each time the febe bit is received at zero in a superframe. If in two or more consecutive superframes, febe bit is received equal zero, two or more interrupt cycles are issued.

FIE = 0: no interrupt is issued but the receive febe bit remains active for on chip error counting

OB1, OB0 Overhead Bit processing:
select how each spare overhead bit received from the line is validated and transmitted to the system. RXM4 and RXM56 registers are independently provided onto the system interface as for the eoc channel. Spare overhead bits are validated independently.

OB1	OB0	
0	0	each super frame, a signal is generated for the RXM4 or the RXM56 register. Spare bits are transparently transmited to the system.
0	1	a signal is set at each new spare overhead Bits received.
1	0	a signal is set at each new spare overhead Bits received and confirmed once. (two times identical).
1	1	a signal is set at each new spare overhead Bits received and confirmed twice. (three times identical).

If new bits are received at the same time in M4 and M56, both registers RXM4 and RXM56 are queued in the interrupt register stack.
Bits act, dea are dedicated to the activation procedure. Validation is always done in accordance with the ANSI rule: validation at each new activation bit received and confirmed twice independently from the above rules. These bits are taken into account directly by the activation decoder. An interrupt is not generated for the RM4 Register when one of these bits changes.

OC1, OC0 eoc channel processing:
select how a received eoc message is validated and transmitted to the system.
The eoc message is signaled:
- in µW/DSI mode: on the control interface by an interrupt
- in GCI mode: on the Monitor channel.

OC1	OC0	
0	0	every half a super frame, a signal is generated for the RXEOC register. eoc channel is transparently transmitted to the system.
0	1	a signal is set at each new eoc message received.
1	0	a signal is set at each new eoc message received and confirmed once. (two times identical)
1	1	a signal is set at each new eoc message received and confirmed twice. (three times identical).

Configuration register 1 (CR1)

FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX

FF1, FF0 Frame Format Selection:
Refer to fig.1.

FF1	FF0	
0	0	Format 1
0	1	Format 2
1	0	Format 3
1	1	Format 4

CK0-CK2 Digital Interface Clock select:
CK0-CK2 bits select the BCLK output frequency when DSI clocks are outputs.

CK2	CK1	CK0	BCLK frequency:
0	0	0	256KHz
0	0	1	512KHz
0	1	0	1536KHz
0	1	1	2048KHz
1	X	X	2560KHz

DDM Delayed Data Mode select:
Two different phase-relations may be establish between the Frame Sync input and the first bit of the frame on the Digital Interface:

DDM = 0: Non delayed data mode (not available in Format 2) is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa starts with the first 8 bits wide time-slot while FSb with the second 8 bits wide time-slot.

DDM = 1: delayed data mode (not available in Format 4): which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, FSa pulse indicates the first 8 bits wide time-slot while FSb indicates the second.

CMS Clocks Master Select:

CMS = 0: BCLK, FSa and FSb are inputs; BCLK can have in Format 1, 2 and 3 value between 256KHz to 4048KHz, value in Format 4: 512KHz to 6176KHz.

CMS = 1: BCLK, FSa and FSb are outputs; FSa is a 8 kHz clock pulse indicating the frame beginning, FSb is a 8 kHz clock pulse is indicating the second time-slot. BCLK is a bit clock signal whose frequency bits CK2-CK0.

BEX B channels Exchange:

BEX = 0: B1 and B2 Tx/Rx channels are associatedwith B1 and B2 registers respectively.

BEX = 1: B1 and B2 channels are exchanged.

Configuration register 2 (CR2)

SFS	NTS	DMO	DEN	DD	0	BP2	-

SFS Super Frame Synchronization Select:
Significant in LT mode only.

SFS = 0: SFS is an input that synchronizes the transmit frame counter of ths GSC board (timing to be precised).

SFS = 1: SFS is an output issued from the free-running Transmit Frame counter of the GSC board. in NT mode SFS is always an output.

NTS LT / NT mode Select.

NTS = 0: LT mode selected

NTS = 1: NT (NT1, NT2, TE) mode selected

DMO D channel Transfer mode Select.
Significant only when DEN=1.

DMO = 1: D channel data is shifted in and out on Dx and Dr pins in continuous mode at 16 kbit/s on the falling and rising edges of DCLK respectively.

DMO = 0: D channel data is shifted in and out on Dx and Dr pins in a multiplexed mode at the BCLK frequency on the falling and rising edges of BCLK respectively when the assigned time-slots are active.

DEN D channel port Enable.

DEN = 0: D channel port disabled. D bits are transferred on Br and Bx; Multiplexed mode is selected automatically. Test port (TA, TD, TCLK) is selected and may be activated by a Test instruction.

DEN = 1: The D channel port (DX, DR, DCLK) is selected. D bits are transferred on Dr and Dxin a mode depending on DMO bit setting. Test port is disabled.

DD 2B+D Data channel Disable.

DD = 0: 2B+D channel transfer is enabled as soon as the line is completly synchronized.

DD = 1: 2B+D channel transfer is idle; 2B+D bits transmitted to the line are ones or zero depending on configuration respectively selected. 2B+D bits on the Digital Interface are in

the high impedance state. A second level of transparency control is provided for each channel independently from the others when format 3 is selected. See bits EB1, ED and EB2 in TXB1 and TXB2 configuration registers.

BP2 Break Points.
Significant only when NTS=0 (LT selected).

BP2 = 1: a break point in the activation sequencer is enabled after the UID has detected that NT was activatsd avoiding automatic response by act bit = 1.

BP2 = 0: the break point is disabled allowing automatic activation sequencing.

Configuration register 3 (CR3)
After reset: 00H

LB1	LB2	LBD	DB1	DB2	DBD	TLB	-

LB1, LB2, LBD Line side Loopback select.
When set high they turn each individual B1, B2, or D channel from the Line receive input to the Line transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if the D port is selected).

DB1, DB2, DBD Digital side Channel Loopback select.
When set high they turn each individual B1, B2, or D channel from the Digital Interface receive input to the Digital Interface transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if D port selected).

TLB Transparent Loopback select

TLB = 0: loopback are non transparent when line side loopback is set, data transmitted onto the digital interface is forced to one. When digital side loopback is set data transmitted onto the line is forced to one or zero depending on NT or LT configuration respectively.

TLB = 1: 2B+D is transparently transferred through the UID.

Configuration register TXB1
Significant only when format 3 selected.
After reset: 00H

-	-	TS5	TS4	TS3	TS2	TS1	TS0

TS5-TS0 Transmit B1 Time Slot Assignment
Those bits define the binary number of the transmit B1 channel time-slot on Bx input. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXB2
Register significant only when format 3 selected.
After reset: 01H

-	-	TS5	TS4	TS3	TS2	TS1	TS0

TS5-TS0 Transmit B2 Time Slot Assignment
Those bits define the binary number of the transmit B2 channel time-slot on Bx input. Time slots are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB1
Register significant only when format 3 selected.
After reset: 00H

EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0

EB1 B1 channel transparency

EB1= 1: B1 channel transparency enabled.

EB1= 0: B1 channel transmitted forced to one or zero depending on NT or LT configuration and forced the selected B1 channel time slot on Br output in the high impedance state.

ED D channel transparency enabling

ED = 1: enables the D channel transparency.

ED = 0: forces the D channel transmitted onto the line to one or zero depending on NT or LT configuration respectively and forces the selected D channel time slot on Br or Dr output in the high impedance state

TS5-TS0 Receive B1 Time Slot Assignment
TS5-TS0 bits define the binary number of the receive B1 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB2
Register significant only when format 3 selected.
After reset: 01H

EB2	-	TS5	TS4	TS3	TS2	TS1	TS0

EB2 B2 channel transparency
EB2 = 1: enables the B2 channel transparency.
EB2 = 0: forces the B2 channel transmitted onto the line to one or zero depending on NT or LT configuration respectively and forces the selected B2 channel time slot on Br output in the high impedance state.

TS5-TS0 Receive B2 Time Slot Assignment
Those bits define the binary number of the receive B2 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXD
Significant only when format 3 is selected with the D channel Digital interface selected in the multiplexed mode;
After reset: 0CH in GCI
08H in µW/DSI

DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0

DX5-SX0 Transmit D channel Time Slot Assignment
DX5-DX0 and SX1-SX0 bits define the binary number of the transmit D channel time-slot. DX5-DX0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot, SX1,SX0 bits define the binary numbar of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Configuration register RXD
Significant only when format 3 is selected with the D channel Digital interface selected in multiplexed mode.
After reset: 0CH in GCI
08H in µW/DSI

DR5	DR4	DR3	DR3	DR2	DR1	SR1	SR0

DR5-SR0 Receive D channel Time Slot Assignment
DR5-DR0 and SR1-SR0 bits define the binary number of the receive D channel time-slot. DR5-DR0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot., SR1,SR0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Transmit M4 channel register (TXM4)
(write only)
After reset: 7FH

-	m42	m43	m44	m45	m46	m47	m48

The TXM4 Register is constituted of 7 bits: m42, m43, m44, m45, m46, m47, m48. When the line is fully activated (super framing synchronized), the UID shall continuously send in the M4 channel field the register content to the line once per superframe. Register content is loaded in the transmit register at each superframe.
m41 is the act bit. m42 in LT mode in the LT to NT direction is the dea bit. These activation bits are controlled directly by the on chip activation encoder-decoder. The corresponding bits in the TXM4 register are not significant.

Transmit M5 and M6 channels register (TXM56)
(write only)
After reset: 3EH

-	-	LEC	m51	m61	m52	feb	CTC

LEC External Control pin
The logical level of the output EC is directly controlled by the bit LEC (GCI mode only).

m51, m61, m52 M5 and M6 spare over-head bits
Those spare overhead bits are normally equal to 1. Default value can be changed by setting the respective bits.

feb Transmit febe bit control
The febe bit which is normally at logical 1 and automatically set low in the following superframe when a CRC checking error has been detected in the previous received superframe may be forced to 0 by writing 0 in bit position feb. The febe bit set to zero is sent once to the line in the following available superframe.

CTC Corrupted Transmit CRC Control
CTC = 0: allows the normal calculation of the CRC for the transmitted data to the Line
CTC = 1: CRC result is transmitted inverted starting from next superframe. That ensure transmission of a corrupted CRC.

Activation control register (ACT)
(write only, µW only)
After reset XFH

-	-	-	-	C4	C3	C2	C1

This register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is directly adressed by means of the C/I channel. Activation Control instructions are coded on 4 bits.

Transmit EOC register (TXEOC)
(write only)
After reset: FFFH

ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

TXEOC Register is constituted of 12 bits. When the line is fully activated (super framing synchronized), ST5410 shall continuously send into the EOC channel field the eoc bits twice per superframe. TXEOC register is loaded in the transmit register at each half a superframe.
The address of this register is composed only of 4 bits. The W/R indicator is not needed.

Receive spare M4 overhead bits register (RXM4)
(read only)
After reset: 7FH

-	m42	m43	m44	m45	m46	m47	m48

RXM4 Register is constituted of 8 bits. When the line is fully activated (super frame synchronized), ST5410 extracts the M4 channel bits. m41 is the act bit; m42 in NT mode is the dea bit these bits are under the control of the activation sequencer. No interrupt cycle is provided for the RXM4 register when a change on one of the activation bits is detected.
When one of the remaining received spare bits is validated following the criteria selected in the Configuration Register OPR, the RXM4 register content is queued in the interrupt register stack. Activation bits status are also delivered.

Receive m5, m6 overhead bits register (RXM56)
(read only)
After reset: FFH

-	ES2	ES1	m51	m61	m52	feb	neb

When the line is fully activated (super frame synchronized), ST5410 extracts the overhead bits.
When one of the received spare bits m51, m61, m52 is validated following the criterias selected in the Configuration Register OPR, the RXM56 register content is queued in the interrupt register stack.If the FIE bit in OPR register is set high, the RXM56 register content is queued in the interrupt register stack each time the febe bit is received equal zero with bit feb equal 0.
The CRC received from the far-end is compared at the end of the superframe with the CRC calculated by the UID during that superframe. If an error is detected, the febe bit in the transmit direction is forced equal zero in the next superframe. If the CIE bit in the OPR register is set high, the RXM56 register is queued in the interrupt register stack at each CRC error detected with bit neb equal zero. ES1,ES2 bits indicates the status of the inputs pins ES1,ES2 respectively. At each status change, the RXM56 register is queued in the interrupt register stack.

Activation indication register (RXACT)
(read only)
Afterr reset: XHF

-	-	-	-	C4	C3	C2	C1

This Register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is directly connected to the C/I channel. At each activation status change, an interrupt request is queued in the interrupt register stack. In GCI mode, the C1-C4 bits are directly sent on the C/I channel. Activation Indication instructions are coded on 4 bits according to activation description.

Block Error counter 1 (EC1)
(read only)
After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Error up-counter 1. The register accounts for the febe and mebe errors. When counter goes in overflow (FF), an interrupt is provided for the EC1 register with value FF.

Offset Block error control counter 1 register (EC1) read only
(write only)
After reset: 00H

o7	o6	o5	o4	o3	o2	o1	o0

Block Error Counter 1 can be preset at a value given by Offset register EC1 Error. The counter is preset at that value each time the counter is read or when the preset value is loaded. o7-o0 is the binary value of the error up-counter 1 offset.

Receive EOC register (RXEOC)
(read only)

ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

The RX EOC Register is constituted of 12 bits. When the line is fully activated (super frame synchronized) and when a eoc message is received and validated in accordance with the criteria selected in the Configuration Register OPR, the RX EOC Register is queued in the interrupt register stack. The address of this register is composed only of 4 bits. The W/R indicator is not needed.
After each activation process, this register generates an interrupt giving the first received EOC channel content, even if it is a FFFH.

Table 4: Network-to-NT 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
A	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
B,C,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms).
All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat
act = activation bit (set = 1 during activation)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
dea = deactivation bit (set = 0 to announce deactivation)
uoa = (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

Table 5: NT-to-Network 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 602 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat

act = activation bit (set = 1 during activation)
ps_1, ps_2 = power status bits (set = 0 to indicate power problems)
ntm = NT in Test Mode bit (set = 0 to indicate test mode)
cso = cold-start-only bit (set = 1 to indicate cold-start-only)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
sai = S/T interface activation bit. Used in restricted activation only (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

LINE CODING AND FRAME FORMAT

2B1Q coding rule requires that binary data bits are grouped in pairs so called quats (see Tab.6). Each quat is transmitted as a symbol, the magnitude of which may be 1 out 4 equally spaced voltage levels (see Fig. 6). No redundancy is included and in the limit there is no bound to the Running Digital Sum (RDS), although scrambling controls the RDS in the pratical sense +3 quat referers to the nominal pulse wavwform specified in the ANSI standard. Other quats are deduced directly with respect of the ratio and keeping of the waveform.

The frame format used in UID follows ANSI and French specifications (see Tab. 4 and 5). Each complete frame cosists of 120 quats, with a line baud rate of 80 kbaud/s, giving a frame duration of 1.5ms. A9 quats sync-word defines the framing boundary. Furthermore, a Multiframe consisting of 8 frames is defined in order to provide sub-channels within the spare bits M1 to M6. Inversion of the syncword defines the multiframe boundary. Prior to transmisssion, all data, with the exception of the sync-word,is scrambled using a self-synchronizing scrambler to perform the specified 23rd-order polynomial. Descrambling is included in the receiver. Polynomial is different depending on the direction TE to NT or NT to TE.

Maintenance functions

M channel

In each frame there are 6 "overhead" bits assigned to various control and maintenance functions. Some programmable processing of these bits is provided on chip while interaction with an external controller provides the flexibility to take full advantage of the maintenance channels. See OPR, TXM4, TXM56, TXEOC, RXM4, RXM56, RXEOC register description fo details. New data written to any of the Overhead bit Transmit Registers is resynchronized internally to the next available complete superframe or half superframe, as appropriate.

Embedded Operatione Channel (EOC)

The EOC channel consists of two complete 12 bits messages per superframe, distributed through the M1, M2 and M3 bits of each frame. Each message is composed of 3 fields; a 3 bit address identifying the message destination/origin, a 1 bit indicator for the data mode i.e. encoded message or raw data, and an 8 bits information field. The Control Interface (Microwire or Monitor channel in GCI) provides access to the complete 12 bits of every message in TX and RX EOC registers.

UID does not recognize the received and encoded messages e. g. send corrupted CRC, then the apprpriate command register instruction must be written to the device to invoke the relevant function.

It is possible to select a transparent transmission mode in which the EOC channel can be considered as a transparent 2 kbit/s channel. See OPR register description for details.

M4 channel

M4 bit positions of every frame is a channel in which are trasmitted data bits loaded from the TXM4 transmit register and from the on-chip activation sequencer once the superframe. On the receive side, M4 bits from one complete superframe are first valitated and then stored in the RXM4 Receive Register or transmitted to on-chip activation sequencer. See OPR, TXM4 and RXM4 registers description for details.

Spare M5 and M6 bits

The spare bit positions in the M5 and M6 field form a channel in which are transmitted data bits loaded from the TXM56 transmit register. On the receive side, the spare bits in the M5 and M6 field are first validated and then stored in the RXM56 receive register. See OPR, TXM56 and RXM56 registers description for details.

CRC calculation/checking

In transmit direction, an on-chip CRC calculation circuit automatically generates a checksum of the 2B+D+M4 bits using the specified 12th order polynomial. Once per superframe, the CRC is transmitted in the M5 and M6 bit positions. In receive direction, a checksum is again calculated on the same bits as they are received and, at the end of the superframe compared with the received CRC. The result of this comparison generates a "Far End Block Error" bit (febe) which is transmitted back towards the other end of the Line in the next bute-one superframe and an indication of Near End Block Error is sent to the system by means of Register RXM56. If there is no error in superframe, febe is set = 1, and if there is one or more errors, febe is set = 0.

UID also includes an 8 bits Block Error Counter associated with the febe bits transmitted and received. Block error counting is always enabled but it is possible to disabled the overflow interrupt and/or to enabled/disabled the interrupt issued at each received or transmitted block error detection. See OPR register for details.

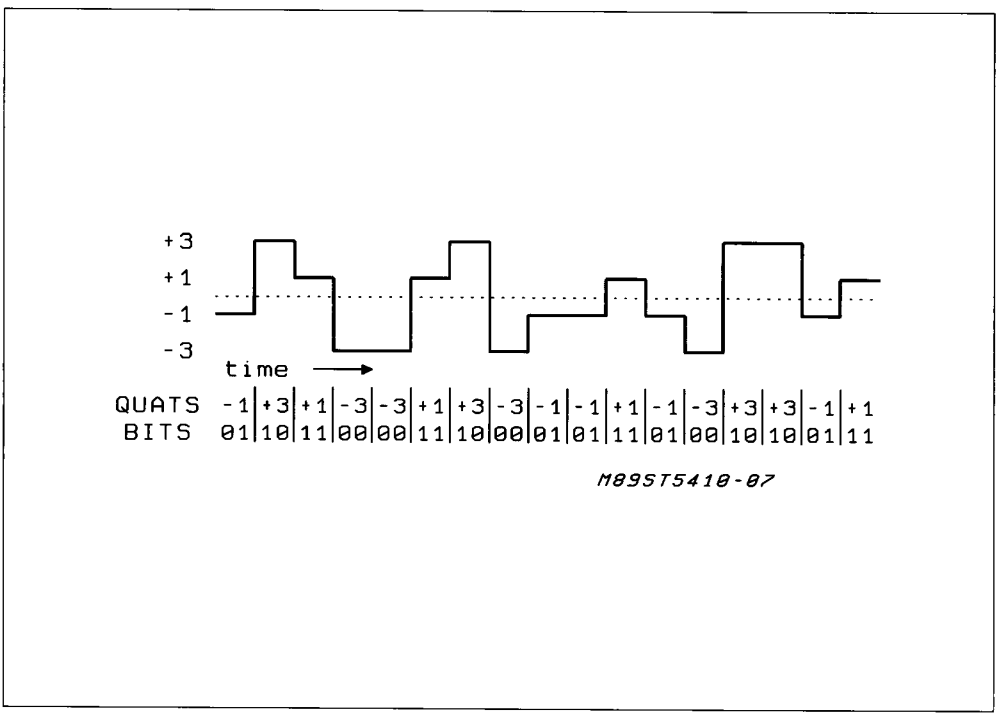
Table 6: 2B1Q Encoding of 2B+ D Fields.

Data	Time → B_1				B_g				D
Bit Pairt	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (relative)	q_1	q_2	q_3	q_4	q5	q_6	q_7	q_8	q_9
# Bits	8				8				2
# Quats	4				4				1

Where: b_{11} = first bit of B_1 octet as received at the S/T interface
b_{18} = last bit of B_1 octet as received at the S/T interface
b_{21} = first bit of B_2 octet as received at the S/T interface
b_{28} = last bit of B_2 octet as received at the S/T interface
d_1 d_2 = consecutive D-channel bits (d_1 is first bit of pair as received at the S/T interface)
q_i = ith quat relative to start of given 18-bit 2B+D data field.

NOTE: There are 12 2B+D 18-bit fields per 1.5 msec basic frame.

Figure 6: Example of 2B1Q Quaternary Symbols.



LINE SECTION

Data transmitted to the line consists of the 2B+D channel data received from the Digital Interface through an elastic data buffer allowing any phase deviation with the line, the activation/deactivation bits (M4) from the on-chip activation sequencer, the CRC code plus maintenance data (eoc channels) and other spare bits in the overhead channels (M4, M5, M6). Data are multiplexed and scrambled prior to addition of the sync-word, whiich generated within the device. A pulse waveform synthesizer then drives the transmit filter, which in turn passes the line signal to the line driver. The differential line-driver Outputs, LO+, LO- are designed to drive a transformer through an external termination circuit. A 1:1.5 transformer designed as shown in the Application section, results in a signal amplitude of normally 2.5V pk on the line for single quats of the +3 level. However, because of the RDS accumulation of the 2B1Q line code, continuous random data will produce signal swings considerably greater than this on the line. Short-circuit protection is included in the output stage; over-voltage protection must be provided externally.

In LT applications, the Network reference clock given by the FSa 8kHz clock input synchronizes the transmitted data to the line. The Digital Interface normally accepts BCLK and Fsa signals from the network, requiring the selection of Slave Mode in CRI. Retiming circuitry on chip allow the 15.36MHz crystal oscillator (or the logic level clock input on XTAL1) to be plesiochronous with respect to the network clock provided the sum of frequency inaccuracies, expressed in ppm deviation from nominal, of the network clock plus the XTAL1 one does not exceed 150ppm.

In NT applications, data is transmitted to the line with a phase deviation of half a frame relative to the received data as specified in the ANSI standard.

The receive input signal should be derived from the transformer by a coupling circuit aa shown in the Application section. At the front end of the receive section is a continuous filter which limits the noise bandwidth to approximately 200kHz. Then, a precanceller provides a degree of analog echo cancellation in order to limit the dynamic range of the composite signal which noise bandwidth limited by a 4th order butterworth switched capacitor low pass filter. After an automatic gain control, a 13bits A/D converter then samples the composite received signal before the echo cancellation from local transmitter by means of an adaptive digital transversal filter. The attenuation and distortion of the received signal from the far-end, caused by the line, is equalized by a second adaptive digital filter configured as a Decision Feedback Equlizer (DFE), that restores a flat channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

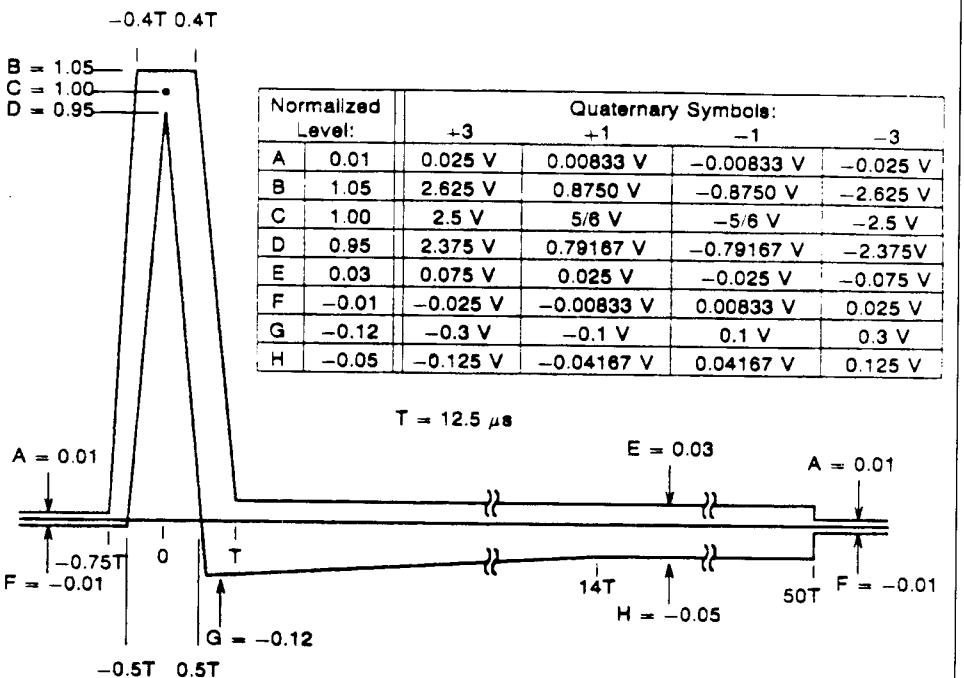
A timing recovery circuit based on a DPLL (Digital Phase-Locked Loop) recovers a very low-jitter clock for optimum sampling of the received symbols. The 15.36MHz crystal oscillator (or the logic level clock input) provides the reference clock for DPLL. In NT configuration, MCLK output provides a very low jitterized 15.36MHz clock to the system.

Received data is then detected and flywheel synchronization circuit searches for and locks onto the frame and superframe syncwords. ST5410 is frame-synchronized when two consecutive synchwords have been consecutively detected. Frame lock will be maintained until six consecutive errored sync-words are detected, which will cause the flywheel to attempt to re-synchronize. If a loss of frame sync condition persists for 480ms the device will cease searching, cease transmitting and go automatically into the RESET state, ready for a further cold start. When UID is frame-synchronized, it is superframe-locked upon the first superframe-locked upon the first superframe sync-word detection. No loss of superframe sync-word is provided.

While the receiver is synchronized, data is descrambled using the specified polynomial, and individual channels demultiplexed and passed to their respective processing circuits: user's 2B+D channel data is transmitted to the Digital Interface through an elastic data buffer allowing any phase deviation with the Line; the activation/deactivation bits (M4) are transmitted to the on-chip cativation sequencer; CRC is transmitted to CRC checking section while maintenance data (eoc) and other spare bits in the overhead channels (M4, M5, N6) are stored in their respective Rx registers.

In NT applications, if the Digital Interface is selected in master mode (see CR1) BCLK and FSa clock outputs are phase-locked to the recovered clock. If it is selected in Slave mode ie for NT1-2 application, the on-chip elastic buffers allow BCLX and FSa to be input from an external source, which must be frequency locked to the received line signal ie using the XTA1 output but with arbitrary phase.

Figure 7: Normalized Output Pulse From NT1 or LT..

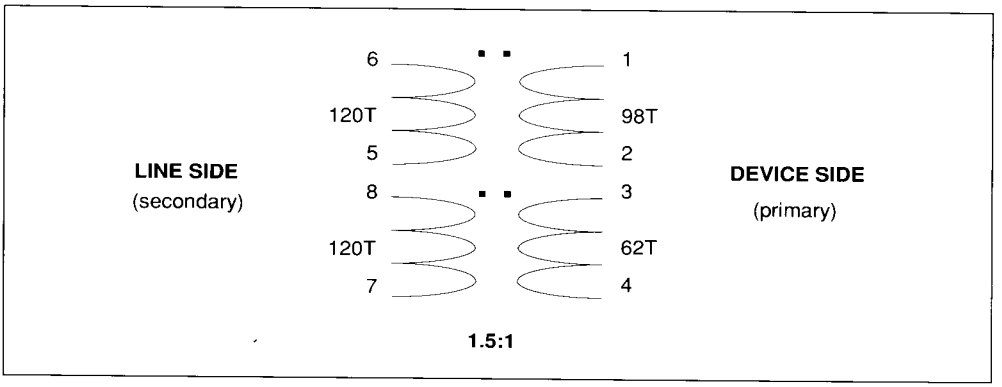


Normalized Level:		Quaternary Symbols: +3	+1	−1	−3
A	0.01	0.025 V	0.00833 V	−0.00833 V	−0.025 V
B	1.05	2.625 V	0.8750 V	−0.8750 V	−2.625 V
C	1.00	2.5 V	5/6 V	−5/6 V	−2.5 V
D	0.95	2.375 V	0.79167 V	−0.79167 V	−2.375V
E	0.03	0.075 V	0.025 V	−0.025 V	−0.075 V
F	−0.01	−0.025 V	−0.00833 V	0.00833 V	0.025 V
G	−0.12	−0.3 V	−0.1 V	0.1 V	0.3 V
H	−0.05	−0.125 V	−0.04167 V	0.04167 V	0.125 V

Line Interface Circuit

It is very important, for compliance with the ANSI and French standard, that the recommended line interface circuit should be strictly adhered to. The channel response and dynamic range of this circuit have been carefully designed as an integral part of the overall signal processing system to ensure the performance requirements are met under all the specified loop conditions. Deviations from this design are likely to result in sub-optimal performance or even total failure of the system on some types of loops.

Figure 8: Transformer Design.



Turns Ratio: Np:Ns = 1:1.5.
Secondary Inductance: Lp 27mH.
Winding Resistances: 30 ohms > (2.25Rp + Rs) > 10 ohms.
Return Loss at: 40 kHz against 135 ohms 26 dB.
Saturation characteristics: THD –70dB when tested with 50mA d.c. through the secondary and a 40kHz sine-wave injected into the primary at a level which generates 5V p-p into 135 ohms at the secondary.

List of suppliers:

SHOTT
PULSE ENGINEERING
AIE

Table 7.

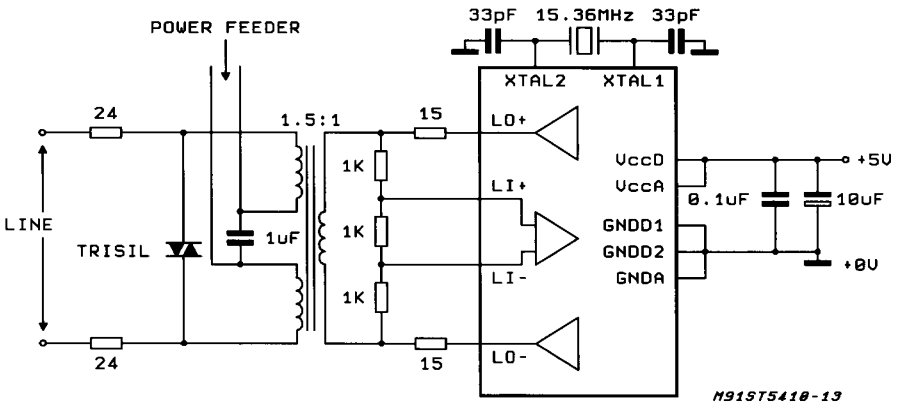
WINDING	NUMBER OF TURNS	WIRE GAUCE
1-2	98 Single	#34 AWG
6-5, 8-7	120+120 Bifilar	#36 AWG
3-4	62 Single	#34 AWG
WINDING	**INDUCTANCE**	**RESISTANCE**
1-2 + 3-4	12 mH	less than 5 ohms
5-6 + 7-8	27 mH	less than 10 ohms

Note: the split primary winding is designed to minimize leakage inductance.

Board Layout

While the pins of the UID are well protected against electrical misuse, it is recommended that the standard CMOS practise of applayng GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used. Great care must be taken in the layout of the printed circuit board in order to preserve the high transmission performance of the ST5410. To maximize performance, do not use the philosophy of separating analog and digital grounds for chip. The 3 GND pins should be connected together as close as possible to the pins, and the 2 VCC pins should be strapped together. All ground connections to each device should meet at a common point as close as possible to the 3 GND pins order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 1.5µF should be connected from this common point to VCC pins as close as possible to the chip. Taking care with the board layout in the following ways will also help prevent noise injection into the receiver frontend and maximize the transmission performances. Keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components. Keep the device, the components connected to LI+/LI- and the transformer as close as possible. Simmetrical layout for the line interface is suggested.

Figure 9: Recommended Connections.



0.1% MATCHING IS REQUIRED TO MEET THE LONGITUDINAL BALANCE SPECIFICATION
THE 150hm AND 1K RESISTORS IN THE INTERFACE CIRCUIT SHOULD BE 1%.

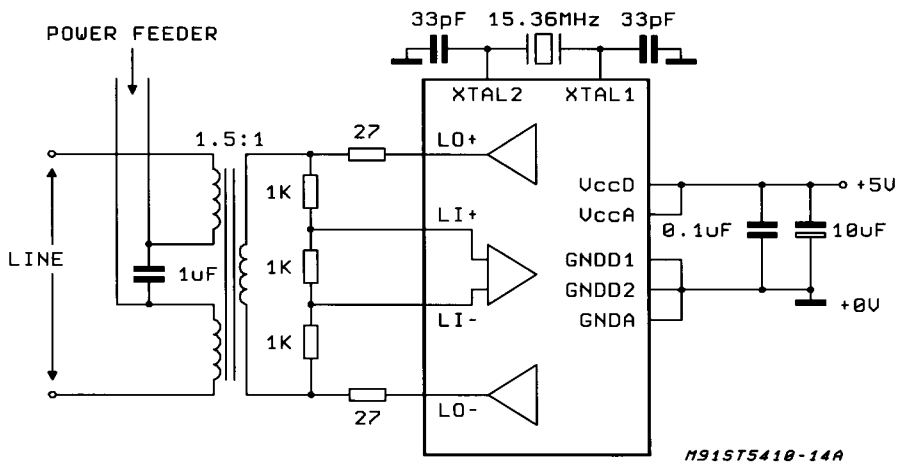
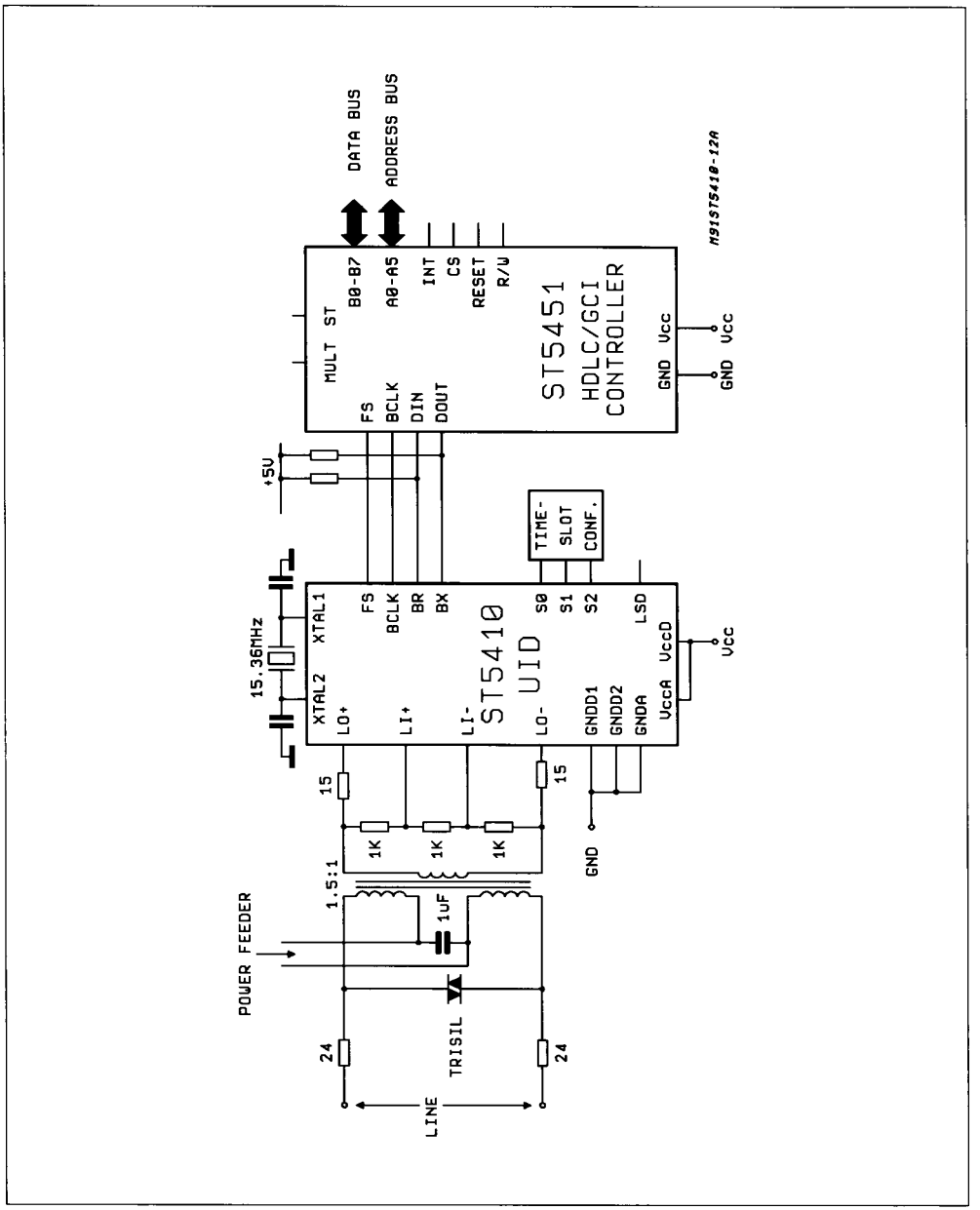


Figure 10: LT Application



APPENDIX A
State Matrix

EVENT	STATE NAME	Power Off	Full Reset	Alertg	Awake	EC Training	WAIT SN2	CHECK SN2	EC Covrg'd	SW Sync	ISW Sync	Active	Deact'n Alert'n	Tear Down	Pending Deact'n	Recv Reset
	STATE CODE	J0	J1	J2	J3	J4	J4.1	J4.2	J5	J6	J7	J8	J9	J10	J11	J12
	TX	SL0	SL0	TL	SL0	SL1	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL3 dea = 1 no change (*)	SL3 dea = 1 act = 1	SL3 dea = 0 act = 0	SL0	SL0	SL0
POWERON		J1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
ACTIVATION REQUEST (AR)		/	ST T5 J2	-	-	-	-	-	-	-	-	-	-	-	-	-
DEACTIVATION REQUEST (DR)		/	-	-	-	-	-	-	-	-	J9	J9	-	-	-	-
END OF TONE TL (3 ms)		/	/	J3	-	/	/	/	/	/	/	/	/	/	/	/
RECEIVED TONE TN and ACTIVATION REQUEST (AR)		/	ST T5 J3 AP	-	-	/	/	/	/	/	/	/	/	/	/	ST T5 STP T7 J3 AP
LOSS OF SIGNAL ENERGY		/	-	-	J4	-	-	J4.1	/	/	/	/	/	/	/	/
ECHO CANCELLER CONVERGED		/	-	-	-	J4.1	-	-	-	-	-	-	-	-	-	-
B-ASIC FRAME SYNC (SW)		/	/	/	/	/	/	/	J6	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	/	STP T5 J7 SYNC	-	-	-	-	-	-
RECEIVED act = 0		/	/	/	/	/	/	/	/	/	-	J7 EI	-	-	-	-
RECEIVED act = 1		/	/	/	/	/		/	/	/	J8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	/	J10 EI	J10 EI	-	-	-	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	/	/	/	/	ST T7 J12 EI	ST T7 J12 EI	ST T7 J12 EI	-	/	/	/
END OF THE LAST SUPERFRAME WITH dea = 0 (4th)		/	/	/	/	/	/	/	/	/	/	/	J11	/	/	/
EXPIRY OF TIMER (**) T5 (15 seconds)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	/	-	/	-	/	/
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	/	/	/	/	/	/	/	ST T7 J12	J1 D1	-
EXPIRY OF TIMER (**) T7 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1
DETECTION OF SIGNAL ENERGY		/	-	-	-	-	J4.2	J5	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	-	-	-	-	-	-

(*) FAO command is needed to send act = 0
(**) When timer is enabled (default)

ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN LT MODE

EVENT	STATE NAME	Power Off	Full Reset	Alertg	EC Training	WAIT SL	CHECK SL	EC Covrg'd	SW Sync	ISW Sync	Pending Active	Active	Pending Deact'n	Tear Down	TE Inactive	Recv Reset
	STATE CODE	H0	H1	H2	H3	H3.1	H3.2	H4	H5	H6	H7	H8	H9	H10	H11	H12
	TX	SN0 INFO0	SN0 INFO0	TN INFO0	SN1 INFO0	SN0 INFO0	SN0 INFO0	SN0 INFO0	SN2 INFO0	SL3 act = 0 INFO2	SN3 act = 1 INFO2	SN3 act = 1 INFO4	SN3 no change	SN0 INFO0	SN3 act = 0 INFO2	SN0 INFO0
POWERON		H1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
RECEIVED S/T INFO 1 SIGNAL (Received AR)		/	ST T4 H2	-	-	-	-	-	-	-	-	/	/	-	/	-
RECEIVED S/T INFO 3 SIGNAL (Received AI)		/	/	/	/	/	/	/	/	H7	-	-	-	-	H7	/
RECEIVED S/T INFO 0 SIGNAL (Received EI)		/	-	-	-	-	-	-	-	-	H11	H11	-	-	-	-
END OF TONE TN (9 ms)		/	/	H3	-	-	-	/	/	/	/	/	/	/	-	/
RECEIVED TONE TL and ACTIVATION REQUEST (AR)		/	ST T4 H2 LSD	-	/	/	/	/	/	/	/	/	/	/	-	ST T4 STP T6 H2 LSD
ECHO CANCELLER CONVERGED		/	-	-	H3.1	-	-	-	-	-	-	-	-	-	-	-
BASIC FRAME SYNC (SW)		/	/	/	/	/	/	H5	-	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	STP T4 H6 AP	-	-	-	-	-	-	-
RECEIVED dea = 0		/	/	/	/	/	/	/	/	H9 DP	H9 DP	H9 DP	-	-	H9 DP	-
RECEIVED act = 0 and dea = 1		/	/	/	/	/	/	/	/	/	-	H7 EI	-	-	-	-
RECEIVED act = 1 and dea = 1		/	/	/	/	/	/	/	/	/	H8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	H10 EI	H10 EI	H10 EI	-	-	H10 EI	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	ST T6 H12 EI	/	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	/	/	ST T6 H12 EI	-
EXPIRY OF TIMER (*) T4 (15 seconds)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	/	/	/	/	-	/	-
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	H3.1	/	/	/	/	/	ST T6 H12	ST T7 J12	/	/
EXPIRY OF TIMER T6 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H1 DI
DETECTION OF SIGNAL ENERGY		/	-	-	-	H3.2	H4	-	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	-	-	-	-	-	-	-

(*) When timer is enabled (default)

ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN NT MODE

APPENDIX B
Electrical Parameters

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7.0	V
V_{IN}	Input Voltage	– 0.3 to 7.0	V
T_A	Operting Temperature Range	0 to 70	°C
T_{stg}	Storage TemperatureRange	– 55 to 150	°C

TRANSMISSION ELECTRICAL PARAMETERS

Parameter	Min.	Typ.	Max.	Unit
LINE INTERFACE FEATURES				
Differential Input Resistance		140		KΩ
Line Driver Load			1000	pF
Differential Output Offset at LO+ / LO–	– 30	0	30	mV
Power up Output Differential Impedance (20KHz Bandwidth)		1		Ω
Power Down Output Diffrential Impedance	8	12	16	Ω
POWER CONSUMPTION				
I_{CCO}		2		mA
I_{CC1}		55		mA
TRANSMISSION PERFORMANCES				
Transmit Pulse Amplifier		3.2		V
Transmit Pulse Linearity	36	50		dB
Input Pulse Amplitude Differential Between LI+ and LI	±4		±800	mVpk

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Dig Inputs			0.7	V
V_{IH}	Input High Voltage	All Dig Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Inputs			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Inputs	V_{CC}–0.5		0.7	V
V_{OL}	Output Low Voltage	Br, I_O = +7mA All other Dig Outputs, IO = 1mA			0.4	V
V_{OH}	Output High Voltage	Br, I_O = –7mA All other Dig Outputs, I_O = –1mA All Outputs, I_O = –100µA	2.4 2.4 V_{CC}–0.5			V V V
I_L	Input Current	Any Dig Input, GND < V_{IN} < V_{CC}	–10		10	µA
I_{OZ}	Output Current in High Impedance State (TRISTATE)	Br, INT, LSD, CO, DR GND, V_{OUT} < V_{CC}	–10		10	µA

TIMING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MASTER CLOCK (timing diagram 15)						
FMCLK	Frequency of MCLK Tolerance	Including Temperature, Aging, Etc...	 –100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tWMH	Clock Pulse Width, MCLK High Level	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	20			ns
tWML	Clock Pulse Width, MCLK Low Level		20			ns
tRM tFM	Rise Time of MCLK Fall Time of MCLK	Used as a Logic Input			10 10	ns ns
DIGITAL INTERFACE (timing diagrams 1 to 12)						
FBCLK	Frequency of BCLK	Formats 1, 2 and 3 Format 4 and GCI Mode	256 512		4095 6144	KHz KHz
tWBH	Clock Pulse Width, BCLK High Level	Measured from V_{IH} to V_{IH}	30			ns
tWBL	Clock Pulse Width, BCLK Low Level	Measured from V_{IL} to V_{IL}	30			ns
tRB	Risae Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tSFB	Setup Time, FS High or Low to BCLK Low	DSI or GCI Slave Mode only	30			ns
tHBF	Hold Time, BCLK Low to FS High or Low	DSI or GCI Slave Mode only	20			ns
tDBF	Delay Time, BCLK High to FS High or Low	DSI or GCI Master Mode only	–20		20	ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150pF + 2 LSTTL Loads			80	ns
tDBDZ	Delay Time, BCLK High to Data HZ				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150pF + 2 LSTTL Loads See Timing Diagram 9			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHBD	Hold time, BCLK to Data Invalid		20			ns
tDBT	Delay Time, BCLK High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
tDBTZ	Delay Time, BCLK Low to TSR HZ				50	ns
tDFT	Delay Tie, FS High to TSR Low	Load = 100pF + 2 LSTTL Loads See Timing Diagram 12			80	ns
D PORT IN CONTINUOUS MODE: 16KBITS/SEC (timing diagram 13)						
tSDD	Setup Time, DCLK Low to DX High or Low		50			ns
tHDD	Hold Time, DCLK Low to DX High or Low		50			ns
tDDD	Delay Time, DCLK High to DR High or Low	Load = 50pF + 2 LSTTL Loads			80	ns
MICROWIRE CONTROL INTERFACE (timing diagram 14)						
FCCLK	Frequency of CCLK				5	MHz
tWCH	Clock Pulse Width, CCLK High Level	Measured from V_{IH} to V_{IH}	85			ns
tWCL	Clock Pulse Width, CCLK Low Level	Measured from V_{IL} to V_{IL}	85			ns
tRC	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			15	ns
tFC	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			15	ns
tSSC	Setup Time, CSB Low to CCLK High		60			ns
tHCS	Hold Time, CCLK Low to CSB High		10			ns
tWSH	Duration of CSB High		200			ns
tSIC	Setup Time, CI Valid to CCLK High		25			ns
tHCI	Hold Time, CCLK High to CI Invalid		25			ns
tDSO	Delay Time, CSB Low to CO Valid	Out First Bit on CO			50	ns
tDCO	Delay Time CCLK Low to CO Valid	Load = 50 pF + 2LSTTL Loads			50	ns
tDCOZ	Delay Time, CCLK Low to CO HZ				50	ns
tDCI	Delay Time, CCLK Low to INTB Low or HZ	Load = 80pF + 2LSTTL Loads			50	ns

Figure 11: BCLK, FSA, FSB, SLAVE MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY)

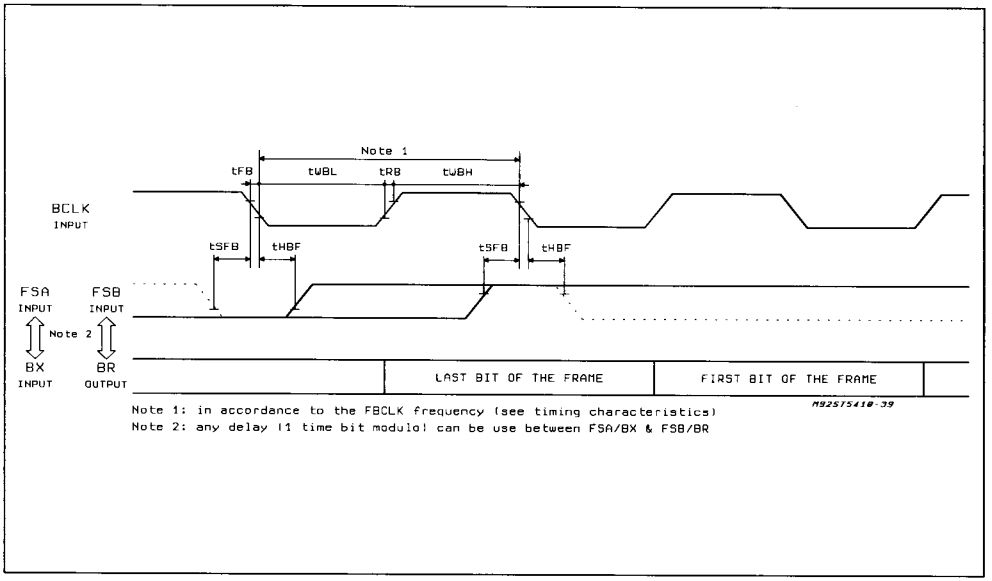


Figure 12: BCLK, FSA, FSB, SLAVE MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY)

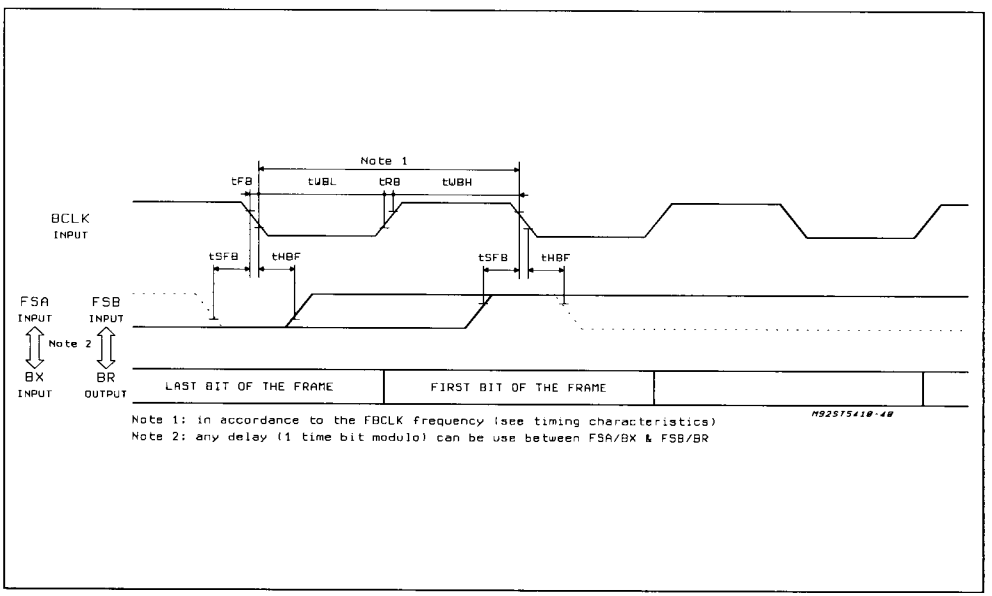


Figure 13: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW and GCI MODE)

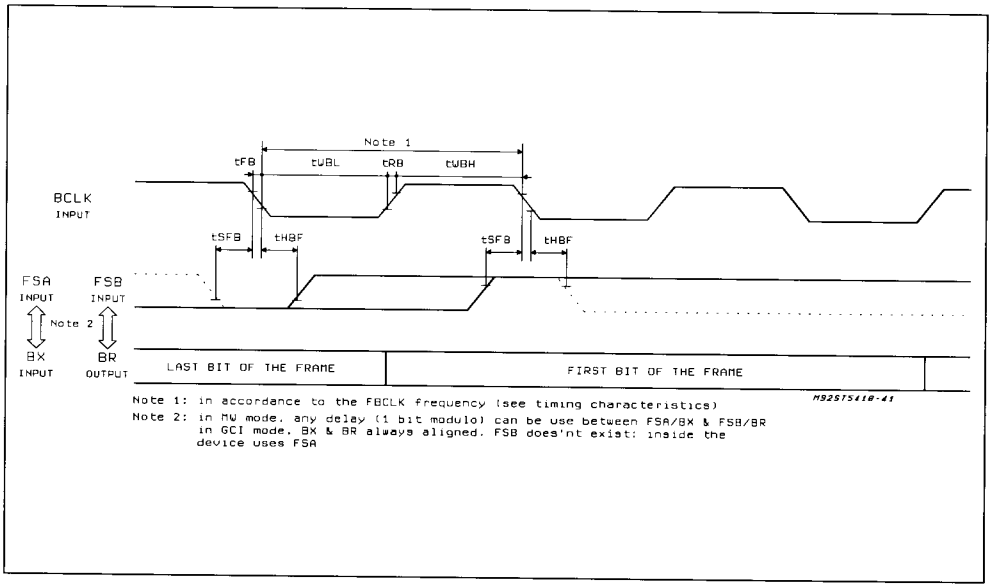


Figure 14: BCLK, FSA, FSB, MASTER MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY)

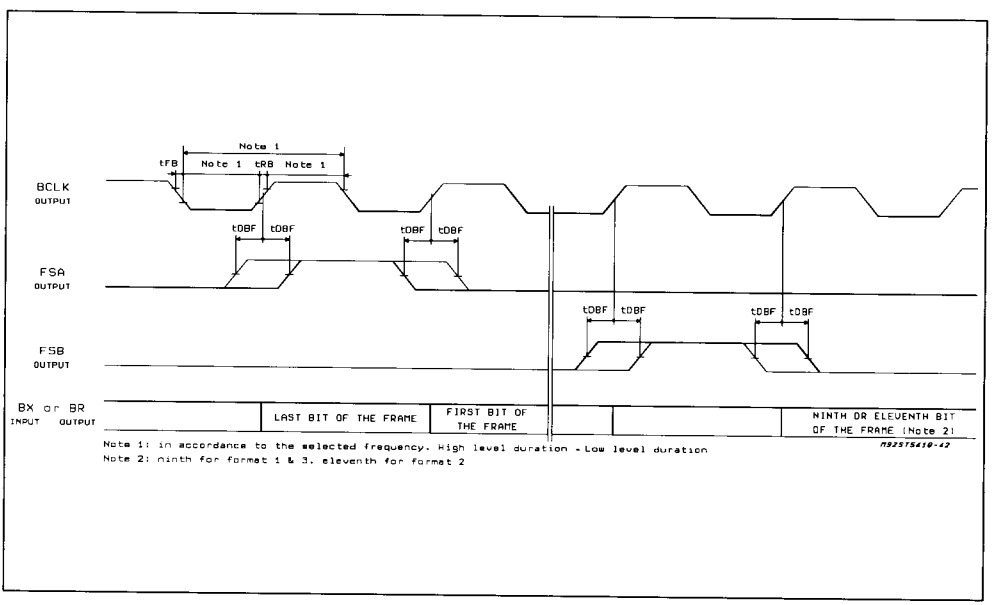


Figure 15: BCLK, FSA, FSB, MASTER MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY)

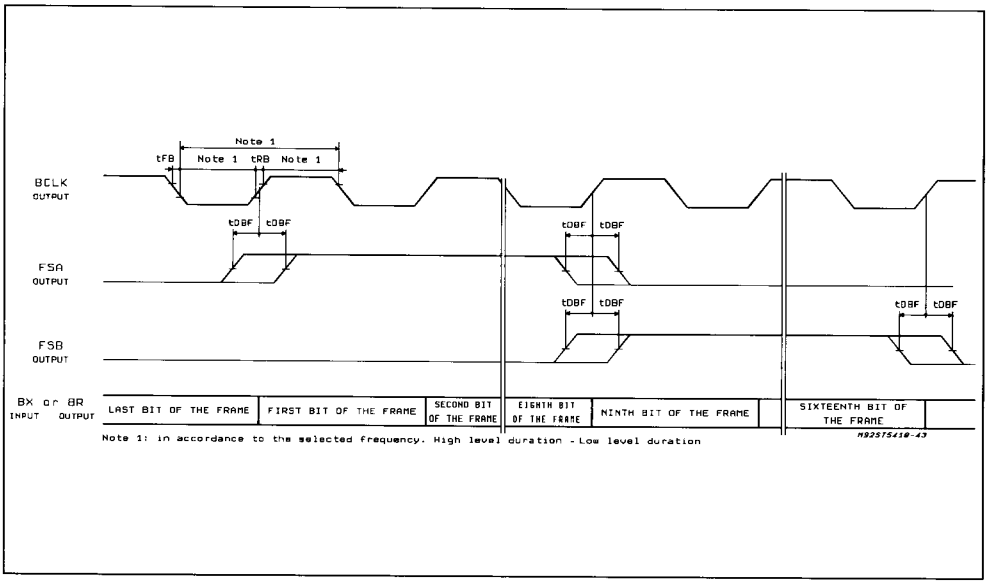


Figure 16: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW and GCI MODE)

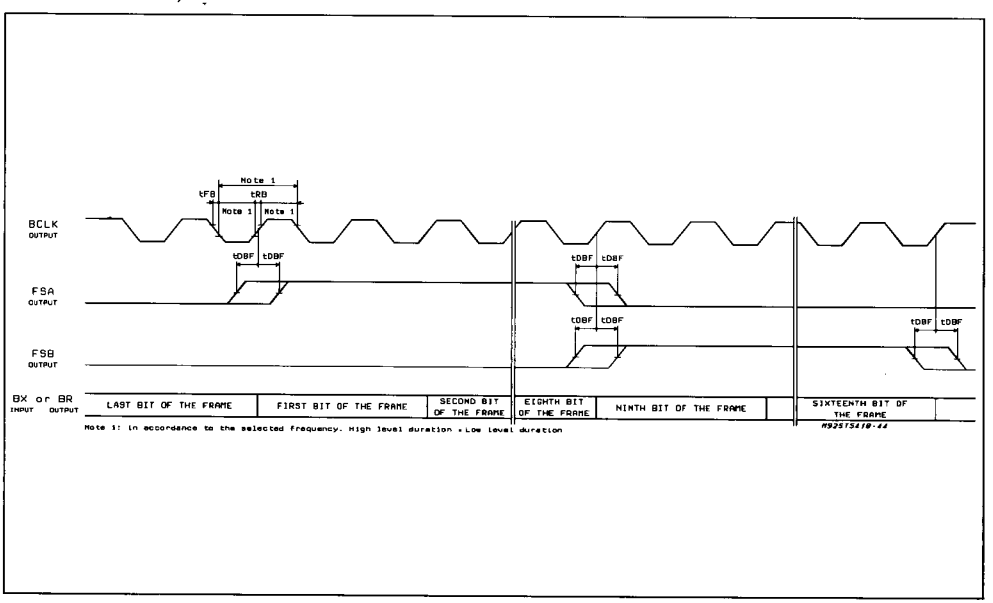


Figure 17: BX, DX, BR, DR, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

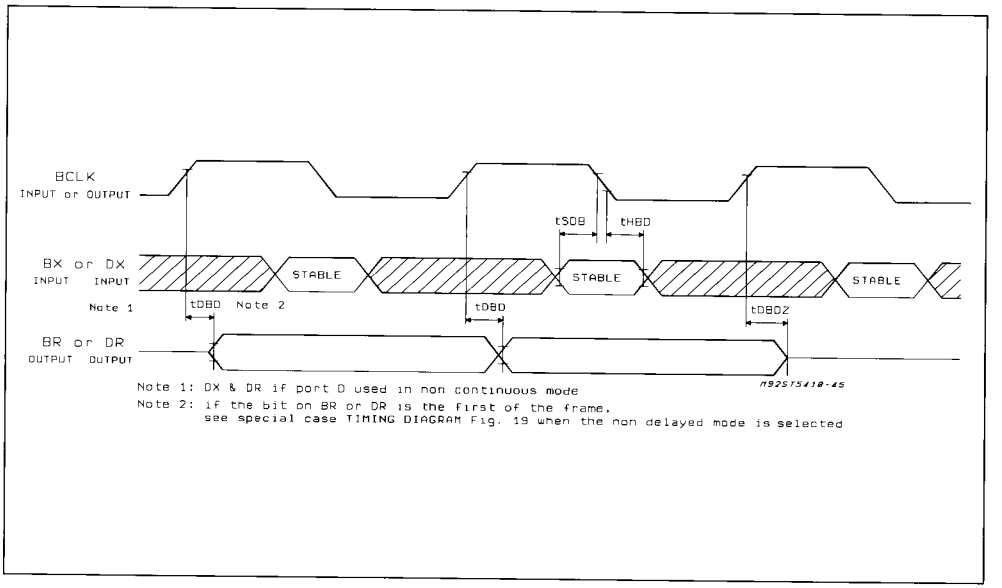


Figure 18: BX, DX, BR, DR, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED, FORMATS 1 2 3 (MW & GCI MODE)

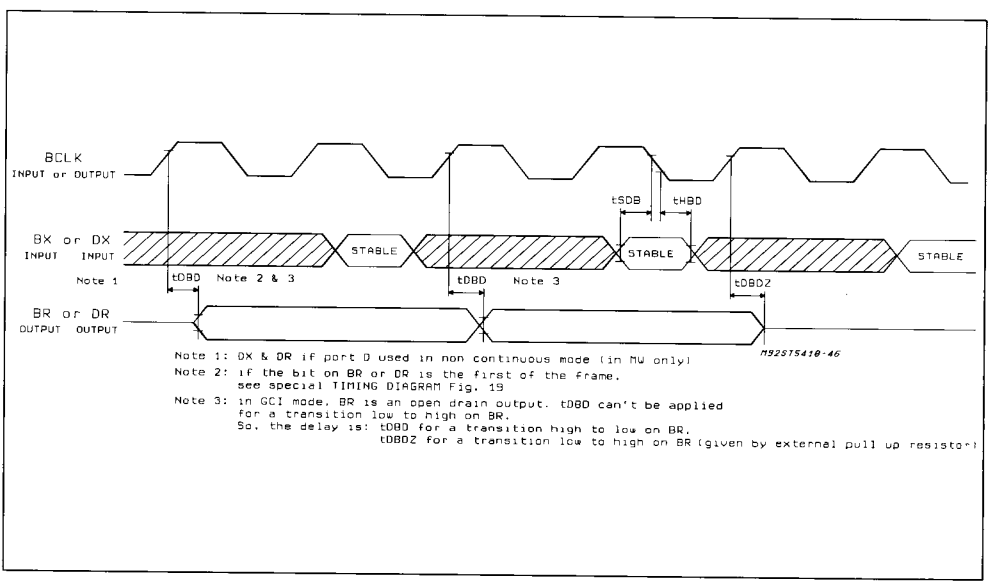


Figure 19: SPECIAL CASE BR, DR, ONLY FIRST BIT OF THE FRAME, IN SLAVE AND NON DELAYED MODES FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

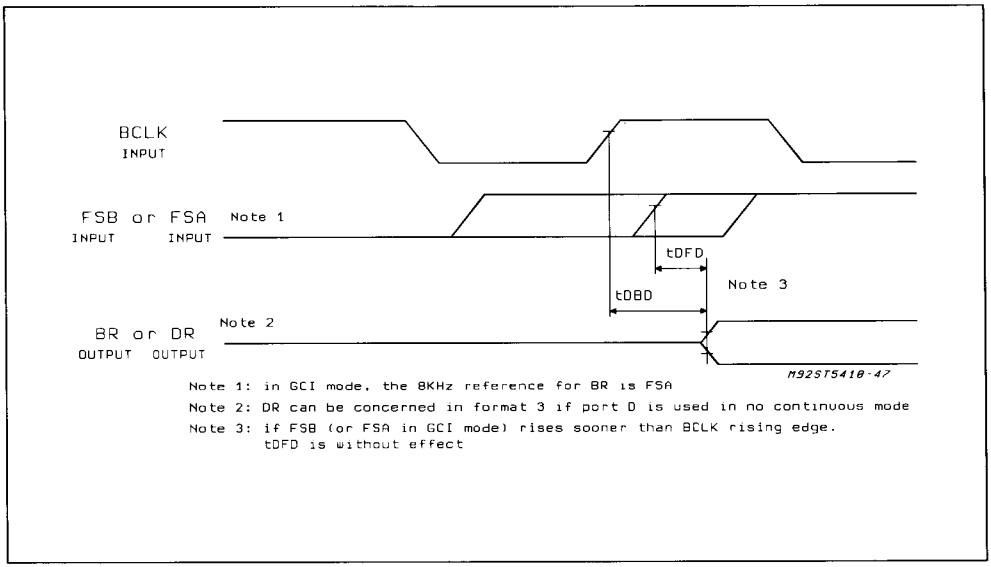


Figure 20: TSRB, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

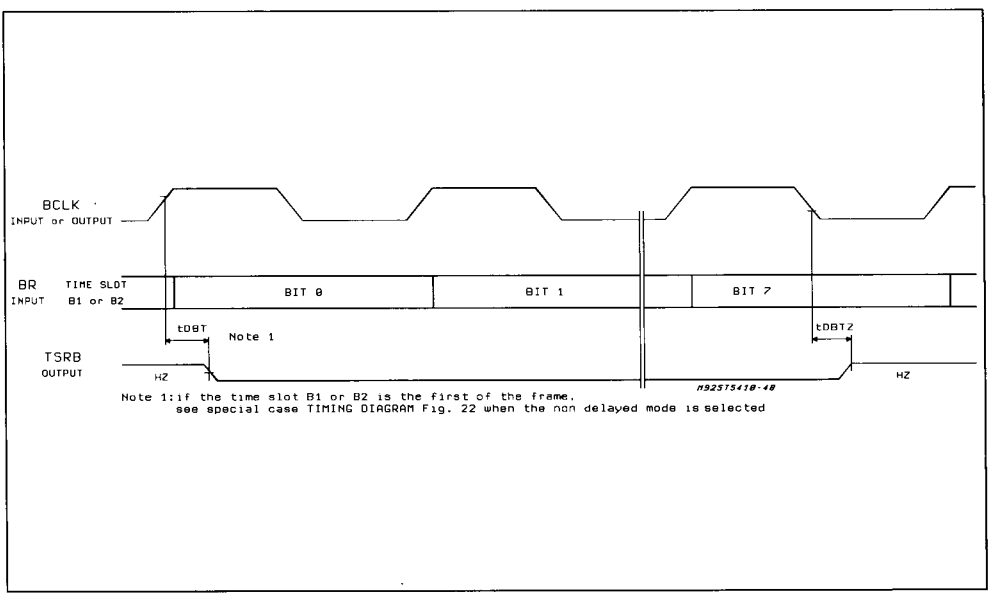


Figure 21: TSRB, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED MODE (MW & GCI)

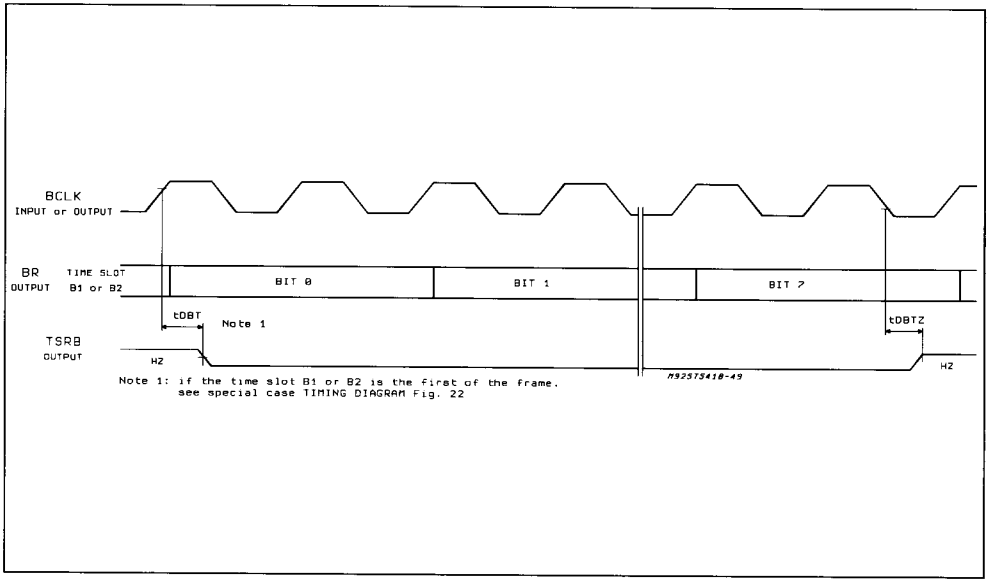


Figure 22: SPECIAL CASE TSRB, B1 OR B2 FIRST CHANNEL OF THE FRAME, IN SLAVE & NON DELAYED MODE, FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

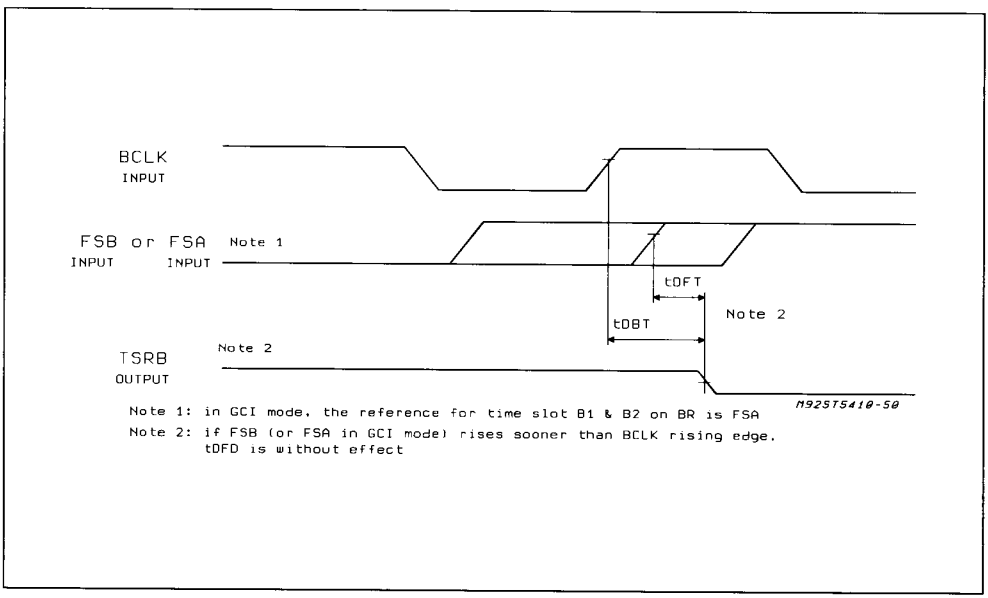


Figure 23: DCLK, DX, DR IN CONTINUOUS MODE SLAVE & MASTER, DELAYED & NON DELAYED MODES ALL FORMATS IN MW MODE ONLY

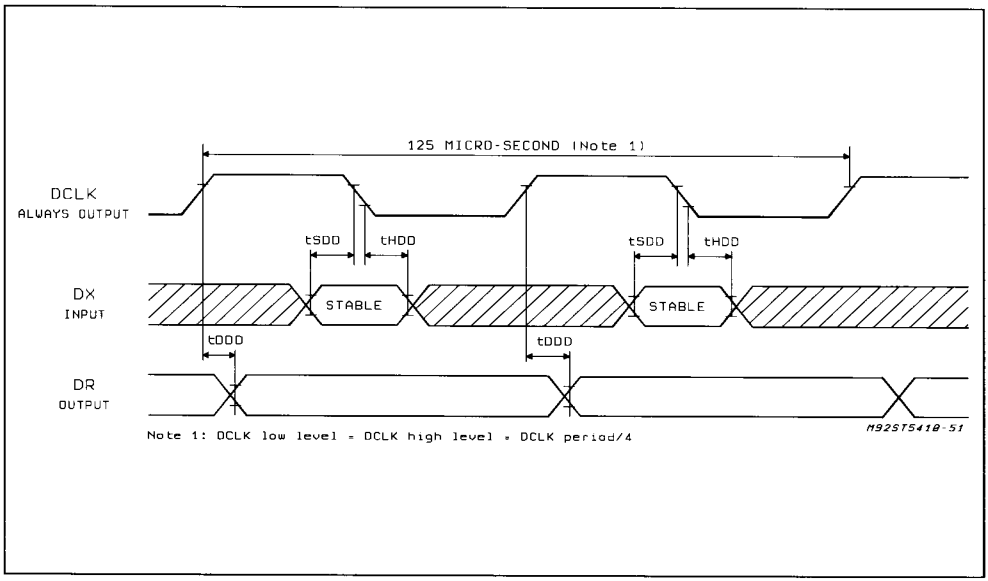


Figure 24: MW PORT

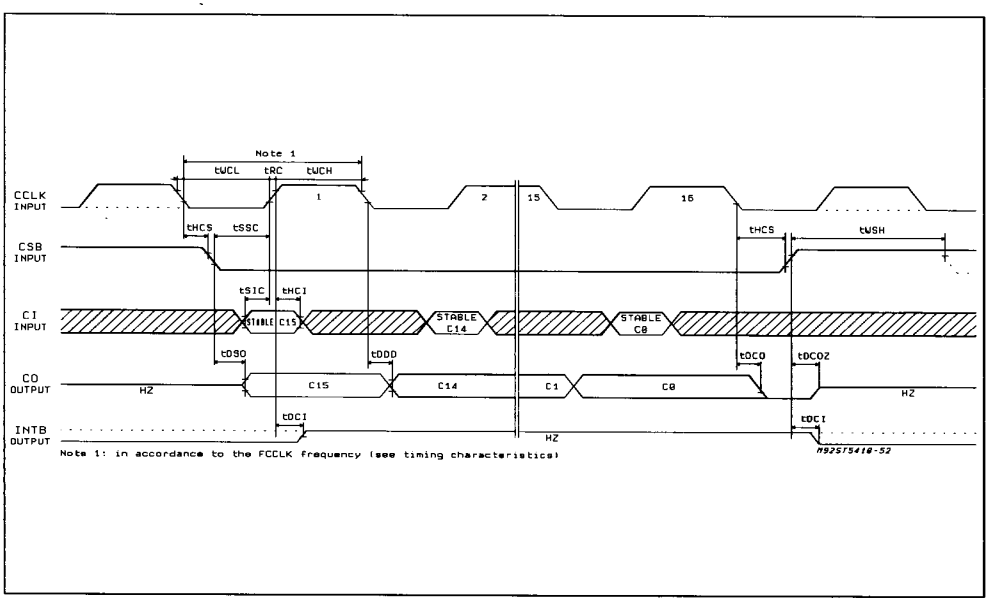


Figure 25: MCLK ALL MODES