CY2910A

CMOS Microprogram Controller

Features

- Fast
  - — CY2910AC has a 50-ns (min.) clock cycle; commercial
  - — CY2910AM has a 51-ns (min.) clock cycle; military
- Low power
  - — I_{CC} (max.) = 170 mA
- V_{CC} margin of 5V ±10% commercial and military
- Sixteen powerful micro-instructions
- Three output enable controls for three-way branch
- Twelve-bit address word
- Four sources for addresses: microprogram counter (MPC), branch address bus, 9-word stack internal holding register
- Internal 9-word by 12-bit stack can be used for subroutine return address or data storage
- 12-bit internal loop counter
- Capable of withstanding greater than 2001V static discharge voltage
- Pin compatible and functional equivalent to the Am2910A and Am29C10A

Functional Description

The CY2910A is a standalone microprogram controller that selects, stores, retrieves, manipulates, and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

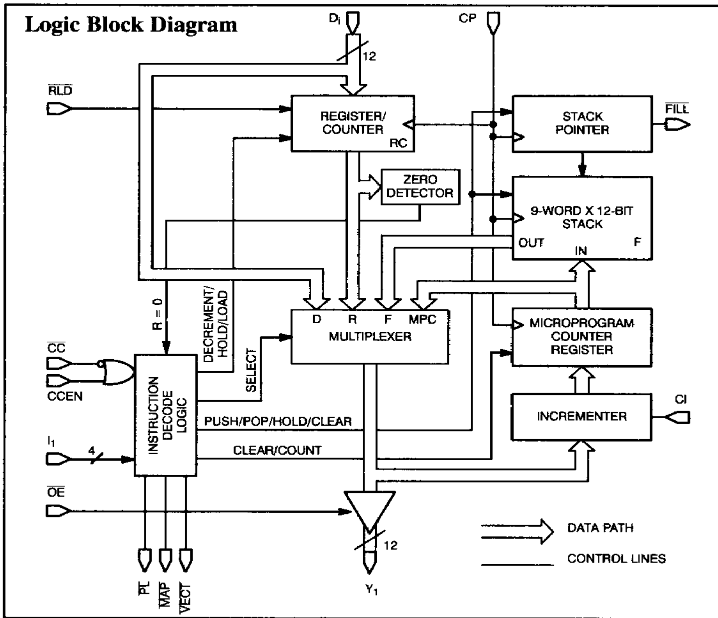
The CY2910A, as illustrated in the block diagram, consists of a 9-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (MicroProgram Counter) and incrementer, a 12-bit-wide by 4-input multiplexer, and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I_0 to I_3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the $Y_0 - Y_{11}$ pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY2910A is a pin-compatible, functional-equivalent, improved-performance replacement for the Am2910A.

The CY2910A is fabricated using an advanced 1.2-micron CMOS process that eliminates latch-up, results in ESD protection over 2001V, and achieves superior performance and low-power dissipation.

Logic Block Diagram



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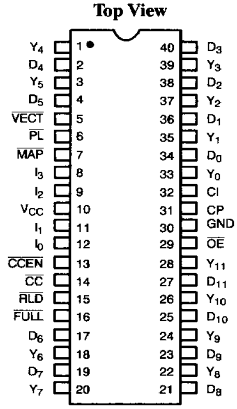
Pin Configuration



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Selection Guide

Minimum Clock Cycle (ns)	Stack Depth (words)	Operating Range	Part Number
50	9	Commercial	CY2910AC
51	9	Military	CY2910AM

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to +150°C

Ambient Temperature with Power Applied .... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30) .... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to +7.0V

DC Input Voltage .... – 3.0V to +7.0V

Output Current into Outputs (LOW) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current (Outputs) .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

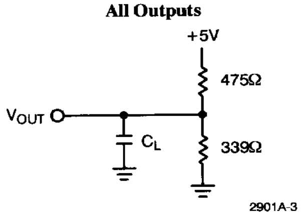
Electrical Characteristics Over Commercial and Military Operating Range[2, 3]

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 1.6 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage		– 3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		– 10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V	– 1.6		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.5V	8		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND or V_{CC}	– 40	+40	μA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = 0V		– 85	mA
I_{CC}	Supply Current	V_{CC} = Max.		170	mA

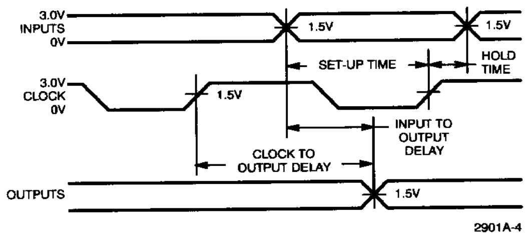
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Output Load for AC Performance Characteristics[6, 7]



Switching Waveforms



Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 50 pF includes scope probe, wiring, and stray capacitance.
7. C_L = 5 pF for output disable tests.

Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY2910A over the commercial (0°C to +70°C) and the military (−55°C to +125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

Clock Requirements[2, 8]

	Commercial	Military
Minimum Clock LOW	20	25
Minimum Clock HIGH	20	25
Minimum Clock Period I = 14	50	51
Minimum Clock Period I = 8, 9, 15[9]	50	50

Combinatorial Propagation Delays (C_L = 50 pF)[2, 8]

To Output	Commercial			Military		
From Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$
$D_0 - D_{11}$	20	—	—	25	—	—
$I_0 - I_3$	35	30	—	40	35	—
$\overline{CC}$	30	—	—	36	—	—
$\overline{CCEN}$	30	—	—	36	—	—
CP I = 8, 9, 15 (Note 9)	40	—	31	—	—	35
CP All Other I	40	—	31	46	—	35
$\overline{OE}$ (Note 10)	25 27	—	—	25 30	—	—

Minimum Set-Up and Hold Times Relative to clock LOW-to-HIGH transition (C_L = 50 pF)[2]

	Commercial		Military	
	Set-Up	Hold	Set-Up	Hold
DI ➧ RC	16	0	16	0
DI ➧ MPC	30	0	30	0
$I_0 - I_3$	35	0	38	0
$\overline{CC}$	24	0	35	0
$\overline{CCEN}$	24	0	35	0
CI	18	0	18	0
$\overline{RLD}$	19	0	20	0

Notes:

8. A dash indicates that a propagation delay path or set-up time does not exist.
9. These instructions are dependent upon the register/counter. Use the shorter delay times if the previous instruction either does not change the register/counter or could only decrement it. Use the longer delay if the instruction prior to the clock was 4 or 12 or if $\overline{RLD}$ was LOW.
10. The enable/disable times are measured to a 0.5V change on the output voltage level with C_L = 5 pF.

Table of Instructions

$I_3 - I_0$	Mnemonic	Name	REG/ CNTR Contents	Result: Fail $\overline{CCEN}$ = L and $\overline{CC}$ = H: Y	Fail: STACK	Pass $\overline{CCEN}$ = H or $\overline{CC}$ = L: Y	Pass: STACK	REG/ CNTR	Enable
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 11)	PL
5	JSPR	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠0	F	Hold	F	Hold	Dec	PL
			=0	PC	Pop	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠0	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠0	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

H = HIGH
L = LOW
X = Don't Care

Note:
11. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, then hold; else load.

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
50	CY2910A–DC	D18	Commercial
	CY2910A–JC	J67	
	CY2910A–LC	L67	
	CY2910A–PC	P17	
51	CY2910A–DMB	D18	Military
	CY2910A–LMB	L67	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3

Clock Requirements

Parameters	Subgroups
Minimum Clock LOW	7, 8, 9, 10, 11

Combinational Propagation Delays

Parameters	Subgroups
From $D_0 - D_{11}$ to Y	7, 8, 9, 10, 11
From $I_0 - I_3$ to Y	7, 8, 9, 10, 11
From $I_0 - I_3$ to $\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	7, 8, 9, 10, 11
From $\overline{CC}$ to Y	7, 8, 9, 10, 11
From $\overline{CCEN}$ to Y	7, 8, 9, 10, 11
From CP (I = 8, 9, 15) to $\overline{FULL}$	7, 8, 9, 10, 11
From CP (All Other I) to Y	7, 8, 9, 10, 11
From CP (All Other I) to $\overline{FULL}$	7, 8, 9, 10, 11

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Minimum Set-Up and Hold Times

Parameters	Subgroups
DI ♦ RC Set-Up Time	7, 8, 9, 10, 11
DI ♦ RC Hold Time	7, 8, 9, 10, 11
DI ♦ MPC Set-Up Time	7, 8, 9, 10, 11
DI ♦ MPC Hold Time	7, 8, 9, 10, 11
$I_0 - I_3$ Set-Up Time	7, 8, 9, 10, 11
$I_0 - I_3$ Hold Time	7, 8, 9, 10, 11
$\overline{CC}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{CC}$ Hold Time	7, 8, 9, 10, 11
$\overline{CCEN}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{CCEN}$ Hold Time	7, 8, 9, 10, 11
CI Set-Up Time	7, 8, 9, 10, 11
CI Hold Time	7, 8, 9, 10, 11
$\overline{RLD}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{RLD}$ Hold Time	7, 8, 9, 10, 11