ANALOG DEVICES

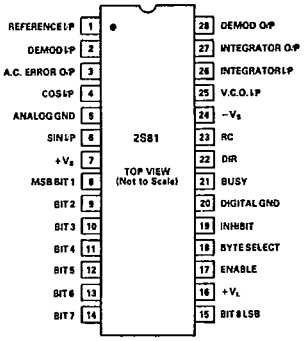
Low-Cost, Monolithic 12-Bit Resolver-to-Digital Converter

T-71-35-03 **2S81**

FEATURES
- Low Cost
- Monolithic Construction
- 28-Pin DIP Package
- Ratiometric Conversion
- Low Power Consumption: 300mW typical
- Dynamic Performance Set by User
- High Tracking Rate: 260 rps max
- Velocity Output

APPLICATIONS
- Brushless Motor Control
- Programmable Limit Switches
- Process Control
- Numerical Control of Machine Tools
- Robotics
- Axis Control

2S81 PIN CONFIGURATION



5

GENERAL DESCRIPTION

The 2S81 is a monolithic 12-bit tracking resolver-to-digital converter packaged in a 28-pin DIP. It is manufactured in Analog Devices' proprietary BiMOS II process which combines high-density and low-power CMOS logic with high-accuracy bipolar linear circuitry.

The converter can track resolver signals at rates up to 260 revolutions per second (15,600 rpm). Users can set the converter's dynamic performance with external components, providing greater flexibility in tailoring the converter to suit system requirements.

The 2S81 converts resolver format input signals into a 12-bit natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long lead lengths when the converter is located remotely from the resolver. The 12-bit output word is in a three-state digital logic form, available in 2 bytes on the 8 output data lines. BYTE SELECT and INHIBIT pins ensure easy data transfer. In addition, output pins are available to permit the use of external counters to count cycle or pitch. An analog signal proportional to velocity is also available.

PRODUCT HIGHLIGHTS

Monolithic: The single-chip construction reduces package size and increases inherent reliability.

Low Cost: The use of a single integrated circuit to perform the conversion ensures low cost.

Ratiometric Tracking Conversion: Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerates harmonic distortion in the reference and input signals.

Dynamic Performance Set by User: By selecting external resistor and capacitor values, the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low-cost preferred value resistors and capacitors.

Velocity Output: An analog signal proportional to velocity is linear to 1% (typical). This can be used in place of a velocity transducer in many applications to provide loop stabilization and velocity feedback data.

MODELS AVAILABLE

The 2S81 operates over 0 to +70°C temperature range. The reference frequency can range from 400 to 20,000Hz.

SPECIFICATIONS (typical at 25°C unless otherwise specified)

T-71-35-03

Model	2S81JD	Units	Notes
OVERALL CONVERTER SPECIFICATIONS (CONNECTED AS SHOWN IN FIGURE 1)			
Resolution	12	Bits	
Accuracy	±30 + 1LSB	Arc Minutes	Accuracy will be Affected by the Offset at the INTEGRATOR I/P.
Tracking Rate Range	0 to 260 (max)	rps	User Selected, Max Rate Limited at Lower Operating Frequencies.
Operating Frequency Range	400 to 20,000	Hz	
Repeatability of Position Output	1	LSB	
Bandwidth	User Selectable		
Velocity Signal			See "Using the Velocity Signal"
Linearity Over Full Range	±1 (typ), ±3 (max)	%	
Over 0 to 6000 rpm	±1 (max)	%	
Reversion Error	±5 (max)	%	Symmetry of $-V_S$ and $+V_S$ Power Supplies to be within ±5%.
	±2 (max)	%	With $-V_S$ Adjusted for Best Performance.
Zero Offset (for 260 rps Max Tracking Rate)	±6 (typ) + 16 (max)	mV	Depends on VCO I/P Resistor (R6).
Zero Offset Tempco (for 260 rps Max Tracking Rate)	−22	µV/°C	Depends on VCO I/PResistor (R6).
Gain Scaling Accuracy	±10	% FSD	
Output Voltage	±8	V dc	
Noise and Ripple (av-pk)	1.5	%	See Section "Using the Velocity Signal"
ANALOG INPUTS			
Protection	All Analog Inputs Are Diode Protected Against Overvoltage at ±8V		
REFERENCE INPUT			
Frequency	400 – 20,000	Hz	
Voltage Level Nominal	2	V rms	
max	11	V peak	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
SIGNAL INPUTS (SIN, COS)			
Frequency	400 – 20,000	Hz	
Allowable Phase Shift (Signal to Reference)	10	Degrees	
Voltage Level	2, ±10%	V rms	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Maximum Voltage Nominal	±8	V	
DIGITAL INPUTS	TTL-Compatible		
INHIBIT			
Sense	Logic LO to Inhibit		
Time to Data Stable (After Negative Going Edge of INHIBIT)	1	µs	
BYTE SELECT			
Sense	Logic HI Selects 8MSBs on Pins 8-15 Logic LO Selects 4LSBs on Pins 8-11; Pins 12-15 Are Logic LO		
Data Available (After Change in State)	150 (typ), 450 (max)	ns	
ENABLE			
Sense	Logic LO to Enable Position Outputs Logic HI Position Outputs in High Impedance State		
Enable and Disable Times	200 (typ), 550 (max)	ns	
ANALOG OUTPUTS			
Protection	Short Circuit Output Current Limited to ±8mA, ±30% Output Voltage Range Will Be Degraded for Currents >3mA		
Output Voltage Range (typ)	+9 to −9	V	
(max)	+10.5 to −10.5	V	
(min)	+8 to −8	V	
DIGITAL OUTPUTS			
Format	V_L = +5V TTL Compatible V_L = +12V CMOS Compatible		Voltage on V_L Sets the Voltage Level of Digital Outputs.

T-71-35-03

Model	2S81JD	Units	Notes
POSITION OUTPUTS			
Format	Three-State Natural Binary		
Resolution	12	Bits	
Number of Data Lines	8		Pins 8 to 15
Max Load	3	LSTTL	
Monotonicity	Guaranteed		
DIRECTION (DIR)			
Sense	Logic "HI" When Counting Up Logic "LO" When Counting Down		
Timing	Only Changes, if Required, at Start of Output Position Data Update Cycle		
Max Load	3	LSTTL	
RIPPLE CLOCK (RC)			
Sense	Positive Going Edge When Counting Up from All "1s" and When Counting Down from All "0s" as Data Changes		
Timing	Edge Occurs at Least 300ns Before Change in DIR Can Occur		
Width (min)	300	ns	
Reset	By Start of Next Data Update		
Max Load	3	LSTTL	
BUSY			
Sense	Logic "HI" When Converter Position Output Changing		
Timing	Positive Going Edge 50ns Before Change in Position Output		
Width (typ)	300	ns	
(min)	200	ns	
(max)	600	ns	
Load, (max)	3	LSTTL	
POWER SUPPLIES			The Device May Latch Up If $+V_S$ is Applied without $-V_S$.
Voltage Levels			
$+V_S$	$+12 \pm 10\%$	V	
$-V_S$	$-12 \pm 10\%$	V	
$+V_L$[5]	$+5$ to $+14$	V	
Current			
$+V_S$	12 (typ), 23 (max)	mA	
$-V_S$	12 (typ), 23 (max)	mA	
$+V_L$	0.5 (typ), 1.5 (max)	mA	
Power Dissipation	300 (typ), 600 (max)	mW	
GENERAL			
Operating Temperature Range	0 to +70	°C	
Storage Temperature Range	−65 to +150	°C	
Weight	0.2 (5)	Oz. (Grams)	

5

Model	2S81JD	Units	Notes
CONVERTER CHARACTERISTICS			
RATIO MULTIPLIER			
Function	AC ERROR Output Represents the Difference between the Angle at the SIN and COS Inputs Compared to the Position Output Angle		
AC Error Output Scaling	44.4	mV/Bit	
Accuracy	30	Arc Minutes	
Differential Nonlinearity	±0.25 (max)	LSB	
PHASE SENSITIVE DETECTOR			Specified Over the Operating Frequency Range. Tested at 1kHz.
Output Offset Voltage (max)	15	mV	
Gain of Signal (dc out, rms in)			
In Phase w.r.t. Reference	−0.9 ±2%		
In Quadrature w.r.t. Reference	±0.02 (max)		
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
INTEGRATOR			
Open Loop Gain at 10kHz	60 ±3	dB	
Output Impedance at 10kHz (max)	0.5	Ω	
Dead Zone Current	100	nA/LSB	See Section "Integrator"
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	60 (typ), 150 (max)	nA	
Output Voltage Range (min)	+8 to −8	V	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
VCO			
Maximum Rate	1.1	MHz	
VCO Rate	7.4 ±10%	kHz/μA	
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	120 (typ), 300 (max)	nA	
Input Bias Current Tempco	−0.55	nA/°C	
Input Voltage Range	+8 to −8	V	
Reversion Error	±5	%	
Linearity of Absolute Rate	+3	%	
Sensitivity of VCO Rate in "Up Direction" to $-V_S$	−7	%/V	
Sensitivity of VCO Rate in "Down Direction" to $-V_S$	+2	%/V	

NOTE
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1] . . . . . 0V to +14V dc
$-V_S$ . . . . . 0V to −14V dc
$+V_L$ . . . . . 0V to $+V_S$
Reference . . . . . +14V to $-V_S$
Sin . . . . . +14V to $-V_S$
Cos . . . . . +14V to $-V_S$
Any Logic Input . . . . . −0.4V to $+V_L$ dc
Demodulator Input . . . . . +14V to $-V_S$
Integrator Input . . . . . +14V to $-V_S$
VCO Input . . . . . +14V to $-V_S$

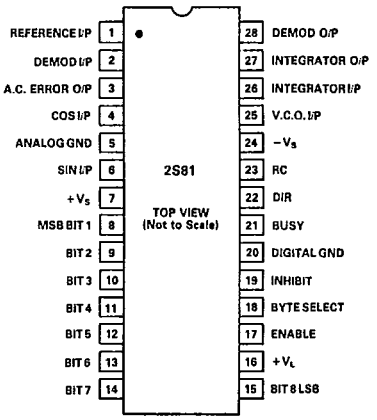
CAUTION:
1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

ORDERING INFORMATION

Model	Package Option*	Temperature Range	Operating Frequency Range
2S81JD	D-28	0 to +70°C	400 to 20,000Hz

*See Section 14 for package outline information.

PIN CONFIGURATION



OPERATION OF THE CONVERTER

When connected in a circuit such as is shown in Figure 1 the 2S81 operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. This means that the digital output will automatically follow the input for speeds up to the maximum tracking rate, set by the choice of external components. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

As the digital output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is *always* valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changes with a change in direction.

Both the RIPPLE clock pulse and DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$.

Position Output

The resolver shaft position is represented at the converter output by a natural binary digital word.

The static angular accuracy quoted is the worst case error that can occur over the full operating temperature range with the following input conditions:

a) Signal input amplitudes within 5% of the nominal values.

b) Signal and reference frequency within the specified operating range.

c) Phase shift between signal and reference less than 10 degrees.

d) Signal and reference waveform harmonic distortion less than 10 percent.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the converters can be used well outside these operating conditions providing the following points are observed.

Signal Amplitude (Sine and Cosine Inputs)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The 2S81 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

Reference Voltage Level

The amplitude of the reference signal applied to the converter's input is noncritical; however, it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

The 2S81 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

Harmonic Distortion

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 volts rms. (For example – a square wave should be 1.9V peak.)

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Velocity Signal

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

5

DC Error Signal

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is therefore proportional to the error between the input angle and the output digital angle. This is the DC ERROR of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators this voltage can be used as a "built-in test".

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm 12V$ and must not be reversed. If one rail is connected without the other, the converter will not operate and may "latch up". In this case the removal of both rails is necessary in order for the converter to function correctly again. The voltage applied to V_L can be $+5V$ to $+V_S$.

It is suggested that decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Suggested values are 100nF (ceramic) and 10μF (tantalum). Decoupling capacitors of 100nF and 10μF should also be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and ANALOG GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER". The two signal ground wires from the resolver should be joined at the ANALOG GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using twisted pair cables with the sine, cosine and reference signals twisted separately.

The external components required should be connected as shown in Figure 1.

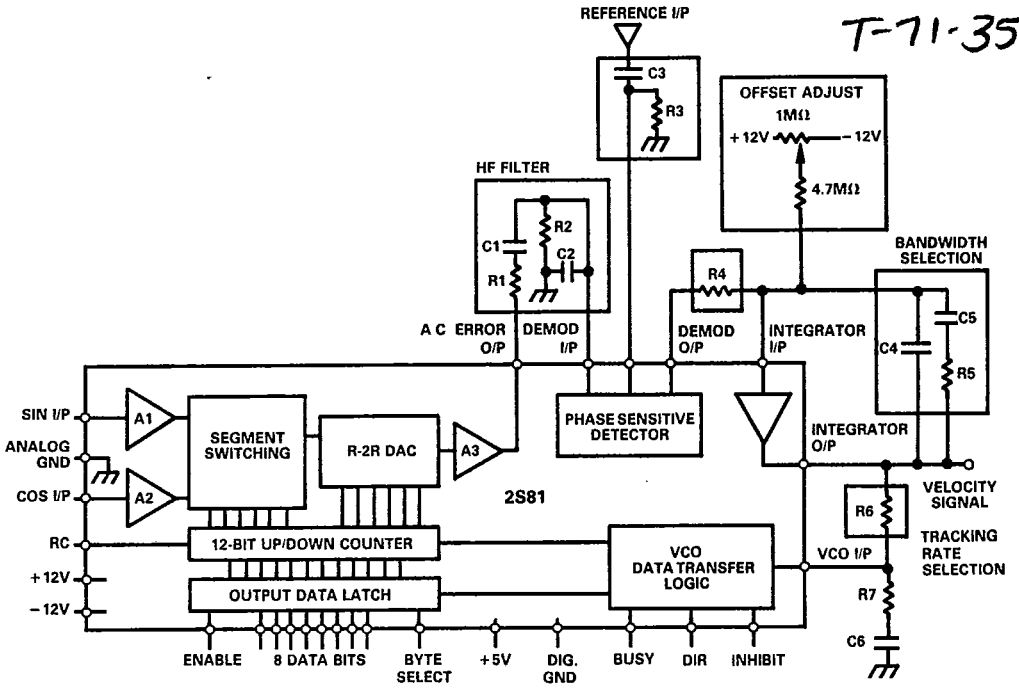


Figure 1. 2S81 Connection Diagram

COMPONENT SELECTION

The following instructions describe how to select the external components to the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used and a 5 percent tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE".

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to reduce the amount of noise present on the signal inputs to the 2S81 reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from a switch mode motor drive is present.

   Values should be chosen so that

   $R1 = R2 = 50k\Omega$ (max)

   $$C1 = C2 = \frac{1}{2\pi f_{REF} R1}$$

   and f_{REF} = Reference frequency (Hz)

   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted then: $R4 = 120k\Omega$

   If R1, C2 are not fitted then: $R4 = 390k\Omega$

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

   $R3 = 100k\Omega$

   $$C3 > \frac{1}{10^5 \times f_{REF}}$$

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate the velocity output will be 8 volts.

   Decide on your required maximum tracking rate, "T" in revolutions per second. Note that "T" must not exceed 260 rps and 1/8 of the reference frequency.

   $$R6 = \frac{14.5 \times 10^3}{T}\ k\Omega$$

   This gives a scale factor of $\frac{T}{8}$ rps/volt

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the Closed-Loop 3dB Bandwidth (B_{CL}) required ensuring that

      $f_{REF} > 2.5 \times B_{CL}$

      Typical values may be 100Hz for 400Hz reference frequency and 500 to 1000Hz for 5kHz reference frequency.

   b. Select C4 so that

      $$C4 = \frac{20.4 \times 10^{-3}}{R6 \times B_{CL}^2}$$

      with R6 in kΩ and B_{CL} in Hz selected above.

   c. C5 is given by

      $C5 = 5 \times C4$

   d. R5 is given by

      $$R5 = \frac{4}{2 \times \pi \times B_{CL} \times C5}\ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted.

   C6 = 470pF R7 = 68Ω.

7. Offset Adjust
   Input bias current at the integrator input can cause an additional positional offset at the output of the converter of 4 arc mins typical, 10 arc mins maximum. If this can be tolerated then the 4.7MΩ resistor and the 1MΩ potentiometer can be omitted from the circuit.

   To adjust for zero offset, ensure the resolver is disconnected and all the other external components are fitted. Connect COS to the REFERENCE INPUT and SIN to the ANALOG GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

   The potentiometer may be replaced by select on test resistors if preferred.

DATA TRANSFER

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:
The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

NOTE: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

ENABLE Input:
The ENABLE input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and application of a logic "LO" presents the data in the latches to the output pins. The operation of the ENABLE has no effect on the conversion process.

BYTE SELECT Input:
The BYTE SELECT input selects the byte of position data to be presented at the data output pins. A logic "HI" on the BYTE SELECT input will present the 8 most significant data bits on pins 8 to 15 when the ENABLE input is taken to a logic "LO". A logic "LO" will present the 4 least significant data bits on pins 8 to 11 and place a logic "LO" on pins 12 to 15 (with the ENABLE input taken to a logic "LO").

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

To transfer data the INHIBIT input should be used. The data will be valid 600ns after the application of a logic "LO" to the INHIBIT. This is regardless of the time when the INHIBIT is applied and allows time for an active BUSY to clear. By using the BYTE SELECT input the two bytes of data can be transferred after which the INHIBIT should be returned to a logic "HI" state to enable the output latches to be updated.

RIPPLE CLOCK (RC) and DIRECTION (DIR) Outputs: As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution or a pitch of the input has been completed. The pulse has a minimum width of 300ns and is reset by the start of the next data update cycle.

The DIRECTION (DIR) logic output indicates the direction of the input rotation, and this data is valid in advance of the RIPPLE CLOCK pulse and stays valid until the direction changes. This is the start of the next data update cycle – if the direction of rotation of the inputs has changed – and will be at least 300ns after the rising edge of the RIPPLE CLOCK (see Figure 2).

The DIR and RC outputs are unaffected by the state of the INHIBIT input.

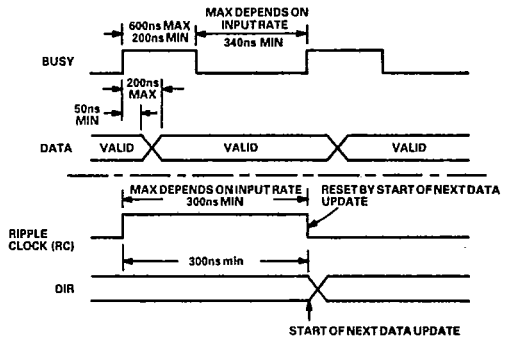


Figure 2. Timing Diagram

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The 2S81 allows the user great flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the exernal components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the 2S81 and the variations in the dynamic performance available to the user.

Loop Compensation

The 2S81 (connected as shown in Figure 1) behaves as a type 2 tracking servo loop where the VCO/counter combination and the Integrator perform the 2 integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0dB axis with 180 degrees of additional phase lag, as shown in Figure 4. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

A block diagram of the 2S81 is given in Figure 3.

Ratio Multiplier

The Ratio Multiplier is the input section of the 2S81 and compares the signal from the resolver inputs, θ, to the output digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by a mechanical device known by that name.

The AC ERROR signal is given by

AC ERROR OUTPUT = A1 sin $(\theta - \phi)$ sinωt.

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage, is 14.5 times

So for 2V rms input signals

AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{4096}\right) \times A1$$

$$= 44.5\text{mV/rms/bit}$$

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any DC offset at this point. Note, however, that the PSD of the 2S81 is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noise environments, and the user is advised to fit a simple HF filter (R1, C2) prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of the components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

T-71-35-03

Phase Sensitive Demodulator

The Phase Sensitive Demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (\text{DEMODULATOR INPUT rms voltage})$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error = 40mV/bit

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the 2S81 to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from 'flickering' (i.e., continually toggling by ± 1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 bit. In order to ensure that this feedback "hysteresis" is set to 1LSB the input current to the integrator must be scaled to be 100nA/bit. So

$$R4 = \frac{40\text{mV/bit}}{100\text{nA/bit}} = 400\text{k}\Omega$$ (390kΩ is the nearest preferred value).

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB (5.3 arc mins) of extra error will be added for each 100nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION".

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocked either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated although the reset period is constant at 400ns.

The VCO rate is fixed for a given input current by the VCO scaling factor,

$= 7.4\text{kHz}/\mu\text{A}$

This is equivalent to a tracking rate of 7400/4096 = 1.807 rps per μA of VCO input current.

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5 volt output at 100 rps (6000 rpm) the VCO input current must be:

$(100 \times 4096)/(7400) = 55.4\mu\text{A}$

Thus R6 would be set to: $5/(55.4 \times 10^{-6}) = 90\text{k}\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

Velocity Offset Voltage = R6 × (VCO bias current)

The temperature coefficient of this offset is given by

Velocity Offset Tempco = R6 × (VCO bias current tempco)

where the VCO bias current tempco is typically −0.55nA/°C.

The maximum recommended rate for the VCO is 1.1MHz which sets the maximum possible tracking rate at

$$1.1 \times \frac{10^6}{4096} \text{ revs/second}$$

Since the maximum voltage swing available at the integrator output is ±8 volts, this implies that the minimum value for R6 is 54kΩ. As

$$\text{Max Current} = \frac{1.1\ 10^6}{7.4 \times 10^3} = 149\mu\text{A}$$

$$\text{Min Value } R_6 = \frac{8}{149 \times 10^{-6}} = 54\text{k}\Omega$$

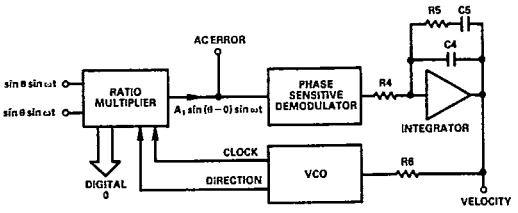


Figure 3. 2S81 Functional Diagram

Transfer Function

By selecting components using the method outlined in the section "Component Selection" the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1+s_N)}{(s_N+2.4)\,(s_N^2+3.4\,s_N+5.8)}$$

where, s_N, the normalized frequency variable is

$$s_N = \frac{2}{\pi}\,\frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A is given approximately by

$$K_A = 6 \times (f_{BW})^2 \quad \text{sec}^{-2}$$

The normalized gain and phase diagrams are given in Figures 4 and 5.

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter has settled to 1LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}}$$

The large signal step response (for steps greater than 10 degrees) applies when the error voltage will exceed the linear range of the converter. Typically the converter will take 3 times longer to reach the first peak for a 179° step.

In response to a velocity step the velocity output will exhibit the same time response characteristics as outlined above for the position output.

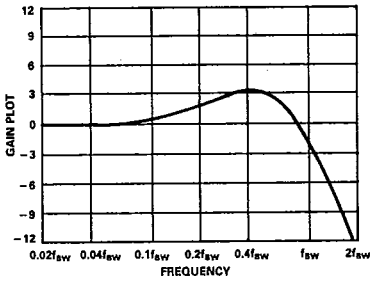


Figure 4. 2S81 Gain Plot

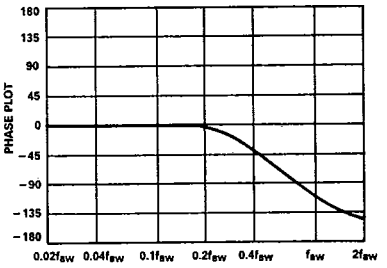


Figure 5. 2S81 Phase Plot

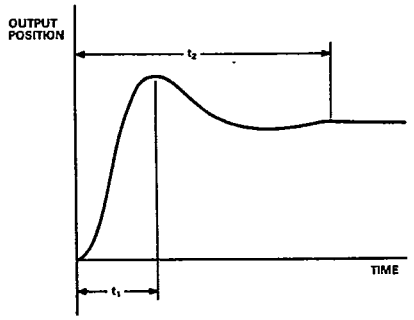


Figure 6. 2S81 Small Step Response

APPLICATIONS

Causes of Additional Error

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will be a maximum of 10 arc minutes over the operating temperature range, and if it can be tolerated in the performance of the converter, then the 4.7MΩ resistor and the 1MΩ potentiometer shown in Figure 1 can be omitted. (An offset of 40mV at the input to the integrator will cause an additional error of 1LSB in the accuracy of the converter.)

A description of how to adjust for zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and will cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$\text{Error} = 0.53\ a.b \text{ arc minutes}$$

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically effect the converter's static accuracy.

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

T-71-35-03

$$\frac{22 \times 20}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

Using the Velocity Signal

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in place of a velocity transducer. Although the conversion loop of the 2S81 includes a digital section there is an additional totally analog feedback loop around the velocity signal. This ensures that there is no digital effects on the output signal and that the loop is closed even when the input signals are such that the digital output does not change.

A better quality velocity signal will be achieved if the following points are considered.

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion Error.
   If necessary, the reversion error can be reduced by a simple trimming circuit. Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO. Because the sensitivity of the VCO rate to $-V_S$ depends on the direction of rotation, the reversion error can be reduced by varying the magnitude of $-V_S$. By trimming a reversion error of less than 1% is achievable.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using screened separate twisted pair cables for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has a low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the 2S81 with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   The signal voltages are 2V rms to prevent a ripple at the LSB switching rate. This is because the 1LSB of analog feedback that prevents the output from flickering will be incorrectly scaled (see section "INTEGRATOR").

   If the above precautions are taken, a very good noise and ripple performance is obtainable making the 2S81 velocity signal usable in very noisy environments, for instance in motor drive applications with PWM switching noise.

   The positional error curve of the converter and the resolver will result in an apparent acceleration when the resolver is rotating at a constant velocity. The main result of this will be a ripple on the velocity signal twice per revolution.

Connecting the Resolver
The recommended connection circuit is shown in Figure 7.

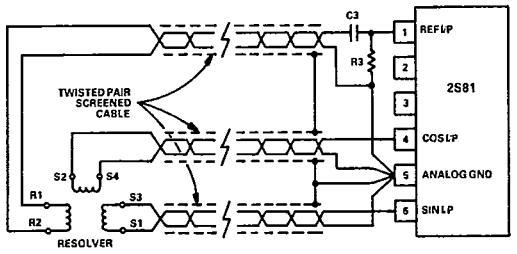


Figure 7. Connecting the 2S81 to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $= \frac{1}{2\pi R C}$

By altering the value of R2 the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

For signal and reference voltages greater than 2V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

Typical Circuit Configuration
Figure 8 shows a typical circuit configuration for the 2S81. Values of the external components have been chosen for a reference frequency of 5kHz and to give a maximum tracking rate of 260 rps and a bandwidth of 520Hz. The resistors are 0.25W (except for the 4.7MΩ which is 0.5W) 5 percent tolerance preferred values. The capacitors are 100V ceramic 5 percent tolerance components.

An offset adjustment potentiometer is included at the integrator input to remove the offset error. Obviously this can be left out of the circuit if the extra inaccuracy can be tolerated.

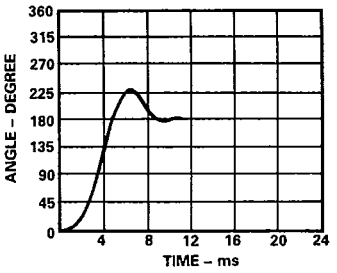


Figure 9. Large Step Response Curves for Typical Circuit Shown in Figure 8

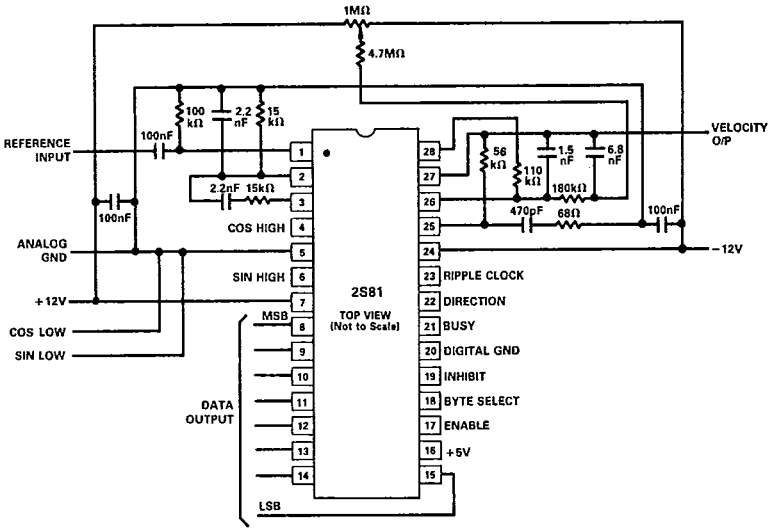


Figure 8. Typical Circuit for the 2S81