T-52-31

54AC16474, 54ACT16474
74AC16474, 74ACT16474
18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0250—D3573, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16474, 54ACT16474 ... WD PACKAGE
74AC16474, 74ACT16474 ... DL PACKAGE
(TOP VIEW)

1$\overline{OEAB}$	1	56	1$\overline{OEBA}$
1CLKAB	2	55	1CLKBA
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
V_{CC}	7	50	V_{CC}
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
2CLKAB	27	30	2CLKBA
2$\overline{OEAB}$	28	29	2$\overline{OEBA}$

description

The 'AC16474 and 'ACT16474 are noninverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$) and clock (1CLKAB or 2CLKAB) inputs. When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs are active (high or low logic levels) and take on either the current A-bus data on a low-to-high transition of 1CLKAB (or 2CLKAB) or the previously stored A-bus data if 1CLKAB (or 2CLKAB) is low.

When 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is similar, but uses 1$\overline{OEBA}$ and/or 2$\overline{OEBA}$ and 1CLKBA and/or 2CLKBA.

FUNCTION TABLE, EACH SECTION†

INPUTS		LATCH DATA	B OUTPUTS
CLKAB	$\overline{OEAB}$		
L	L	Previous A Data	Previous A Data
L	H	Previous A Data	Z
↑	L	Current A Data	Current A Data
↑	H	Current A Data	Z

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by CLKBA and $\overline{OEBA}$.

PRODUCT PREVIEW

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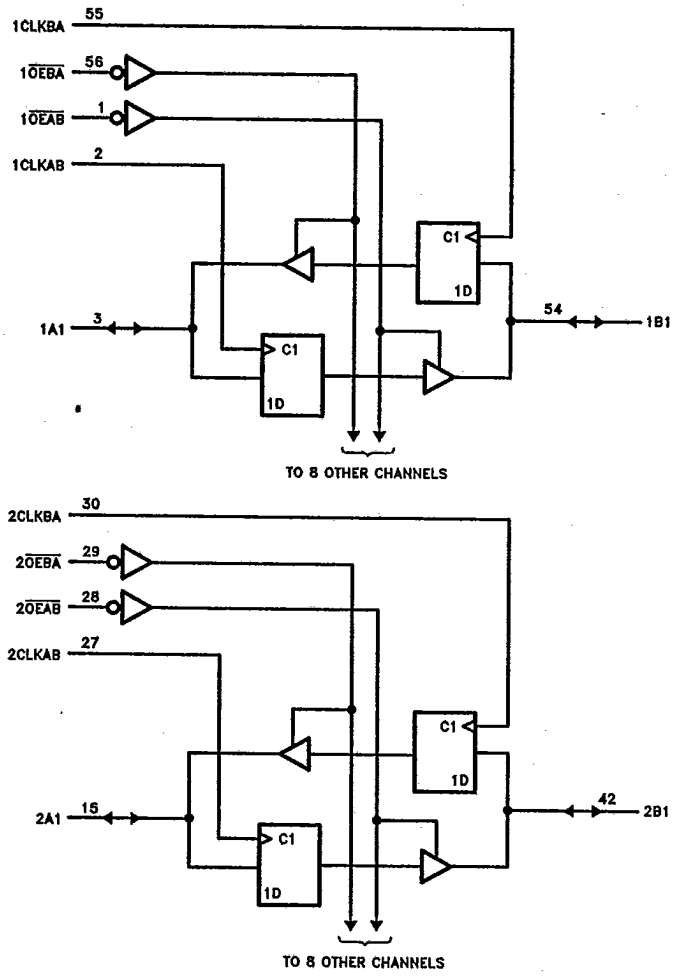
The 74AC16474 and 74ACT16474 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16474 has CMOS-compatible input thresholds. The 'ACT16474 has TTL-compatible input thresholds.

The 54AC16474 and 54ACT16474 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16474 and 74ACT16474 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)



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