élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4393C

Triple 80 MHz Video Amplifier w/Disable

Features

- 80 MHz −3 dB bandwidth for gains of 1 to 10
- 900 V/μs slew rate
- 10 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible
- Available in SOL-16

Applications

- RGB drivers
- RGB multiplexers
- RGB gain blocks
- Video gain blocks
- Coax cable driver
- ADC drivers/input multiplexer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4393CN	−40°C to +85°C	16-Lead P-DIP	MDP0031
EL4393CM	−40°C to +85°C	16-Lead SOL	MDP0027

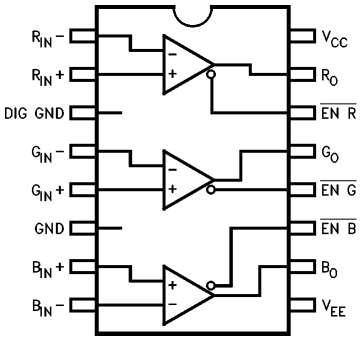
General Description

The EL4393C is three wideband current-feedback amplifiers optimized for video performance. Each amplifier can drive a load of 150Ω at video levels. Each amplifier has a disable capability, which is controlled by a TTL/CMOS compatible logic signal. The EL4393C operates on supplies as low as ±4V up to ±15V.

Being a current-feedback design, the bandwidth stays relatively constant at approximately 80 MHz over the ±1 to ±10 gain range. The EL4393C has been optimized for use with 1300Ω feedback resistors at a gain of 2.

When the outputs are disabled, the supply current consumption drops, by about 4 mA per channel that is disabled. This feature can be used to reduce power dissipation.

Connection Diagram



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Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S^+ and V_S^-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S^+	+18V	Operating Ambient Temperature Range	−40°C to +85°C
Voltage at V_S^-	−18V	Operating Junction Temperature	150°C
Voltage between V_{IN}^+ and V_{IN}^-	±6V	Storage Temperature Range	−65°C to +150°C
Current into V_{IN}^+ or V_{IN}^-	5 mA		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1 KΩ

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	+25°C		2	±15	I	mV
TCV_{OS}	Temperature Coefficient of V_{OS}	Full		50		V	µV/°C
I_B^+	I_{IN}^+ Input Bias Current	+25°C		0.2	5	I	µA
I_B^-	I_{IN}^- Input Bias Current	+25°C		10	65	I	µA
TCI_B^-	Temperature Coefficient of I_B^-	Full		25		V	nA/°C
CMRR	Common-Mode Rejection Ratio (Note 1)	+25°C	50	58		I	dB
−ICMR	I_{IN}^- Input Common-Mode Current (Note 1)	+25°C		3	8	I	µA/V
PSRR	Power Supply Rejection Ratio (Note 2)	+25°C	50	58		I	dB
−IPSR	I_{IN}^- Current Supply Rejection (Note 2)	+25°C		2	5	I	µA/V
R_{OL}	Transimpedance	+25°C	100	217		I	kΩ
R_{IN}	IN^+ Input Impedance	+25°C		2		I	MΩ
V_{IN}	IN^+ Input Range	+25°C	±13	±13.5		I	V
V_O	Output Voltage Swing; R_L = 1 kΩ	+25°C	±12	±13		I	V

TD is 3.4in

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{SC}	Short-Circuit Current (Note 3)	+25°C	40	70		I	mA
$I_{O, DIS}$	Output Current when Disabled	+25°C		5	150	I	µA
DIS V_{IL}	Disable Voltage for Logic Low	+25°C			0.8	I	V
DIS V_{IH}	Disable Voltage for Logic High	+25°C	2.2			I	V
DIS I_{IL}	Disable Logic Low Input Current	+25°C		3	25	I	µA
DIS I_{IH}	Disable Logic High Input Current	+25°C		0	5	I	µA
$I_{CC (en)}$	Positive Supply Current all Channels Enabled	+25°C	15	20	±29	I	mA
$I_{CC (dis)}$	Positive Supply Current all Channels Disabled	+25°C	6	11	16	I	mA
$I_{EE (en)}$	Negative Supply Current all Channels Enabled	+25°C	13	18	±28	I	mA
$I_{EE (dis)}$	Negative Supply Current all Channels Disabled	+25°C	4	9	14	I	mA

Note 1: V_{CM} = ±10V for V_S = ±15V.
Note 2: V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
Note 3: Only one output short circuited. Pulse test or use heatsink.

Closed Loop AC Electrical Characteristics Supplies at ±15V, Load = 150Ω and 15 pF, except where noted. Rf1 and Rf2 = 1500Ω; A_V = 2, T_A = 25°C. (See note 8 re: test fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 4)		960		V	V/µs
SR	Slew Rate w/ ±5V Supplies (Note 5)		470		IV	V/µs
t_s	Settling Time to 1% $5V_{p-p}$ 5V Step (Note 6)		32		V	ns
BW	Bandwidth, −3 dB ±5V Supplies, −3 dB		80 60		IV IV	MHz MHz
BW	Bandwidth, −0.1 dB ±5V Supplies, −0.1 dB		16 21		IV IV	MHz MHz
Peaking	−3 dB BW Tests		0.6		IV	dB
dG	Differential Gain at 3.58 MHz at ±5V Supplies (Note 7)		0.03 0.30		V V	% %
dθ	Differential Phase at 3.58 MHz at ±5V Supplies (Note 7)		0.088 0.096		V V	(°) (°)

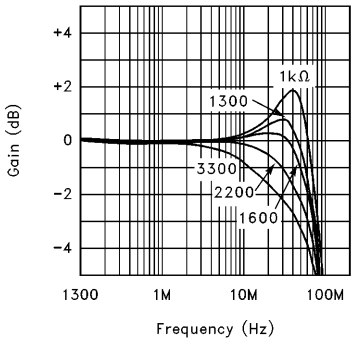
Note 4: R_L = 300Ω, −5V to +5V swing, SR measured at 20% to 80%.
Note 5: −2V to +2V swing, SR measured at 20% to 80%.
Note 6: R_L = 300Ω.
Note 7: DC offset from −0.7V through +0.7V AC amplitude is 286 mV_{P-P}, equivalent to 40 ire.
Note 8: Test fixture was designed to minimize capacitance at the I_N^+ input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

TD is 2.7in

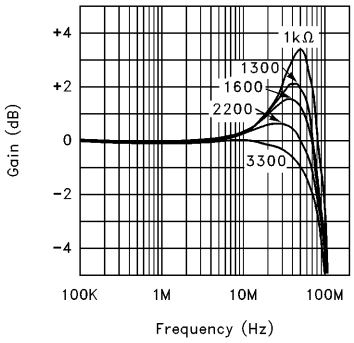
TD is 2.4in

Typical Performance Curves

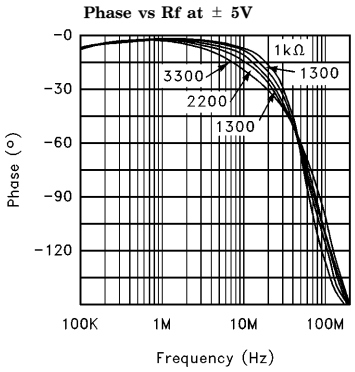
Gain Flatness vs Rf at ± 5V



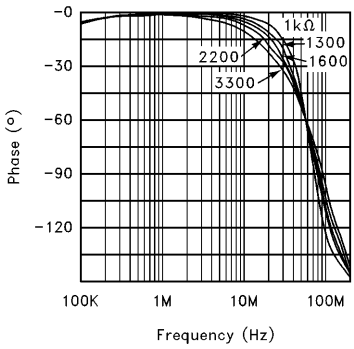
Gain Flatness vs Rf at ± 15V



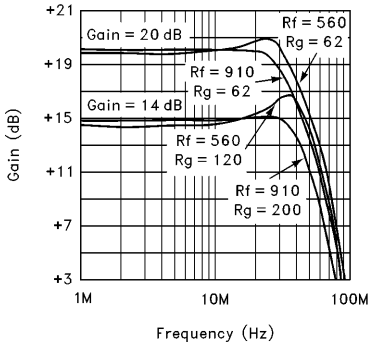
Phase vs Rf at ± 5V



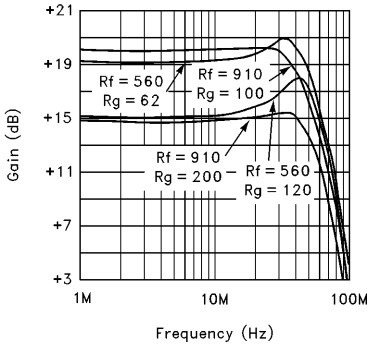
Phase vs Rf at ±15V



Gain of 5, 10 vs Various Rf, Rg at ±5V



Gain of 5, 10 vs Rf, Rg at ± 15V



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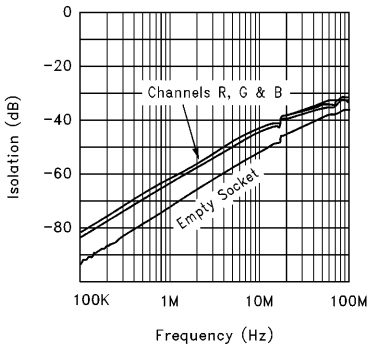
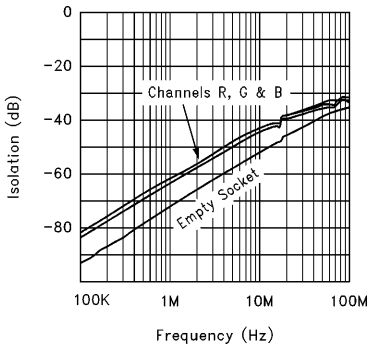
Typical Performance Curves — Contd.

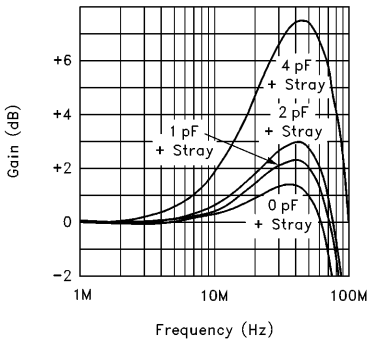
Disabled Isolation Test at ±5V



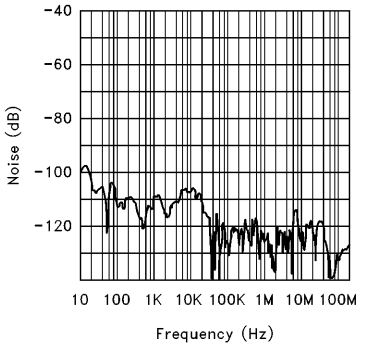
Disabled Isolation Test at ± 15V



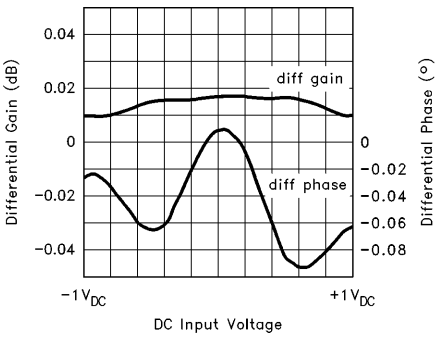
Cin—vs Peaking



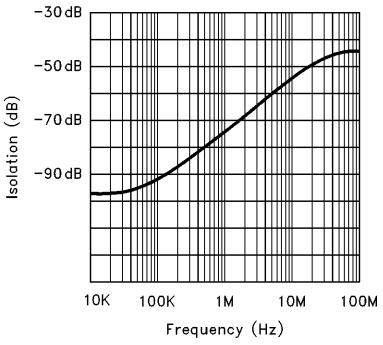
Voltage Noise



Differential Gain & Phase at 3.58 MHz



EL4393 MUX Channel Channel Isolation



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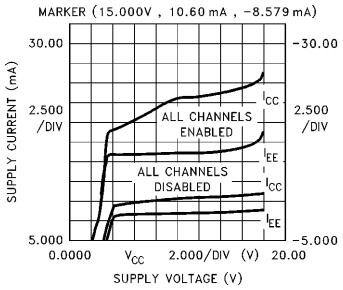
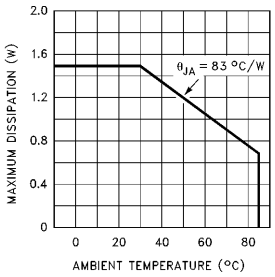
Typical Performance Curves — Contd.

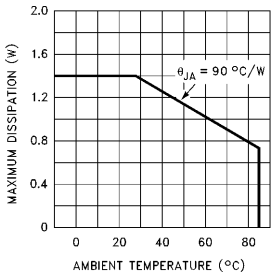
Supply Current vs Supply Voltage



Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP



Maximum Power Dissipation vs Ambient Temperature— 16-Pin SOL



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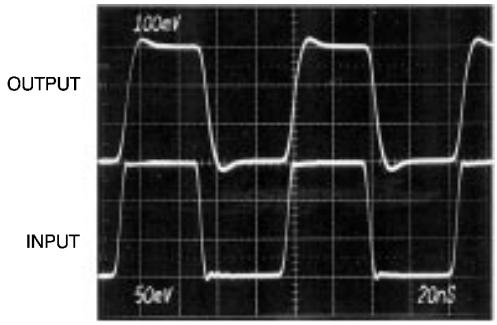
Small Signal Pulse Response



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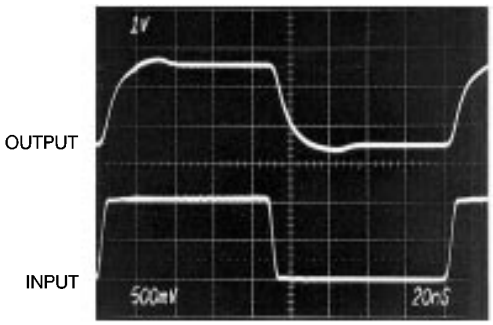
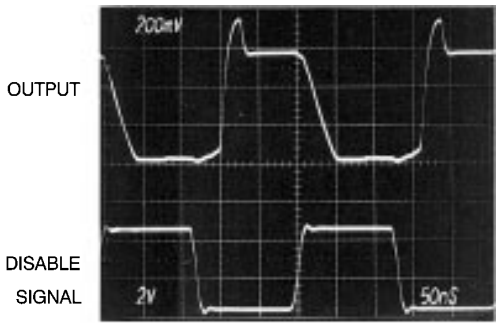
Large Signal Pulse Response



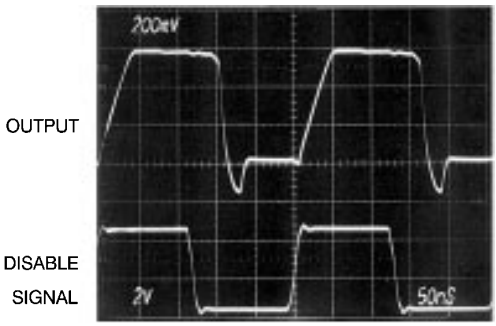
4393-6

Enable/Disable with + VE Voltage Output



4393-7

Enable/Disable with − VE Voltage Output



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Typical Application for EL4393, and General Rules for PCB Layout

The figure shows two EL4393's configured as a 2:1 RGB multiplexer, and cable driver, driving 75Ω, back terminated cables. Each channel of the EL4393 is configured to give a gain of two, to make up for the losses of the back terminating resistor.

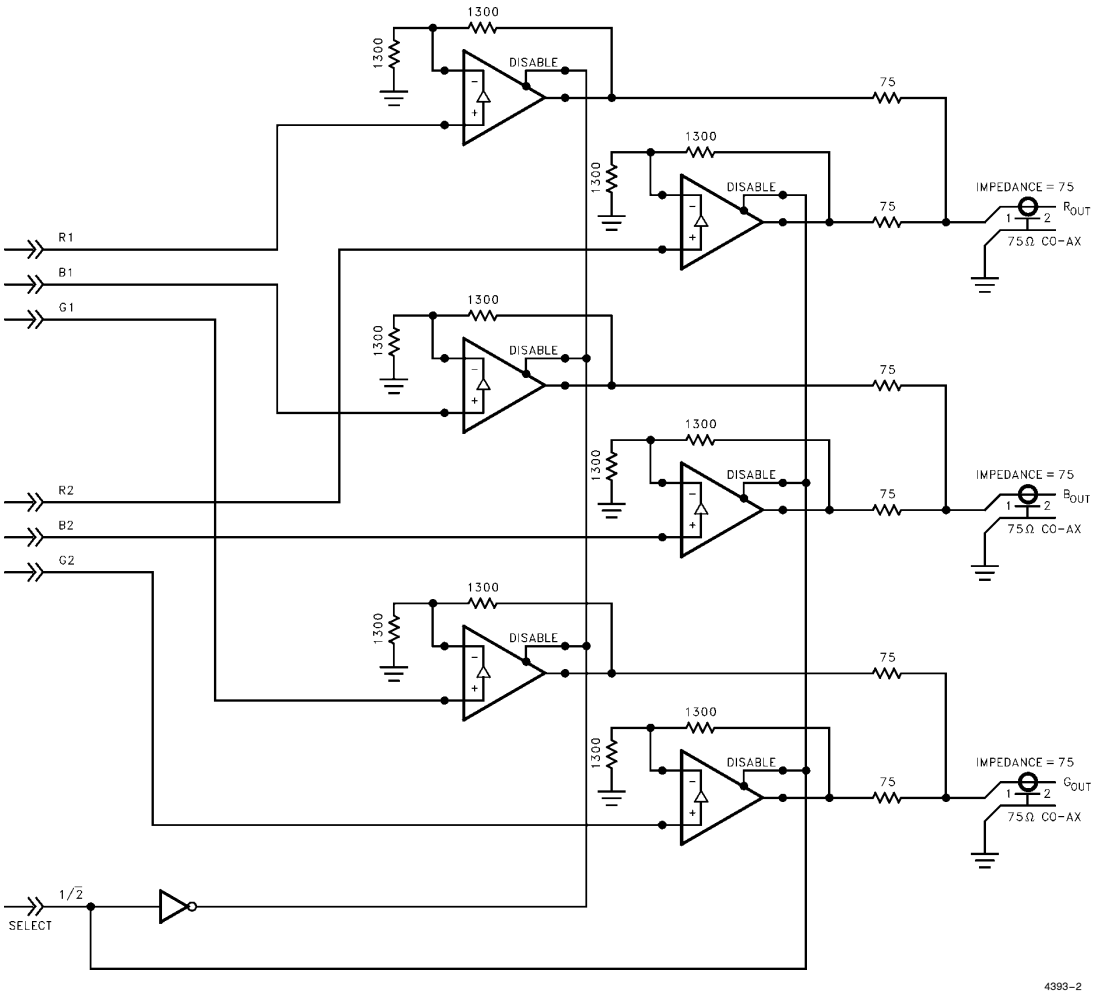
In this example, the Disable pins of each RGB section are driven by a complementary TTL "select" signal. Larger multiplexers can be assembled, with a 1-of-n TTL decoder selecting each RGB triplet.

The circuit gives channel isolations of typically better than −50 dB at 10 MHz, and with a 20 dB/decade slope, extending down to better than −90 dB at frequencies below 100 kHz.

The schematic does not show things like power supply decoupling, or pcb layout, grounding and signal returns, but these will all affect the overall performance of the circuit, and care should be taken with these aspects.

It is recommended that the V_{CC} and V_{EE} pins each be decoupled by a 0.1 μF NPO or X7R dielectric ceramic capacitors to ground within 0.1 inch of the part, and in parallel with the 0.1 μF, A 47 μF tantalum capacitor, also to ground. The 47 μF capacitors should be within 0.25 inch of their power pins. The ground plane should be underneath the package, but cut away from the In− inputs. Care should be taken with the center channel feedback—it must be kept away from any of the in+ or in− pins, if it has to go under the package. Route the G-out line between the pin 3 ground and the pin 4 In− if going under the package is essential. Otherwise, loop the G-out trace around all the other circuitry, to its Rf resistor. The Rf and if used, Rg resistors should be on the input side of the package, to minimize trace length on the In− pins.

The digital input disables are on the output side of the package, so that a good ground plane down the center of the board underneath the package will isolate any fast edges from the sensitive inputs.



Typical Application Circuit

TAB WIDE

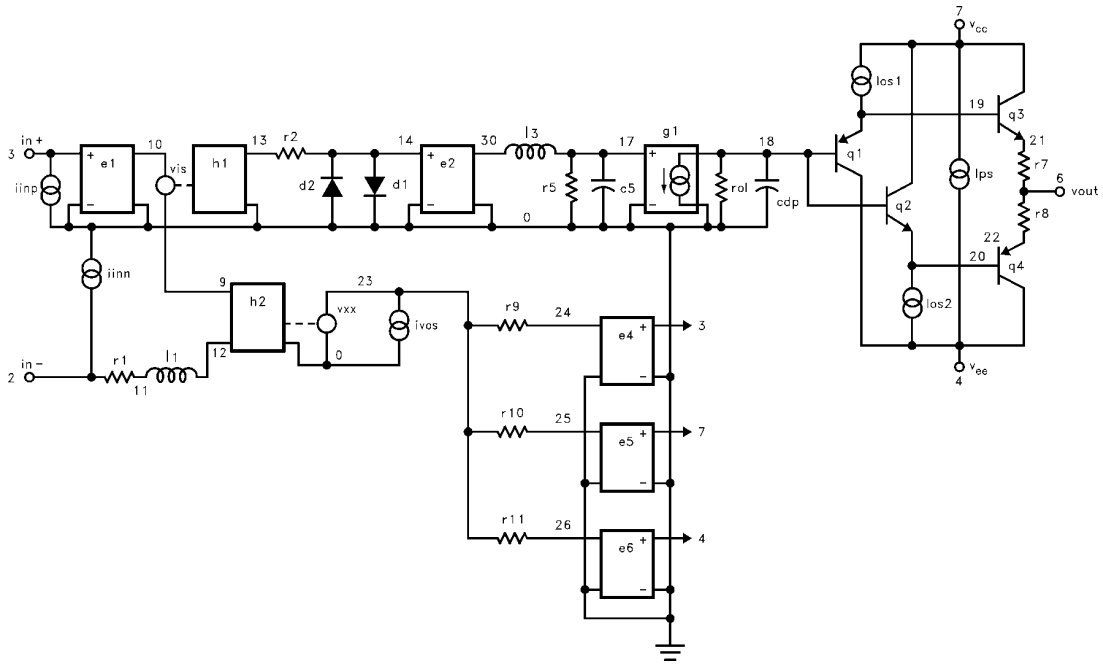
EL4393C Macromodel

```
* Revision A, July 1993
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:          +input
*                       |     -Input
*                       |     |     +Vsupply
*                       |     |     |     -Vsupply
*                       |     |     |     |     Putput
*                       |     |     |     |     |
* subckt EL4393/EL       3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l 1 11 12 29 nH
iinp 3 0 0.2 μA
iinm 2 0 10 μA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l5 30 17 1.2 μH
c5 17 0 1 pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 250k
cdp 18 0 2.2 pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5 mA
ios2 20 4 2.5 mA
*
* Error Terms
*
ivos 0 23 2 mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 33 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.2nS)
.model qp pnp (is=5e-15 bf=100 tf=0.2nS)
.model dclamp d (is=1e-30 ibv=0.266 bv=1.5 n=4)
.ends
```

TD is 3.6in

TD is 5.3in

EL4393C Macromodel — Contd.



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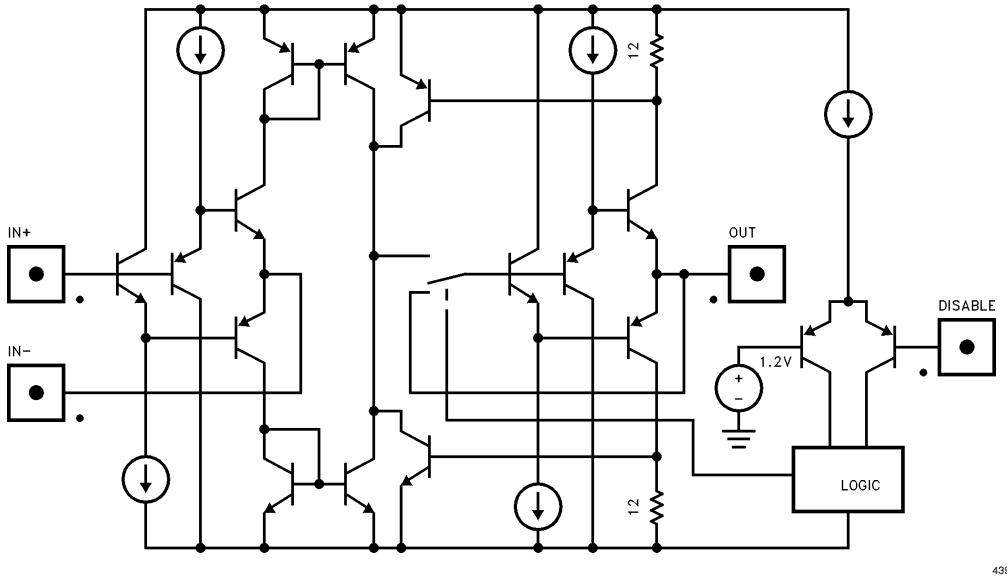

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Simplified Schematic of One Channel of EL4393

BLANK

EL4393C
Triple 80 MHz Video Amplifier w/Disable

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