Integrated Device Technology, Inc.

HIGH-SPEED 2K X 8 FOURPORT™ STATIC RAM

IDT7052S/L

FEATURES:

- High-speed access
  - — Military: 20/25/35/45ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power operation
  - — IDT7052S
    Active: 750mW (typ.)
    Standby: 10mW (typ.)
  - — IDT7052L
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- True Four-Port memory cells which allow simultaneous reads of the same memory locations
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

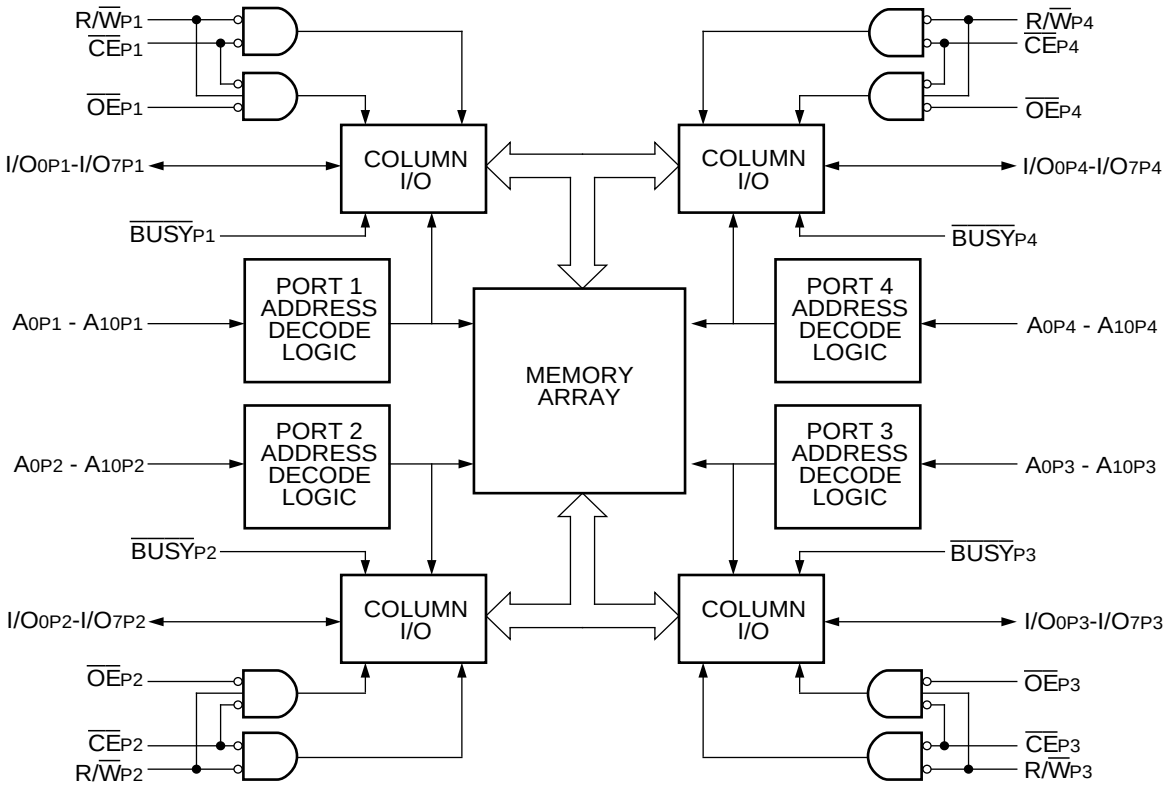
DESCRIPTION:

The IDT7052 is a high-speed 2K x 8 FourPort Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7052 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location

FUNCTIONAL BLOCK DIAGRAM



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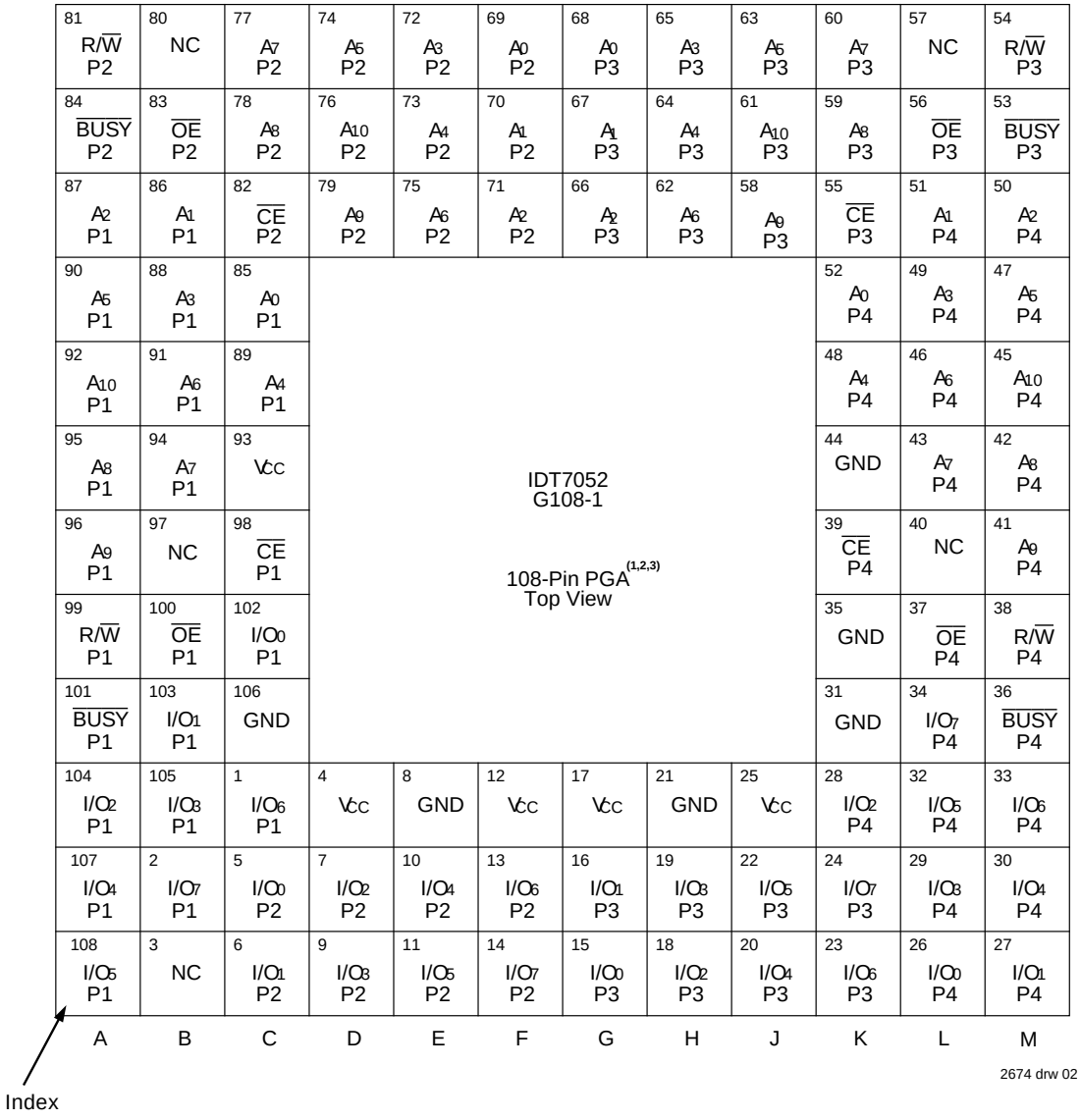
from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CMOS high-performance technology, this four port RAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7052 is packaged in a ceramic 108-pin PGA, a plastic 132-pin quad flatpack, and a 120-pin thin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

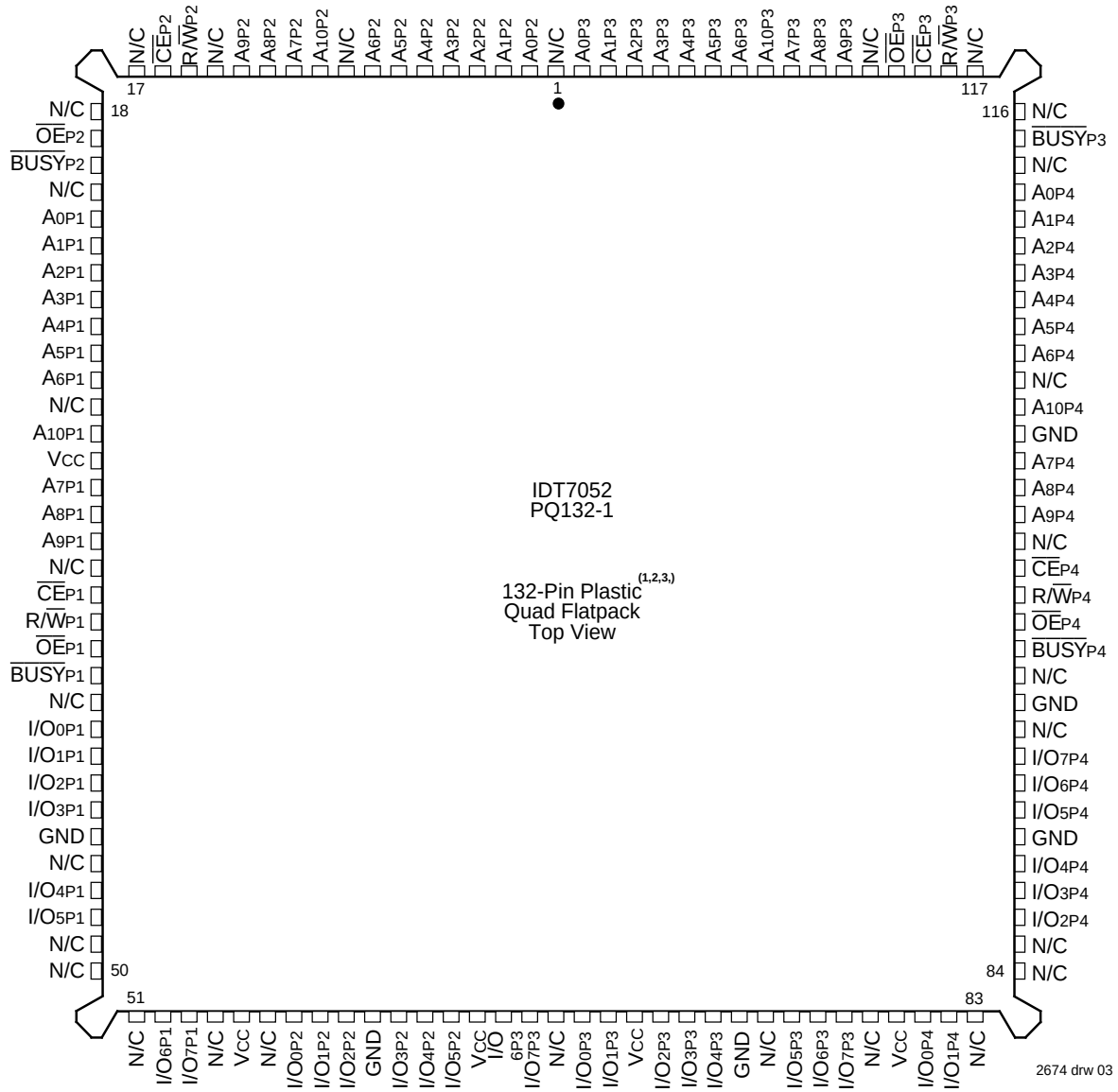
PIN CONFIGURATIONS



	A	B	C	D	E	F	G	H	J	K	L	M	
12	81 R/$\overline{W}$ P2	80 NC	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 NC	54 R/$\overline{W}$ P3	12
11	84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A_8 P2	76 A_{10} P2	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 A_{10} P3	59 A_8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
10	87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
09	90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
08	92 A_{10} P1	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 A_{10} P4	08
07	95 A_8 P1	94 A_7 P1	93 V_{CC}							44 GND	43 A_7 P4	42 A_8 P4	07
06	96 A_9 P1	97 NC	98 $\overline{CE}$ P1							39 $\overline{CE}$ P4	40 NC	41 A_9 P4	06
05	99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
04	101 $\overline{BUSY}$ P1	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 $\overline{BUSY}$ P4	04
03	104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
02	107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
01	108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01

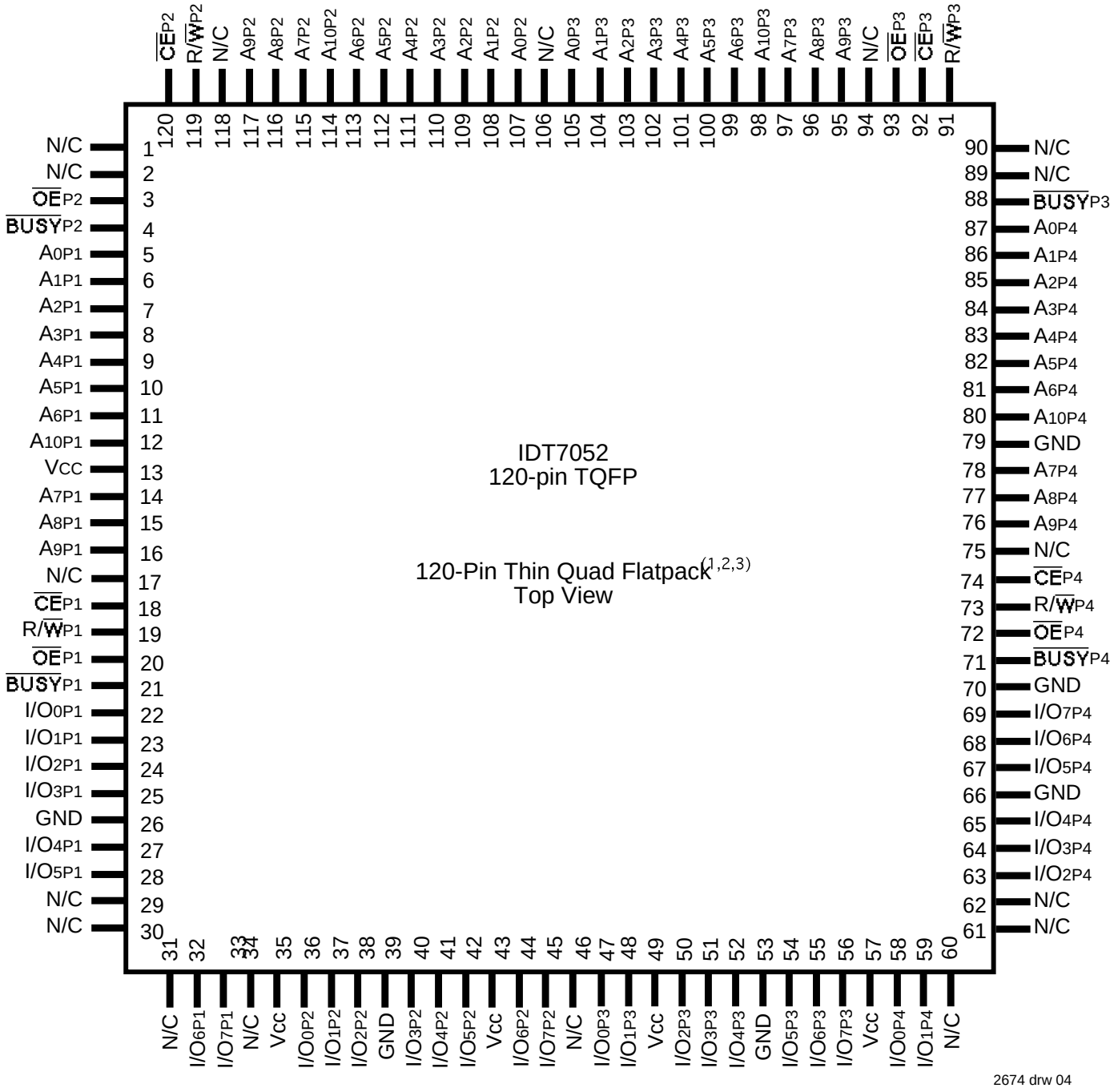
NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONT'D.)



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONT'D.)



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NOTES:
1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS[1,2]

Symbol	Pin Name
A_0 P1 – A_{10} P1	Address Lines – Port 1
A_0 P2 – A_{10} P2	Address Lines – Port 2
A_0 P3 – A_{10} P3	Address Lines – Port 3
A_0 P4 – A_{10} P4	Address Lines – Port 4
I/O_0 P1 – I/O_7 P1	Data I/O – Port 1
I/O_0 P2 – I/O_7 P2	Data I/O – Port 2
I/O_0 P3 – I/O_7 P3	Data I/O – Port 3
I/O_0 P4 – I/O_7 P4	Data I/O – Port 4
R/$\overline{W}$ P1	Read/Write – Port 1
R/$\overline{W}$ P2	Read/Write – Port 2
R/$\overline{W}$ P3	Read/Write – Port 3
R/$\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
V_{CC}	Power

NOTES: 2674 tbl 01
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2674 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 0.5V.

CAPACITANCE (TQFP Package Only)

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2674 tbl 03
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2674 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2674 tbl 05
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1, 5) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Condition	Version		IDT7052X15 COM'L. ONLY Typ.(2)	IDT7052X15 COM'L. ONLY Max.	IDT7052X20 Typ.(2)	IDT7052X20 Max.	Unit
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = 0(4)	MIL.	S	150	400	150	380	mA
				L	150	340	150	320	
			COM'L.	S	150	340	150	320	
				L	150	290	150	270	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}(5)	MIL.	S	240	420	230	410	mA
				L	210	360	200	350	
			COM'L.	S	260	390	240	370	
				L	230	345	210	325	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE}$ = V_{IH}, f = f_{MAX}(5)	MIL.	S	90	135	80	125	mA
				L	80	105	70	115	
			COM'L.	S	80	105	70	95	
			L		70	90	60	80	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports, $\overline{CE}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0(4)	MIL.	S	1.5	30	1.5	30	mA
				L	.3	4.5	.3	4.5	
			COM'L.	S	1.5	1.5	1.5	1.5	
				L	.3	.3	.3	.3	

Symbol	Parameter	Condition	Version		IDT7052X25 Typ.(2)	IDT7052X25 Max.	IDT7052X35 Typ.(2)	IDT7052X35 Max.	IDT7052X45 Typ.(2)	IDT7052X45 Max.	Unit
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = 0(4)	MIL.	S	150	315	150	360	150	360	mA
				L	150	310	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	
				L	150	250	150	250	150	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}(5)	MIL.	S	225	400	210	395	195	390	mA
				L	190	340	180	330	170	325	
			COM'L.	S	225	350	210	335	195	330	
				L	195	305	180	290	170	285	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE}$ = V_{IH}, f = f_{MAX}(5)	MIL.	S	45	115	40	110	35	105	mA
				L	40	85	35	80	30	75	
			COM'L.	S	60	85	40	75	35	70	
				L	50	70	35	60	30	55	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports, $\overline{CE}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0(4)	MIL.	S	1.5	30	1.5	30	1.5	30	mA
				L	.3	4.5	.3	4.5	.3	4.5	
			COM'L.	S	1.5	1.5	1.5	1.5	1.5	1.5	
				L	.3	1.5	.3	1.5	.3	1.5	

NOTES:

2674 tbl 07

1. "X" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C and are not production tested.
3. f = 0 means no address or control lines change.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. For the case of one port, divide the appropriate current above by four.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7052S		IDT7052L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:
1. At Vcc≤2.0V input leakages are undefined.

2674 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

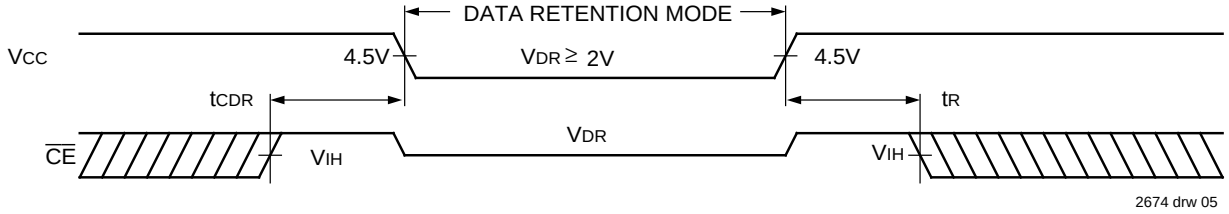
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	MIL.	—	25	1800	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	COM'L.	—	25	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.

2674 tbl 08

LOW V_{CC} DATA RETENTION WAVEFORM



2674 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2674 tbl 09

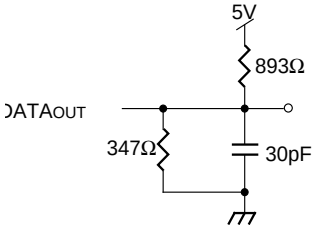
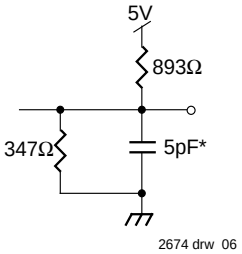


Figure 1. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})



2674 drw 06

Figure 2. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(3)

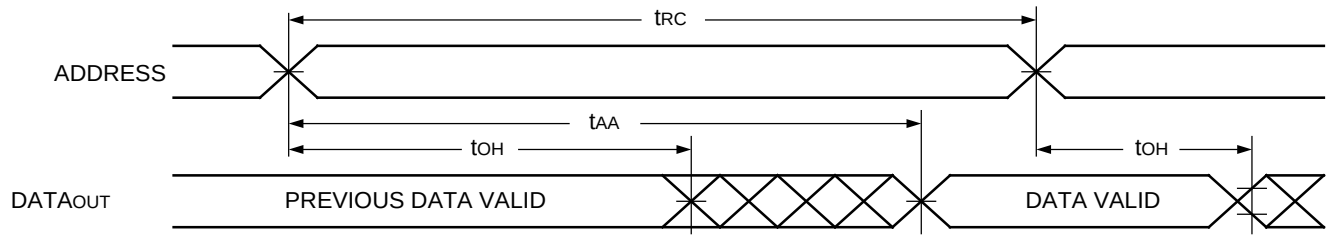
Symbol	Parameter	IDT7052X15 COM'L. ONLY Min.	IDT7052X15 COM'L. ONLY Max.	IDT7052X20 Min.	IDT7052X20 Max.	Unit
READ CYCLE						
t_{RC}	Read Cycle Time	15	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	20	ns
t_{ACE}	Chip Enable Access Time	—	15	—	20	ns
t_{AOE}	Output Enable Access Time	—	8	—	10	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	ns
t_{LZ}	Output Low-Z Time(1, 2)	5	—	5	—	ns
t_{HZ}	Output High-Z Time(1, 2)	—	12	—	12	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	15	—	20	ns

Symbol	Parameter	IDT7052X25 Min.	IDT7052X25 Max.	IDT7052X35 Min.	IDT7052X35 Max.	IDT7052X45 Min.	IDT7052X45 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	45	ns
t_{ACE}	Chip Enable Access Time	—	25	—	35	—	45	ns
t_{AOE}	Output Enable Access Time	—	15	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time(1, 2)	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time(1, 2)	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	25	—	35	—	45	ns

NOTES: 2674 tbl 10

1. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figures 1 and 2).
2. This parameter is guaranteed but is not production tested.
3. "X" in part number indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1)

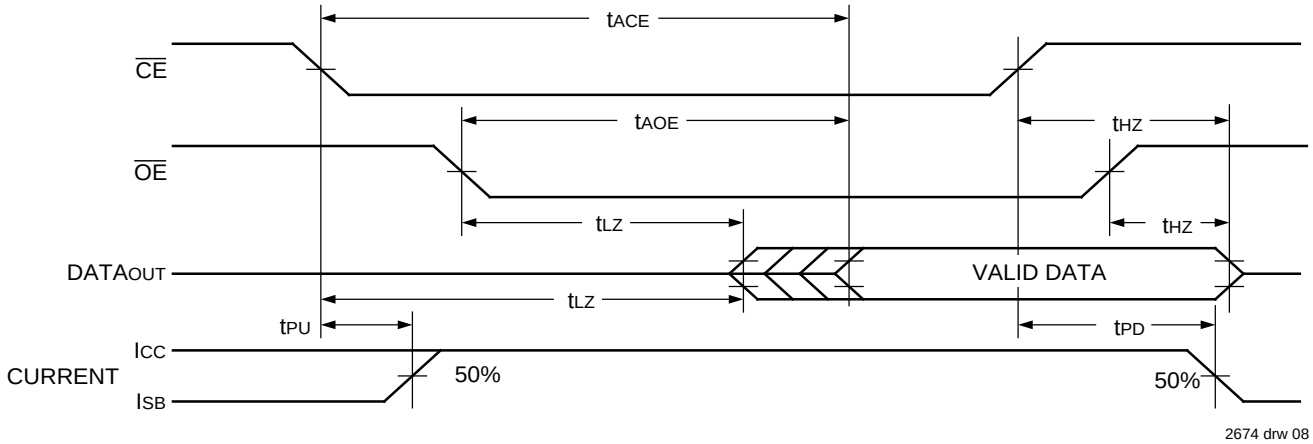


2674 drw 07

NOTE:

1. R/$\overline{W}$ = V_{IH}, $\overline{OE}$ = V_{IL}, and $\overline{CC}$ = V_{IL}.

TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 3)



2674 drw 08

NOTES:
1. R/$\overline{W}$ = V_{IH} for Read Cycles.
2. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7052X15 COM'L. ONLY Min.	IDT7052X15 COM'L. ONLY Max.	IDT7052X20 Min.	IDT7052X20 Max.	Unit
WRITE CYCLE						
tWC	Write Cycle Time	15	—	20	—	ns
tEW	Chip Enable to End-of-Write	12	—	15	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width(3)	12	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	12	—	15	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	ns
tDH	Data Hold Time	0	—	0	—	ns
tWZ	Write Enabled to Output in High-Z(1, 2)	—	12	—	12	ns
tOW	Output Active from End-of-Write(1, 2)	0	—	0	—	ns
tWDD	Write Pulse to Data Delay(4)	—	25	—	35	ns
tDDD	Write Data Valid to Read Data Delay(4)	—	20	—	30	ns
BUSY INPUT TIMING						
tWB	Write to $\overline{BUSY}$(5)	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(6)	12	—	15	—	ns

NOTES:
2674 tbl 11

1. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed but is not production tested.
3. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .Specified for $\overline{OE}$ at high (refer to “Timing Waveform of Write Cycle”, Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write with Port-to-Port Read”.
5. To ensure that the write cycle is inhibited on port "A" during contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
6. To ensure that a write cycle is completed on port "A" after contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
7. "X" in part number indicates power rating.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7052X25		IDT7052X35		IDT7052X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	35	—	45	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	30	—	35	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width[3]	20	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	20	—	20	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High-Z[1, 2]	—	15	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write[1, 2]	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	45	—	55	—	65	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	35	—	45	—	55	ns
BUSY INPUT TIMING								
t_{WB}	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[6]	15	—	20	—	20	—	ns

NOTES:

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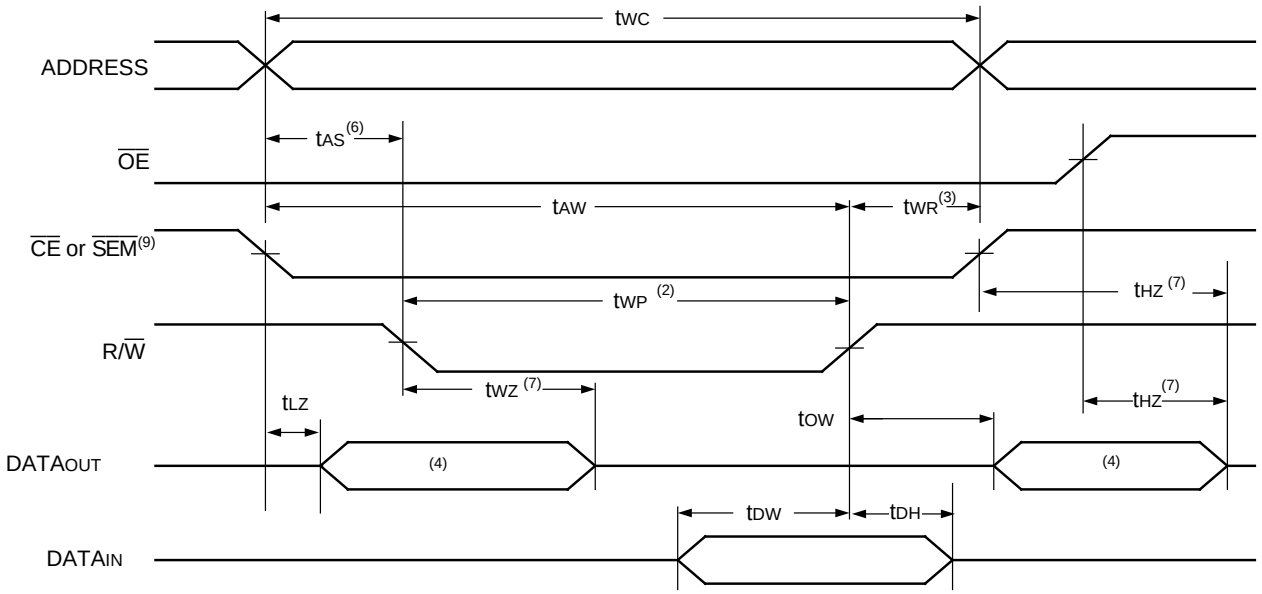
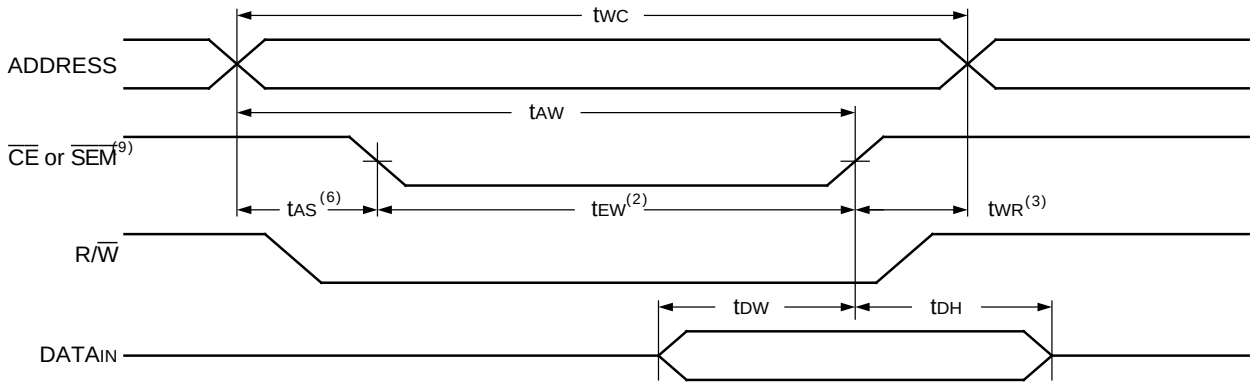
1. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed but is not production tested.
3. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .Specified for $\overline{OE}$ at high (refer to “Timing Waveform of Write Cycle”, Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write with Port-to-Port Read”.
5. To ensure that the write cycle is inhibited on port "A" during contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
6. To ensure that a write cycle is completed on port "A" after contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
7. "X" in part number indicates power rating.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(5,8)



2674 drw 09

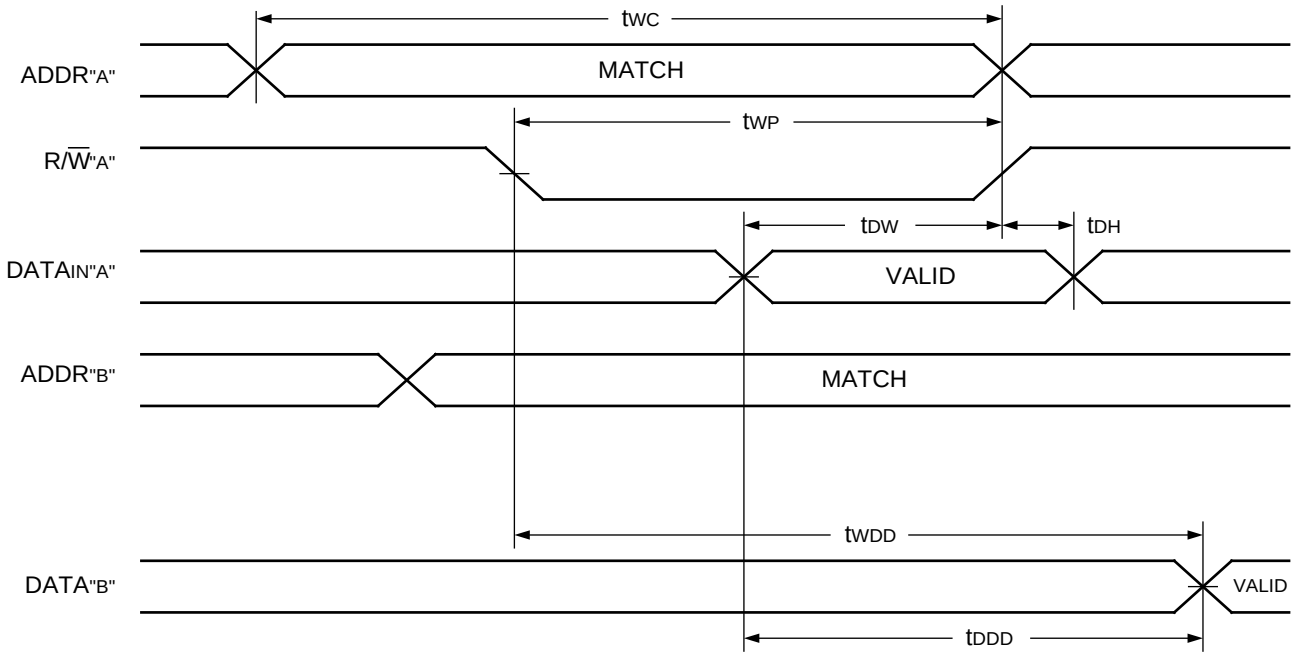
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 5)



2674 drw 10

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figure 2).This parameter is guaranteed but is not production tested.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition.

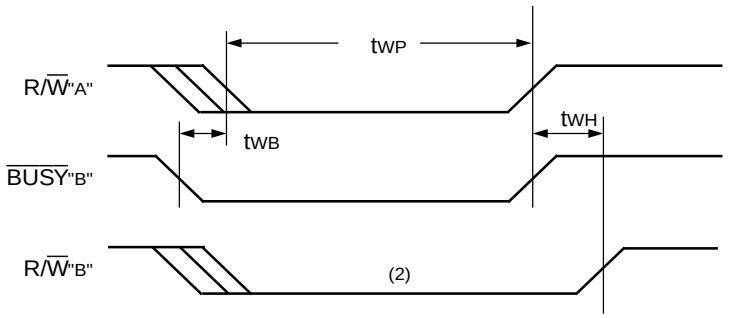
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ(1, 2, 3)



2674 drw 11

NOTES:
1. Assume $\overline{BUSY}$ input = V_{IH} and $\overline{CE}$ = V_{IL} for the writing port.
2. $\overline{OE}$ = V_{IL} for the reading ports.
3. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2674 drw 12

NOTES:
1. $\overline{BUSY}$ is aserted on Port "B" blocking R/$\overline{W}$"B" until $\overline{BUSY}$ "B" goes HIGH.

FUNCTIONAL DESCRIPTION

The IDT7052 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

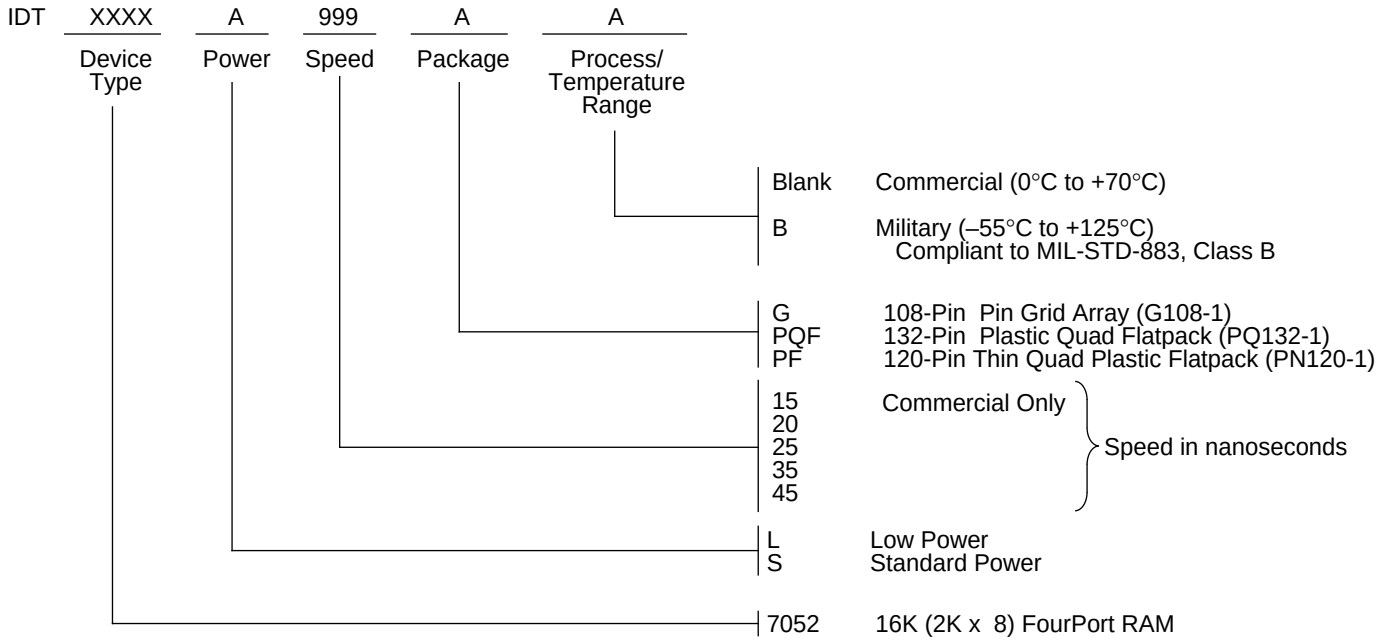
TABLE I – READ/WRITE CONTROL

Any Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{CE}_{P1}$ = $\overline{CE}_{P2}$ = $\overline{CE}_{P3}$ = $\overline{CE}_{P4}$ =V_{IH} Power Down Mode, I_{SB} or I_{SB1}
L	L	X	$DATA_{IN}$	Data on port written into memory(2, 3)
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	Outputs Disabled

2698 tbl 12

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care, "Z "= High Impedance
2. If $\overline{BUSY}$ = V_{IL}, write is blocked.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION



2674 drw 13A