Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) STRAM

IDT10496RL
IDT100496RL
IDT101496RL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with registers on inputs and latches on outputs
- Balanced Read/Write cycle time: 10/12/15 ns
- Access time: 10/12/15 ns (max.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

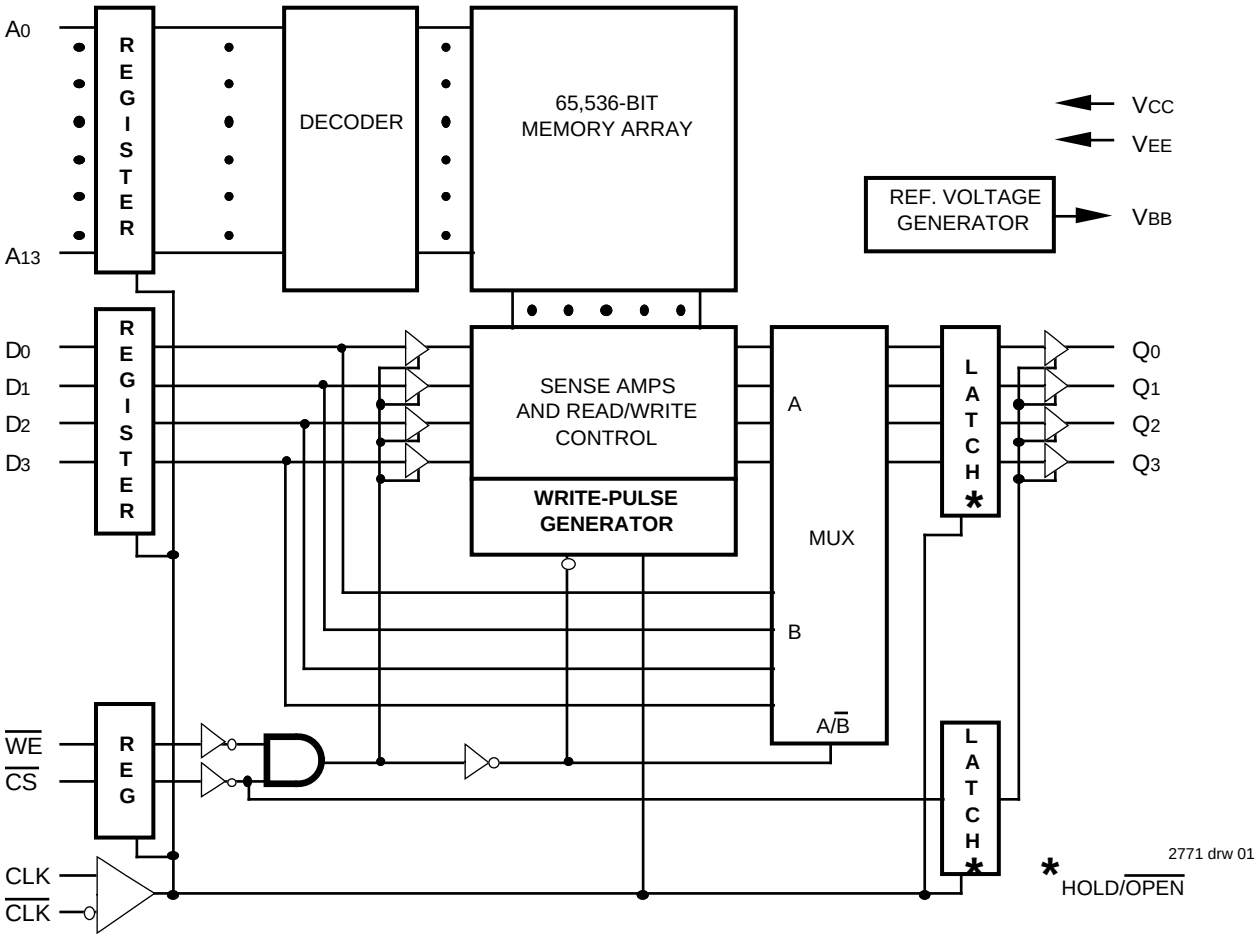
DESCRIPTION:

The IDT10496RL, IDT100496RL and IDT101496RL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs are captured by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

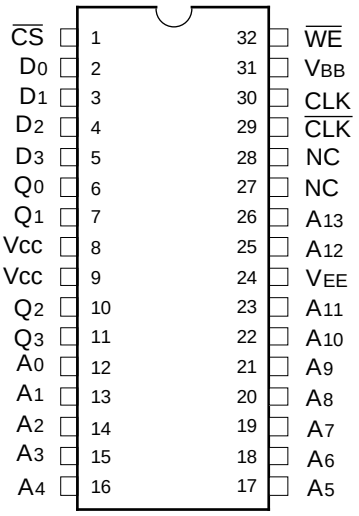
Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



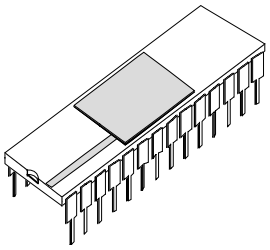
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



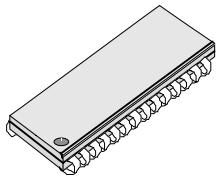
2771 drw 02

TOP VIEW



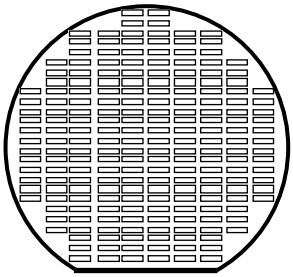
400-Mil-Wde CERAMIC PACKAGE C32-2

2771 drw 03



300-Mil-Wide PLASTIC SOJ PACKAGE SO32-2

2771 drw 04



Hi-Rel Die For Hybrid and MCM Applications

2771 drw 05

PIN DESCRIPTION

Symbol	Pin Name
A_0 through A_{13}	Address Inputs
D_0 through D_3	Data Inputs
Q_0 through Q_3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
V_{BB}	Reference Voltage Output (≈1.32V)
V_{EE}	More Negative Supply Voltage
V_{CC}	Less Negative Supply Voltage
NC	No Connect - not internally bonded

CAPACITANCE (T_A=+25°C, f=1.0MHz)

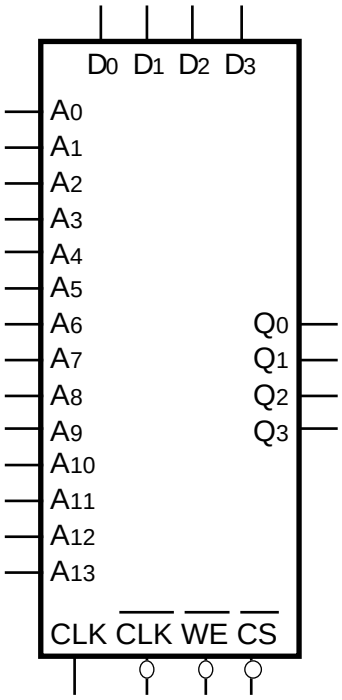
		DIP		SOJ		
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Unit
C_{INCLK}	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
C_{IN}	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
C_{OUT}	Output Capacitance	6	–	3	–	pF

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	Data$_{OUT}$(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATA$_{OUT}$ initiated by falling edge of CLK.

LOGIC SYMBOL



16Kx4 STRAM

2771 drw 05

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature	10K 100K 101K	0 to +75 0 to +85 0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperatuure	Ceramic Plastic	-65 to +150 -55 to +125	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2760 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC ELECTRICAL OPERATING RANGES

I/O	V_{EE}	T_A
10K	-5.2V ± 5%	0 to +75°C, air flow exceeding 2 m/sec
100K	-4.5V ± 5%	0 to +85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 to +75°C, air flow exceeding 2 m/sec

2760 tbl 05

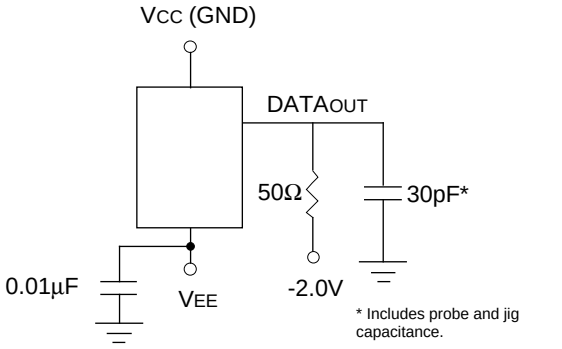
DC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter		10K Min.	10K Max.	10K TA	100K/101K Min.	100K/101K Max.	Unit
V_{OH}	Output HIGH Voltage (V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$)		-1000 -960 -900	-840 -810 -720	0°C 25°C 75°C	-1025	-880	mV
V_{OL}	Output LOW Voltage (V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$)		-1870 -1850 -1830	-1665 -1650 -1625	0°C 25°C 75°C	-1810	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage (V_{IN}= $V_{IH(Min)}$ or $V_{IL(Max)}$)		-1020 -980 -920	— — —	0°C 25°C 75°C	-1035	—	mV
V_{OLC}	Output Threshold LOW Voltage (V_{IN}= $V_{IH(Min)}$ or $V_{IL(Max)}$)		— — —	-1645 -1630 -1605	0°C 25°C 75°C	—	-1610	mV
V_{IH}	Input HIGH Voltage (Guaranteed Input Voltage High for All Inputs)		-1145 -1105 -1045	-840 -810 -720	0°C 25°C 75°C	-1165	-880	mV
V_{IL}	Input LOW Voltage (Guaranteed Input Voltage Low for All Inputs)		-1870 -1850 -1830	-1490 -1475 -1450	0°C 25°C 75°C	-1810	-1475	mV
I_{IH}	Input HIGH Current							
	V_{IN}= $V_{IH(Max)}$	CS Others	— —	220 110	— —	— —	220 110	µA µA
I_{IL}	Input LOW Current							
	V_{IN}= $V_{IL(Min)}$	CS Others	0.5 -50	170 90	— —	0.5 -50	170 90	µA µA
I_{EE}	Supply Current		-260	—	—	-240 (100K) -260 (101K)	— —	mA

NOTE:
1. RL = 50Ω to -2V, air flow exceeding 2 m/sec.

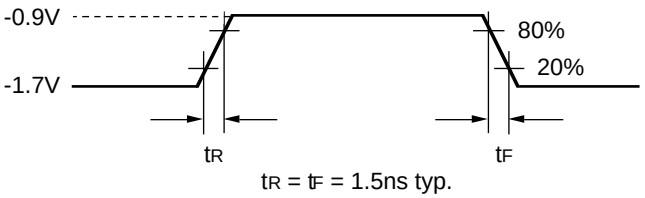
2760 tbl 05

AC TEST LOAD CONDITION



2771 drw 07

AC TEST INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

2771 drw 08

RISE/FALL TIME

Symbol	Parameter	Min.	Typ.	Max.	Unit
tR	Output Rise Time	—	1.5	—	ns
tF	Output Fall Time	—	1.5	—	ns

2771 tbl 06

FUNCTIONAL DESCRIPTION

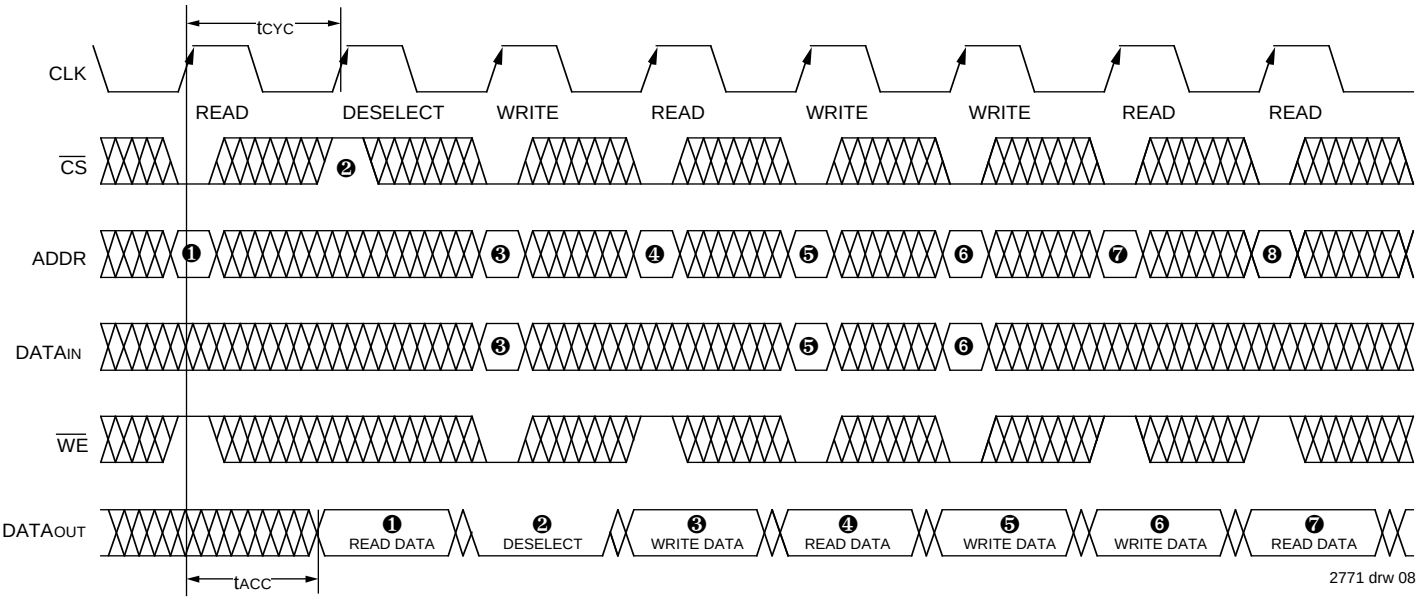
The IDT10496RL, IDT100496RL and IDT101496RL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses, input data, and control status. Inputs are sampled on the rising edge of the clock (CLK) input (falling edge of CLK). In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Output data flows out the output latch and is held into the next cycle.

READ TIMING

In a typical read cycle, the read address is captured by the rising edge of clock, as at ❶ below. Then, when clock goes low, the read data for the read address clocked in at ❶ is gated through the output latch to the output pins. There is a short delay from falling clock to output ready, called tDR (see Read Cycle Timing). If the clock-high time (tWH) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified tACC. But if tWH is longer than the cell access-time, output data will be valid tDR after clock goes low. Thus, the time it takes from clock-to-output for any given

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



2771 drw 08

address (the latency, or t_{ACC}) is

$$t_{ACC} = t_{ACC} \text{ or } (t_{WH} + t_{DR}),$$

whichever is larger.

The output latch takes some time to change state for the next cycle, but this time is very short. Therefore, data hold time from clock low (t_{DH}) is specified as zero minimum hold time.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) at rising edge of clock. This case occurs at ❷ below. Outputs then attain the disable state (low) t_{ACC} later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses the clock-high time as the write pulse, and thus determines the minimum clock-high time, t_{WH}.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins in the appropriate time slot (i.e. after $t_{WH} + t_{DR}$). This function is sometimes called “Transparent Write,” and is useful for write-through cache applications. Thus the input data sampled at ❸ is available on the output at the end of the cycle.

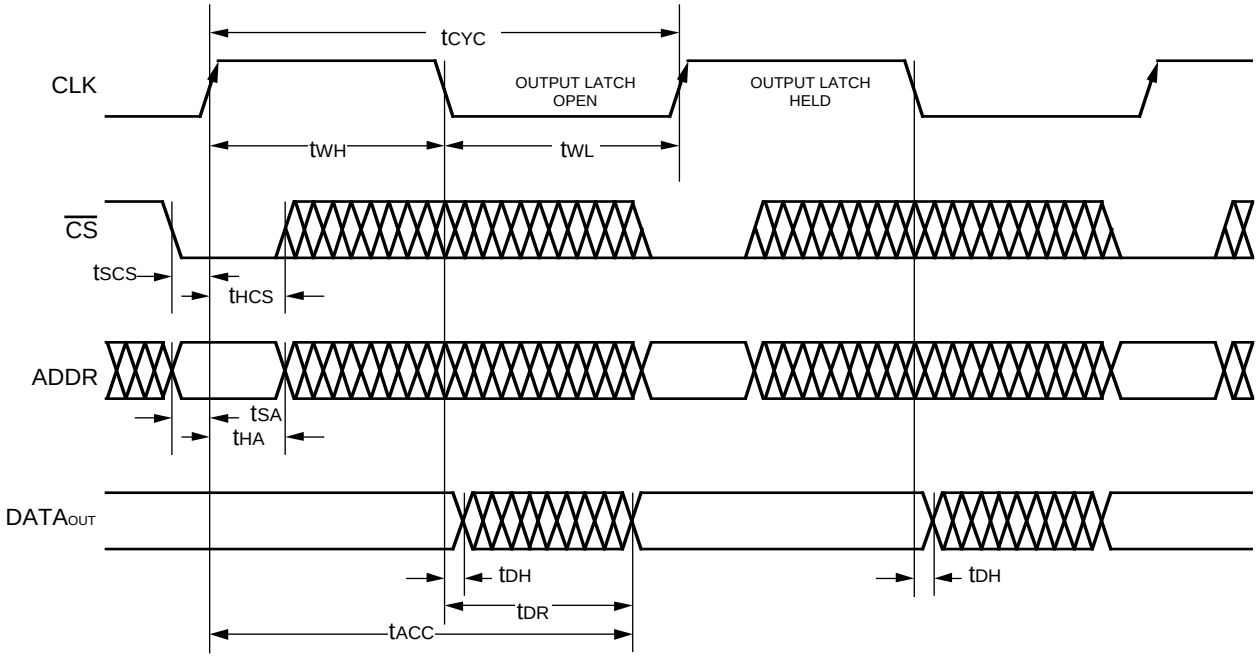
There are no restrictions on the order of read cycles and write cycles.

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
t_{CYC}	Cycle Time	–	10	–	12	–	15	–	ns
t_{ACC}[2]	Access Time from Clock High	–	–	10	–	12	–	15	ns
t_{WL}	Clock Low Pulse Width	–	5	–	5	–	6	–	ns
t_{WH}	Clock High Pulse Width	–	5	–	5	–	6	–	ns
t_{SCS}	Setup Time for Chip Select	–	1	–	1	–	1	–	ns
t_{SA}	Setup Time for Address	–	1	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2.5	–	2.5	–	2.5	–	ns
t_{HA}	Hold Time for Address	–	2.5	–	2.5	–	2.5	–	ns
t_{DH}	Data Hold from Clock Low	–	2	–	2	–	2	–	ns
t_{DR}	Data Ready from Clock Low	–	2	5	2	5	2	5	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of t_{ACC} or $t_{WH} + t_{DR}$.

READ CYCLE TIMING DIAGRAM



2771 drw 09

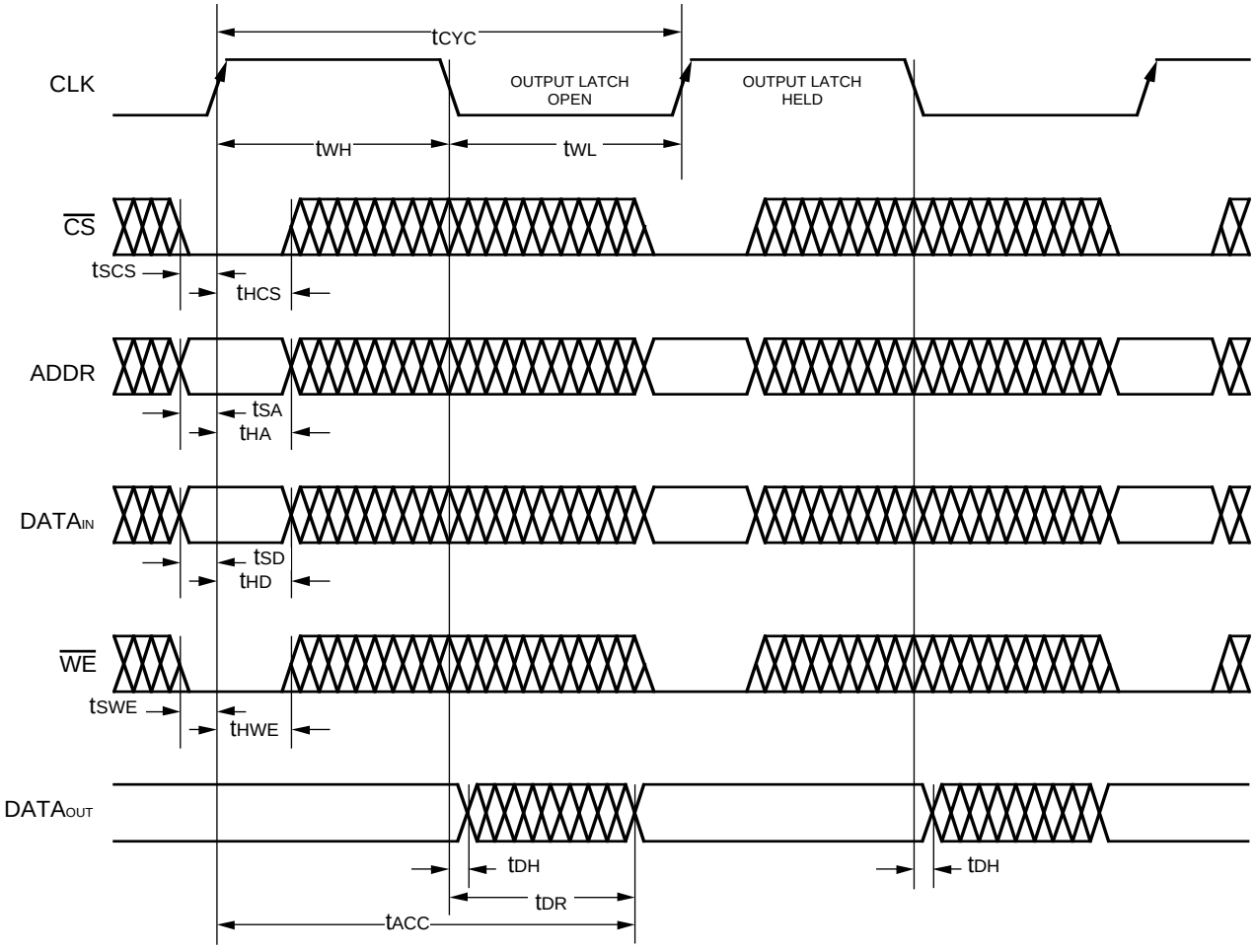
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle[2]									
t_{SWE}	Setup Time for Write Enable	–	1	–	1	–	1	–	ns
t_{SD}	Setup Time for Data In	–	1	–	1	–	1	–	ns
t_{HWE}	Hold Time for Write Enable	–	2.5	–	2.5	–	2.5	–	ns
t_{HD}	Hold Time for Data In	–	2.5	–	2.5	–	2.5	–	ns

2771 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements. Write Data appears on output pins after falling edge of clock.

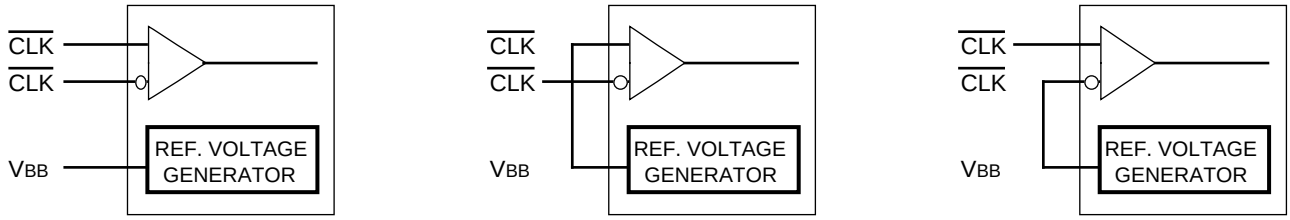
WRITE CYCLE TIMING DIAGRAM



2771 drw 10

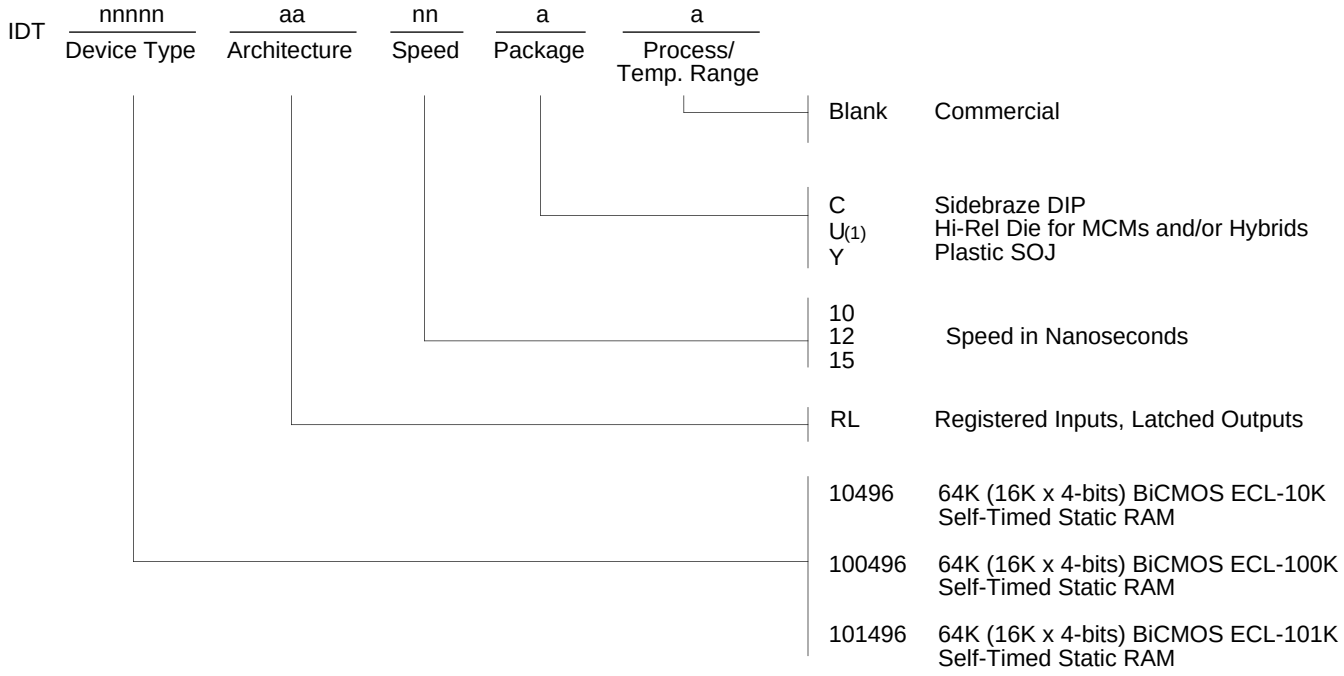
CLOCK INPUT

The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. V_{BB} is designed to drive clock input only and is not intended to be used for any other purpose.



(a) Differential Mode **(b) Falling-Edge-Active Single-Ended Mode** **(c) Rising-Edge-Active Single-Ended Mode**

2771 drw 11



2771 drw 12

NOTE:
1. Please contact your IDT Sales Representative for more information on specifications and availability of Die products.