



Integrated Device Technology, Inc.

32K x 36 CacheRAM™

3.3V SYNCHRONOUS BURST SRAM WITH PIPELINED OUTPUT

PRELIMINARY
IDT71V536
FEATURES:

- 32K x 36 memory configuration
- Supports high performance system speed - 120 MHz (5.0ns Clock-to-Data Access).
- LBO input selects interleaved or linear burst mode
- Self-timed write cycle with global write control (\overline{GW}), byte write enable (\overline{BWE}), and byte writes (\overline{BWx})
- Power down controlled by ZZ input
- Single 3.3V power supply (+10/-5%)
- Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)

DESCRIPTION:

The IDT71V536 is a 3.3V high-speed 1,179,648-bit CacheRAM organized as 32K x 36 with full support of the Pentium™ and PowerPC™ processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 120MHz.

The IDT71V536 CacheRAM contains write, data, address,

and control registers. Internal logic allows the CacheRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V536 can provide four cycles of data for a single address presented to the CacheRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}=LOW$), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the LBO input pin.

The IDT71V536 CacheRAM utilizes IDT's high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

PIN DESCRIPTION SUMMARY

A0 – A14	Address Inputs	Input	Synchronous
\overline{CE}	Chip Enable	Input	Synchronous
CS0, CS1	Chips Selects	Input	Synchronous
\overline{OE}	Output Enable	Input	Asynchronous
\overline{GW}	Global Write Enable	Input	Synchronous
\overline{BWE}	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$ - $\overline{BW_4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock Input	Input	N/A
\overline{ADV}	Burst Address Advance	Input	Synchronous
\overline{ADSC}	Address Status (Cache Controller)	Input	Synchronous
\overline{ADSP}	Address Status (Processor)	Input	Synchronous
LBO	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O0-I/O31	Data Input/Output	I/O	Synchronous
I/OP1-I/OP4	Data Input/Output (Parity)	I/O	Synchronous
VDD, VDDQ	3.3V Array, 3.3V I/O Power Supply	Power	N/A
VSS, VSSQ	Array Ground, I/O Ground	Power	N/A

3519 tbl 01

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 Pentium is a trademark of Intel Corp.
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COMMERCIAL TEMPERATURE RANGE**MAY 1996**

PIN DEFINITIONS⁽¹⁾

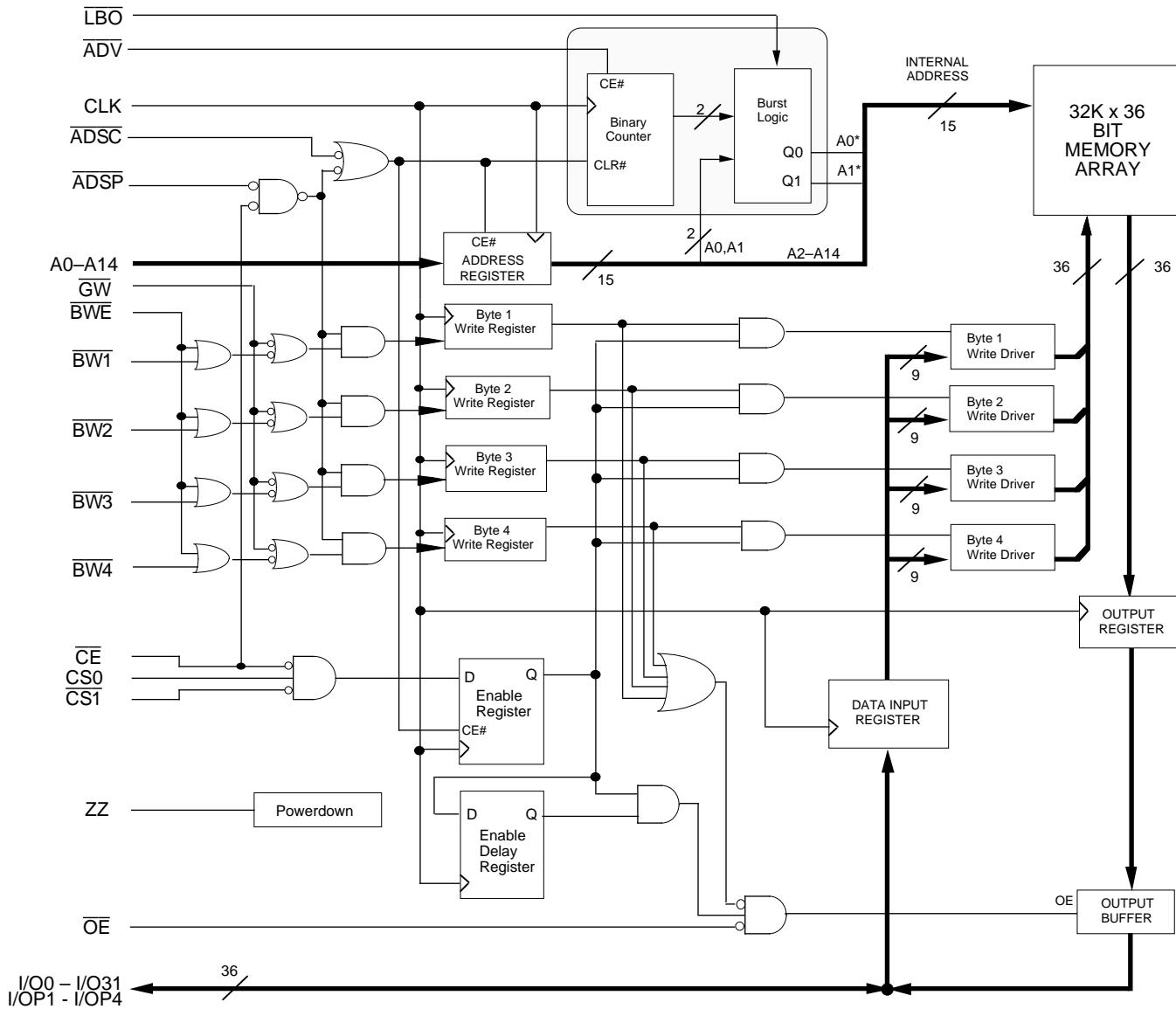
Symbol	Pin Function	I/O	Active	Description
A0-A14	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and ADSC Low or ADSP Low and CE Low.
ADSC	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. ADSC is an active LOW input that is used to load the address registers with new addresses. ADSC is NOT GATED by CE.
ADSP	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. ADSP is an active LOW input that is used to load the address registers with new addresses. ADSP is gated by CE.
ADV	Burst Address Advance	I	LOW	Synchronous Address Advance. ADV is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance.
BWE	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs BW1-BW4. If BWE is LOW at the rising edge of CLK then BWx inputs are passed to the next stage in the circuit. A byte write can still be blocked if ADSP is LOW at the rising edge of CLK. If ADSP is HIGH and BWx is LOW at the rising edge of CLK then data will be written to the SRAM. If BWE is HIGH then the byte write inputs are blocked and only GW can initiate a write cycle.
BW1-BW4	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active LOW byte write. Any active byte write causes all outputs to be disabled. ADSP LOW disables all byte writes. BW1-BW4 must meet specified setup and hold times with respect to CLK.
CE	Chip Enable	I	LOW	Synchronous chip enable. CE is used with CS0 and CS1 to enable the IDT71V536. CE also gates ADSP.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS0 is used with CE and CS1 to enable the chip.
CS1	Chip Select 1	I	LOW	Synchronous active LOW chip select. CS1 is used with CE and CS0 to enable the chip.
GW	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 8-bit data bytes when LOW on the rising edge of CLK. GW superceeds individual byte write enables.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
LBO	Linear Burst Order	I	LOW	Asynchronous burst order selection DC input. When LBO is HIGH the Interleaved (Intel) burst sequence is selected. When LBO is LOW the Linear (PowerPC) burst sequence is selected. LBO is a static DC input and must not change state while the device is operating. LBO has an internal pull-up resistor.
OE	Output Enable	I	LOW	Asynchronous output enable. When OE is HIGH the I/O pins are in a high-impedance state. When OE is LOW the data output drivers are enabled if the chip is also selected.
VDD	Power Supply	N/A	N/A	3.3V core power supply inputs.
VDDQ	Power Supply	N/A	N/A	3.3V I/O power supply inputs.
VSS	Ground	N/A	N/A	Core ground pins.
VSSQ	Ground	N/A	N/A	I/O ground pins.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the chip.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V536 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. ZZ has an internal pull-down resistor.

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

3519 tbl 02

FUNCTIONAL BLOCK DIAGRAM



3519 drw 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	VDD
Commercial	0°C to +70°C	3.3V+10/-5%

3519 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

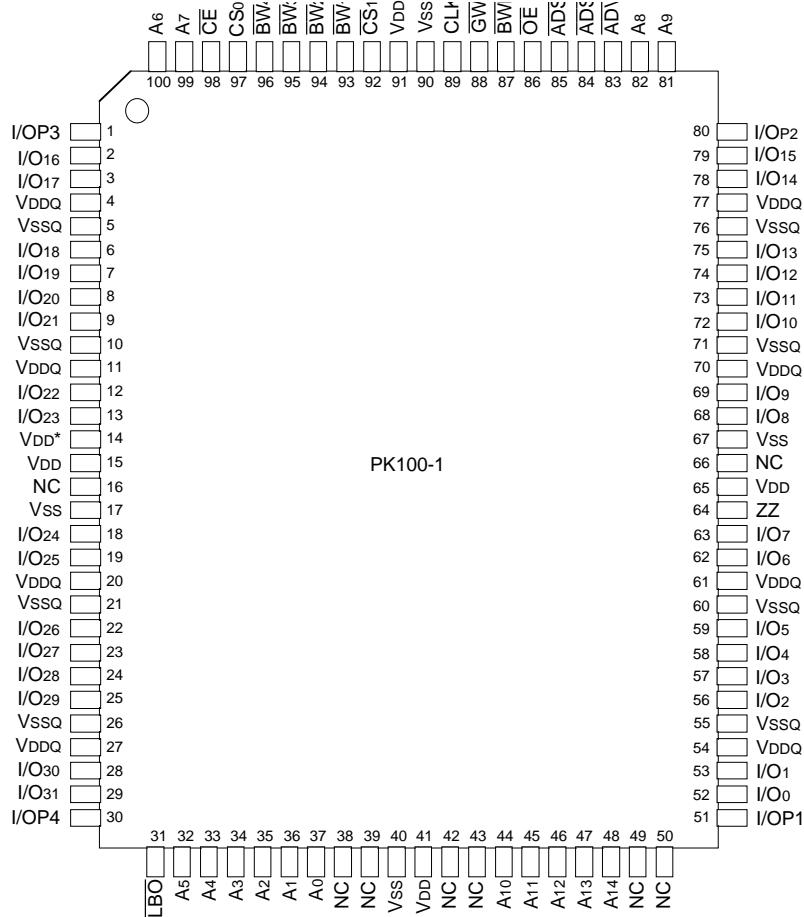
Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD, VDDQ	Supply Voltage	3.135	3.3	3.63	V
VIH	Input High Voltage	2.0	—	VDD+0.3	V
VIL	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

NOTE:

3519 tbl 04

1. VIL (min)= -1.0V for pulse width less than tcyc/ 2, once per cycle.

PIN CONFIGURATION



* Pin 14 does not have to be directly connected to VDD as long as the input voltage is $\geq VIH$.

TOP VIEW TQFP

3519 drw 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VDDQ +0.5	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.2	W
IOUT	DC Output Current	50	mA

NOTES:

3519 tbl 05

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD}, V_{DDQ} and input terminals only.
- I/O terminals.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	4	pF
C _{OUT}	output Capacitance	V _{OUT} = 3dV	8	pF

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

SYNCHRONOUS TRUTH TABLE^(1, 2)

Operation	Address Used	\overline{CE}	CS_0	\overline{CS}_1	$ADSP$	$ADSC$	ADV	GW	BWE	BWx	$\overline{OE}^{(3)}$	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L	L	↑	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	X	X	↑	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	X	X	↑	DIN

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.

2. ZZ = LOW for this table.

3. OE is an asynchronous input.

3519 tbl 07

SYNCHRONOUS WRITE FUNCTION TRUTH TABLE⁽¹⁾

Operation	\overline{GW}	\overline{BWE}	\overline{BW}_1	\overline{BW}_2	\overline{BW}_3	\overline{BW}_4
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 ⁽²⁾	H	L	L	H	H	H
Write Byte 2 ⁽²⁾	H	L	H	L	H	H
Write Byte 3 ⁽²⁾	H	L	H	H	L	H
Write Byte 4 ⁽²⁾	H	L	H	H	H	L

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
 2. Multiple bytes may be selected during the same cycle.

3519 tbl 08

ASYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation ⁽²⁾	\overline{OE}	ZZ	I/O Status	Power
Read	L	L	Data Out (I/O ₀ – I/O ₃₁)	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z — Data In (I/O ₀ – I/O ₃₁)	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
 2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

3519 tbl 09

INTERLEAVED BURST SEQUENCE TABLE ($\overline{LBO}=V_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

NOTE:

1. Upon completion of the burst sequence the counter wraps around to its initial state.

3519 tbl 10

LINEAR BURST SEQUENCE TABLE ($\overline{LBO}=V_{SS}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

3519 tbl 11

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ($V_{DD} = 3.3V \pm 10/-5\%$)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$ I_{IL} $	Input Leakage Current	$V_{DD} = \text{Max.}$, $V_{IN} = 0V$ to V_{DD}	—	5	μA
$ I_{IL} $	ZZ & \overline{LBO} Input Leakage Current ⁽¹⁾	$V_{DD} = \text{Max.}$, $V_{IN} = 0V$ to V_{DD}	—	30	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$, $V_{OUT} = 0V$ to V_{DD} , $V_{DD} = \text{Max.}$	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = 5mA$, $V_{DD} = \text{Min.}$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -5mA$, $V_{DD} = \text{Min.}$	2.4	—	V

NOTE:

1. The ZZ pin has an internal pull-down resistor to VSSQ.
The LBO pin has an internal pull-up resistor to VDDQ.

3519 tbl 12

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽¹⁾ ($V_{DD} = 3.3V \pm 10/-5\%$, $V_{HD} = V_{DD}-0.2V$, $V_{LD} = 0.2V$)

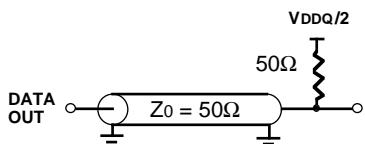
Symbol	Parameter	Test Condition	71V536S5	71V536S6	71V536S7	Unit
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, $V_{DD} = \text{Max.}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, $f = f_{MAX}^{(2)}$	225	210	200	mA
I_{SB}	Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, $f = f_{MAX}^{(2)}$	100	90	80	mA
I_{SB1}	Full Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}$, $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, $f = 0^{(2)}$	10	10	10	mA
I_{ZZ}	Full Sleep Mode Power Supply Current	$ZZ \geq V_{HD}$, $V_{DD} = \text{Max.}$	5	5	5	mA

NOTES:

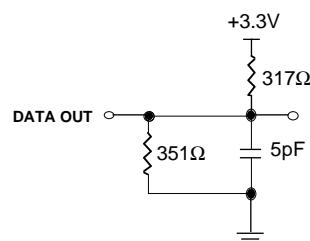
1. All values are maximum guaranteed values.
2. At $f = f_{MAX}$, address inputs are cycling at the maximum frequency of read cycles of $1/t_{Cyc}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input signals are changing.

3519 tbl 13

AC TEST LOADS



3519 drw 03

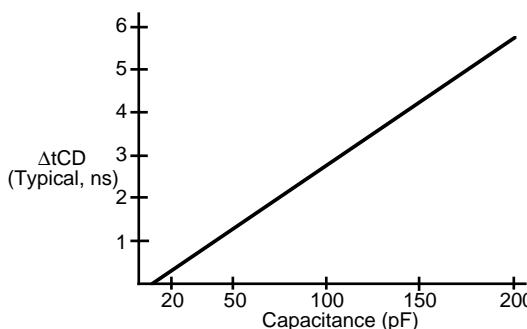


3519 drw 04

Figure 1. AC Test Load

Figure 2. AC Test Load
(for tOHz, tCHz, tolz, and tdc1)

* Including scope and jig



3519 drw 05

Figure 3. Lumped Capacitive Load, Typical Derating

AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3519 tbl 14

AC ELECTRICAL CHARACTERISTICS

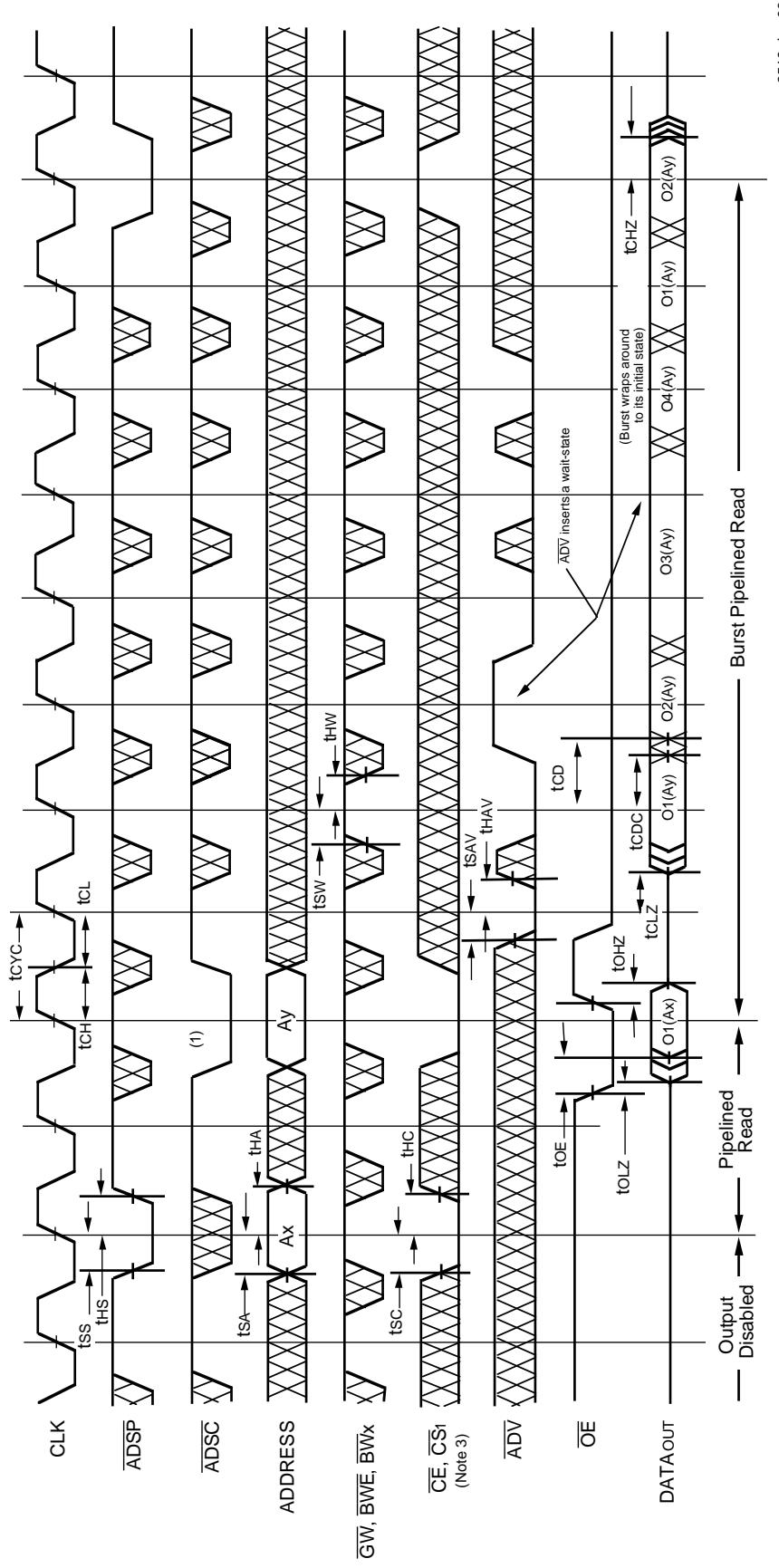
(VDD = 3.3V +10/-5%, TA = 0 to 70°C)

Symbol	Parameter	71V536S5		71V536S6		71V536S7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Parameters								
tCYC	Clock Cycle Time	8.3	—	11	—	13	—	ns
tCH ⁽¹⁾	Clock High Pulse Width	2.5	—	3.7	—	4.5	—	ns
tCL ⁽¹⁾	Clock Low Pulse Width	2.5	—	3.7	—	4.5	—	ns
Output Parameters								
tCD	Clock High to Valid Data	—	5	—	6	—	7	ns
tcDC	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
tCLZ ⁽²⁾	Clock High to Output Active	0	—	0	—	0	—	ns
tCHZ ⁽²⁾	Clock High to Data High-Z	1.5	6	1.5	6	1.5	6	ns
toE	Output Enable Access Time	—	4.8	—	5	—	5	ns
tolZ ⁽²⁾	Output Enable Low to Data Active	0	—	0	—	0	—	ns
toHZ ⁽²⁾	Output Enable High to Data High-Z	—	4.8	—	5	—	5	ns
Set Up Times								
tSA	Address Setup Time	2	—	2	—	2.5	—	ns
tSS	Address Status Setup Time	2	—	2	—	2.5	—	ns
tSD	Data In Setup Time	2	—	2	—	2.5	—	ns
tSW	Write Setup Time	2	—	2	—	2.5	—	ns
tSAV	Address Advance Setup Time	2	—	2	—	2.5	—	ns
tSC	Chip Enable/Select Setup Time	2	—	2	—	2.5	—	ns
Hold Times								
tHA	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
tHS	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
tHD	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
tHW	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
tHAV	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
tHC	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
tZZPW	ZZ Pulse Width	100	—	100	—	100	—	ns
tZZR ⁽³⁾	ZZ Recovery Time	100	—	100	—	100	—	ns
tCFG ⁽⁴⁾	Configuration Set-up Time	40	—	40	—	40	—	ns

NOTES:

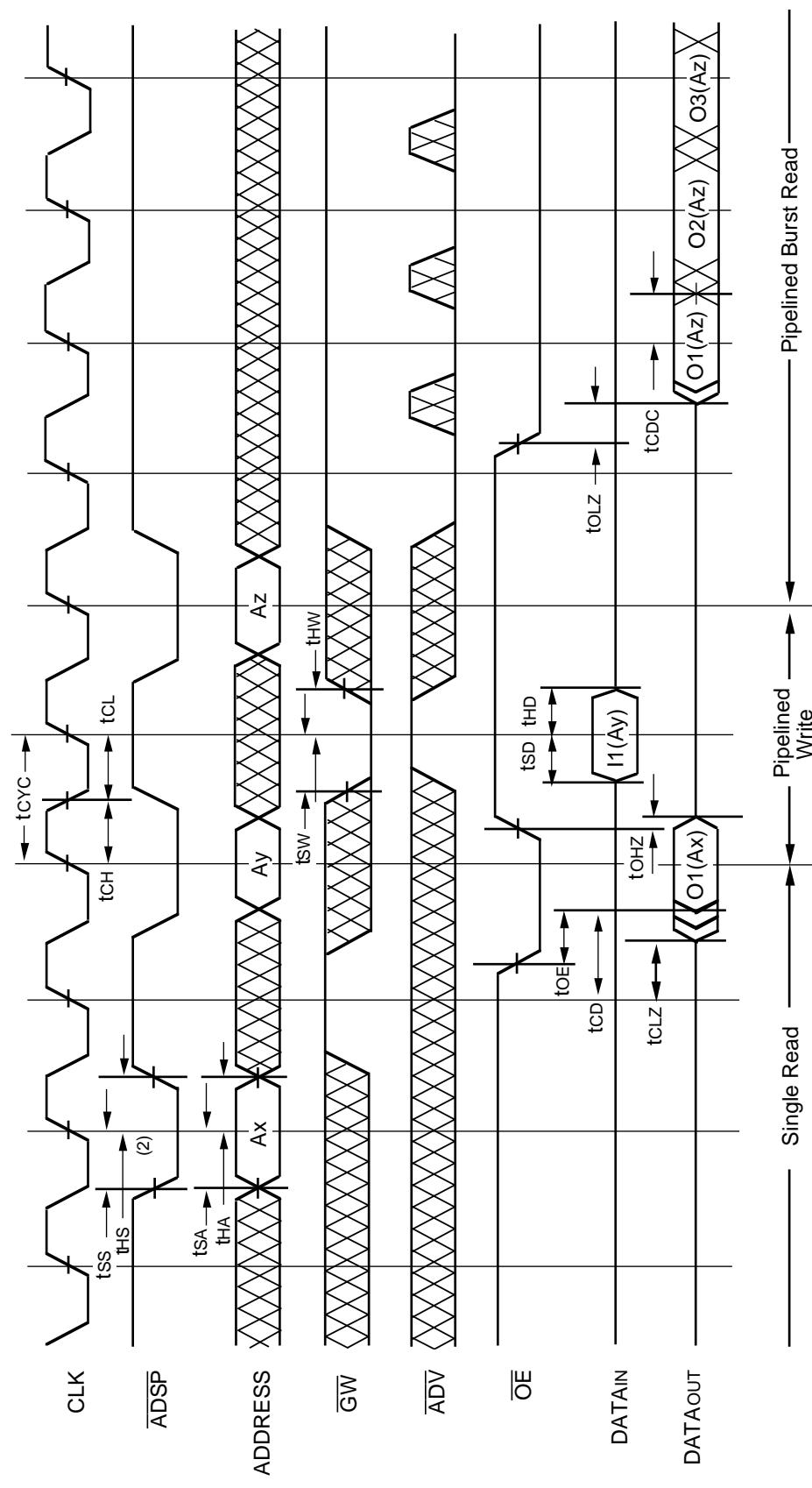
1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured $\pm 200\text{mV}$ from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. tCFG is the minimum time required to configure the device based on the LBO input. LBO is a static input and must not change during normal operation.

3519 tbl 15

TIMING WAVEFORM OF PIPELINED READ CYCLE^(1, 2)**NOTES:**

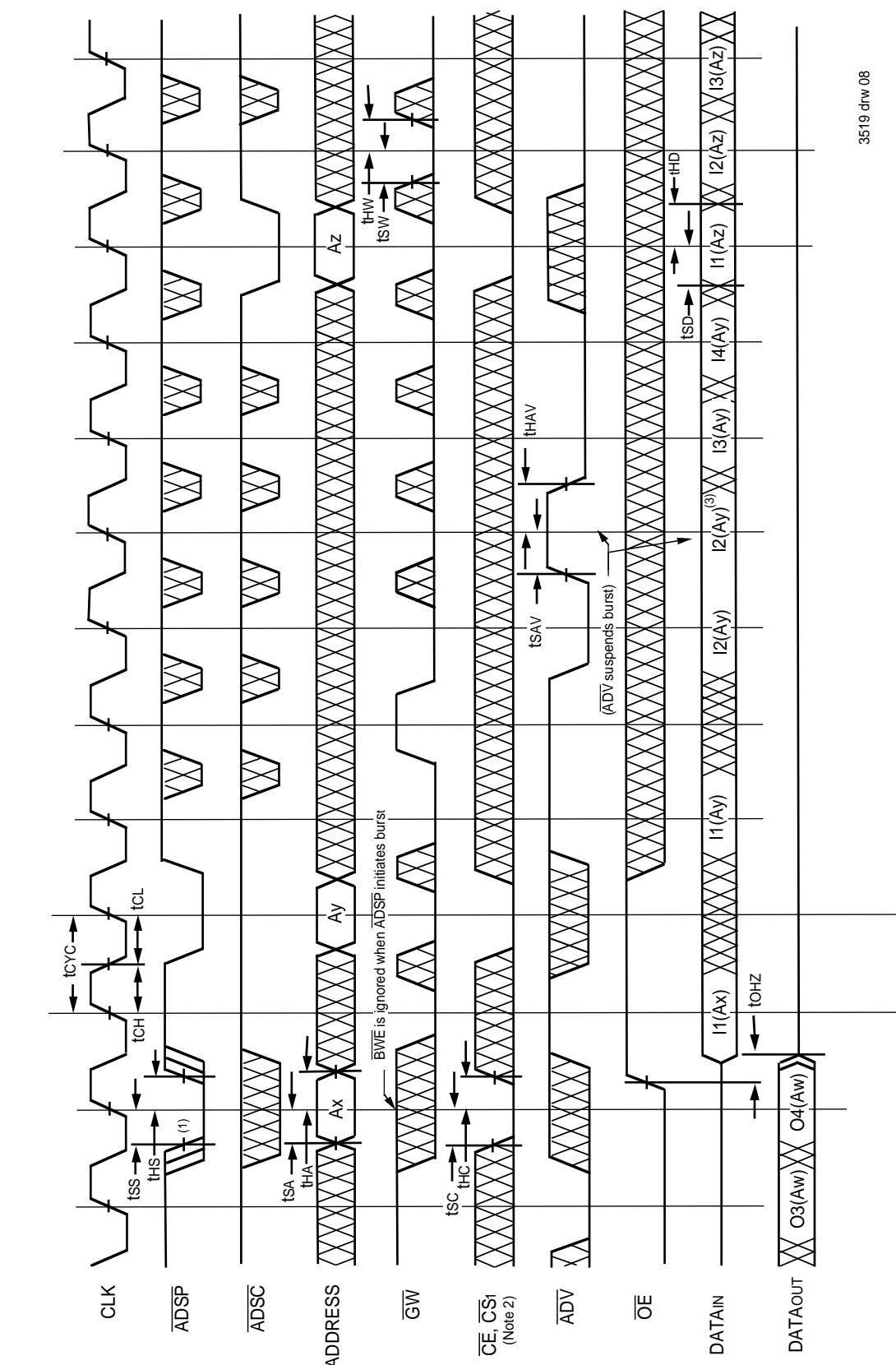
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. ZZ input is LOW and \overline{LBO} is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and \overline{CS}_1 signals. For example, when \overline{CE} and \overline{CS}_1 are LOW on this waveform, CS0 is HIGH.

3519 drw 06

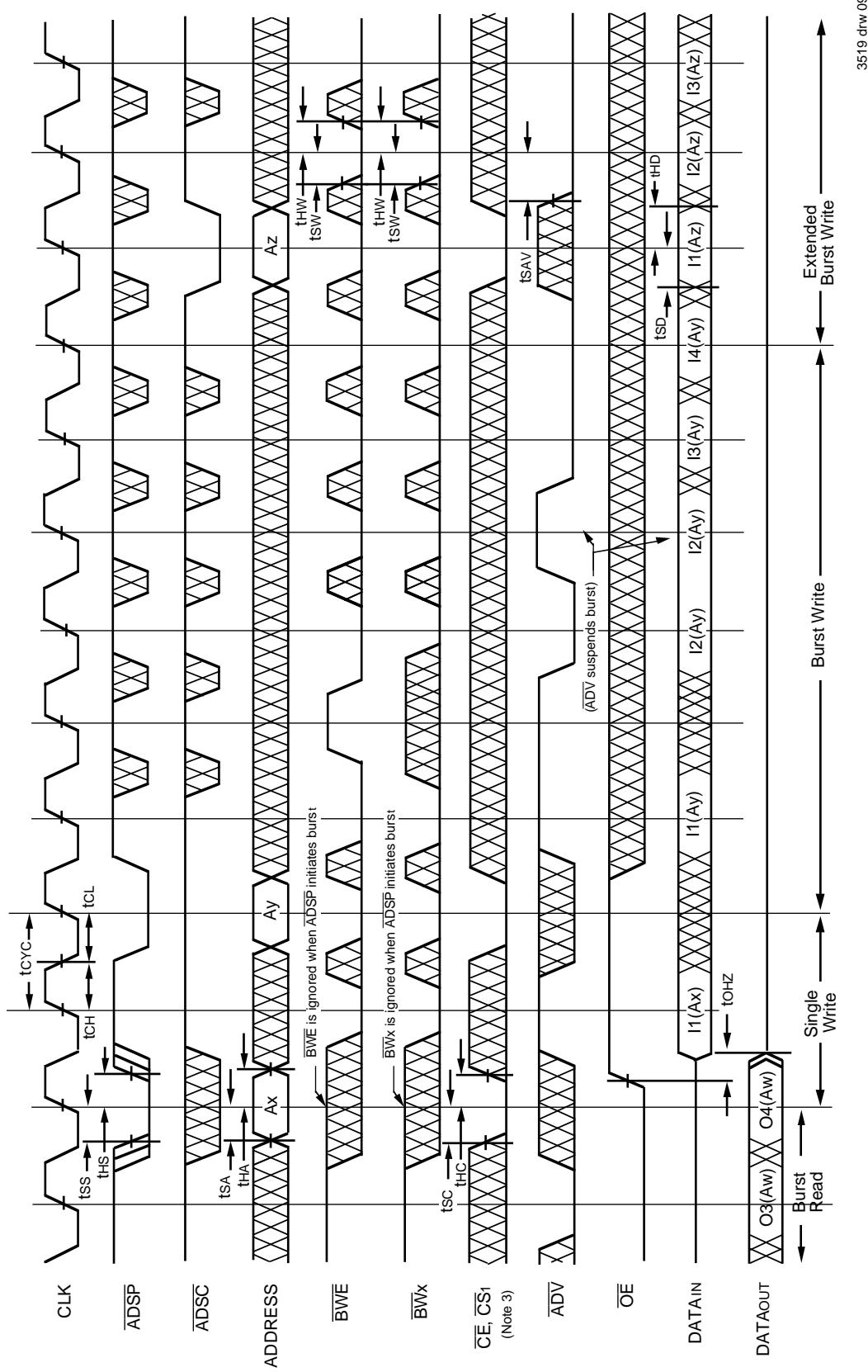
TIMING WAVEFORM OF COMBINED PIPELINED READ AND WRITE CYCLES^(1, 2,3)**NOTES:**

1. Device is selected through entire cycle; \overline{CE} and \overline{CS}_1 are LOW, CS_0 is HIGH.
2. ZZ input is LOW and \overline{LB}_0 is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LB}_0 input.

3519 drw 07

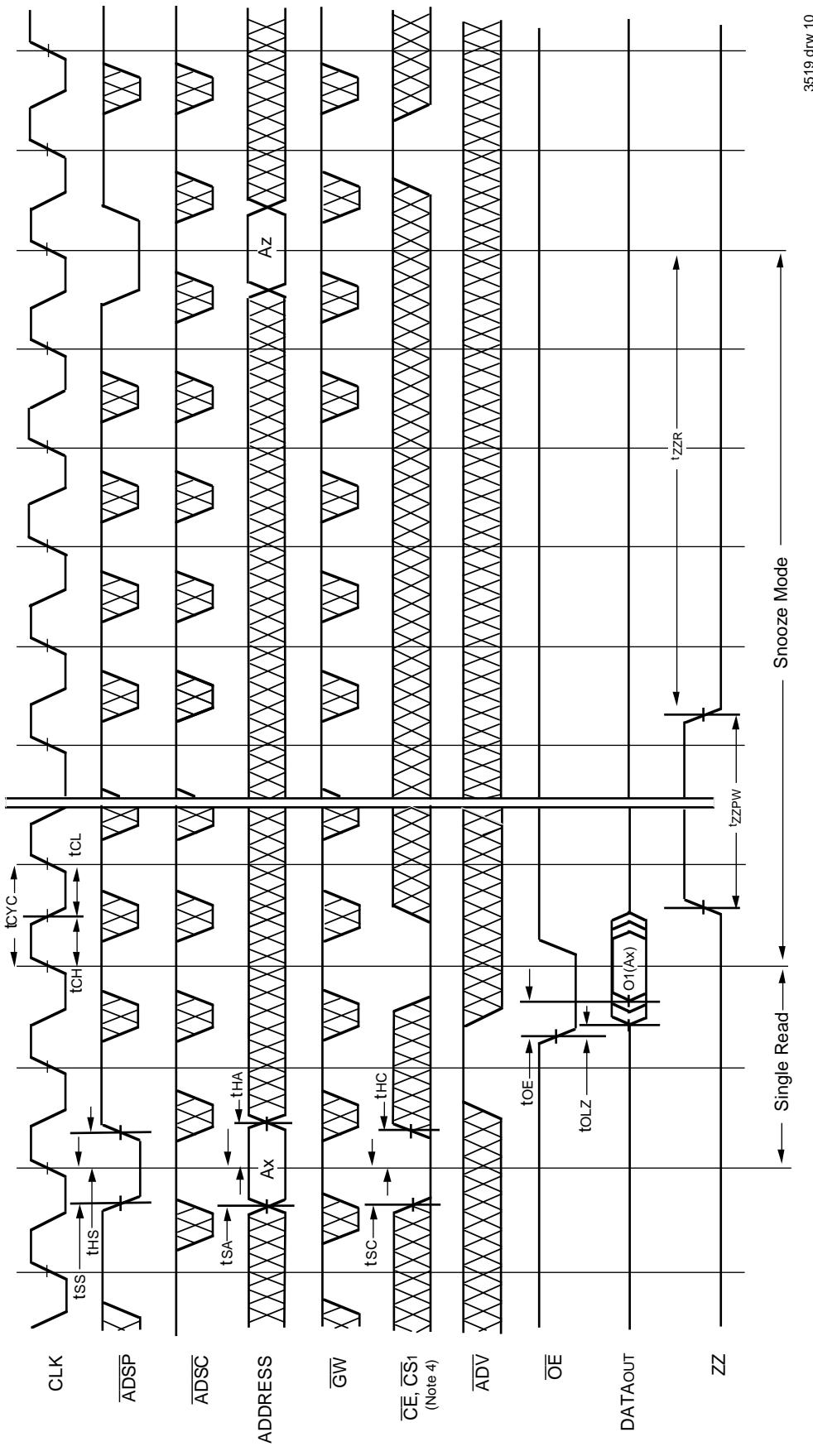
TIMING WAVEFORM OF WRITE CYCLE NO. 1 - \overline{GW} CONTROLLED^(1, 2, 3)**NOTES:**

1. ZZ input is LOW, $\overline{BW/E}$ is HIGH, and $\overline{LB/O}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LB/O}$ input.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 - BYTE CONTROLLED^(1, 2, 3)

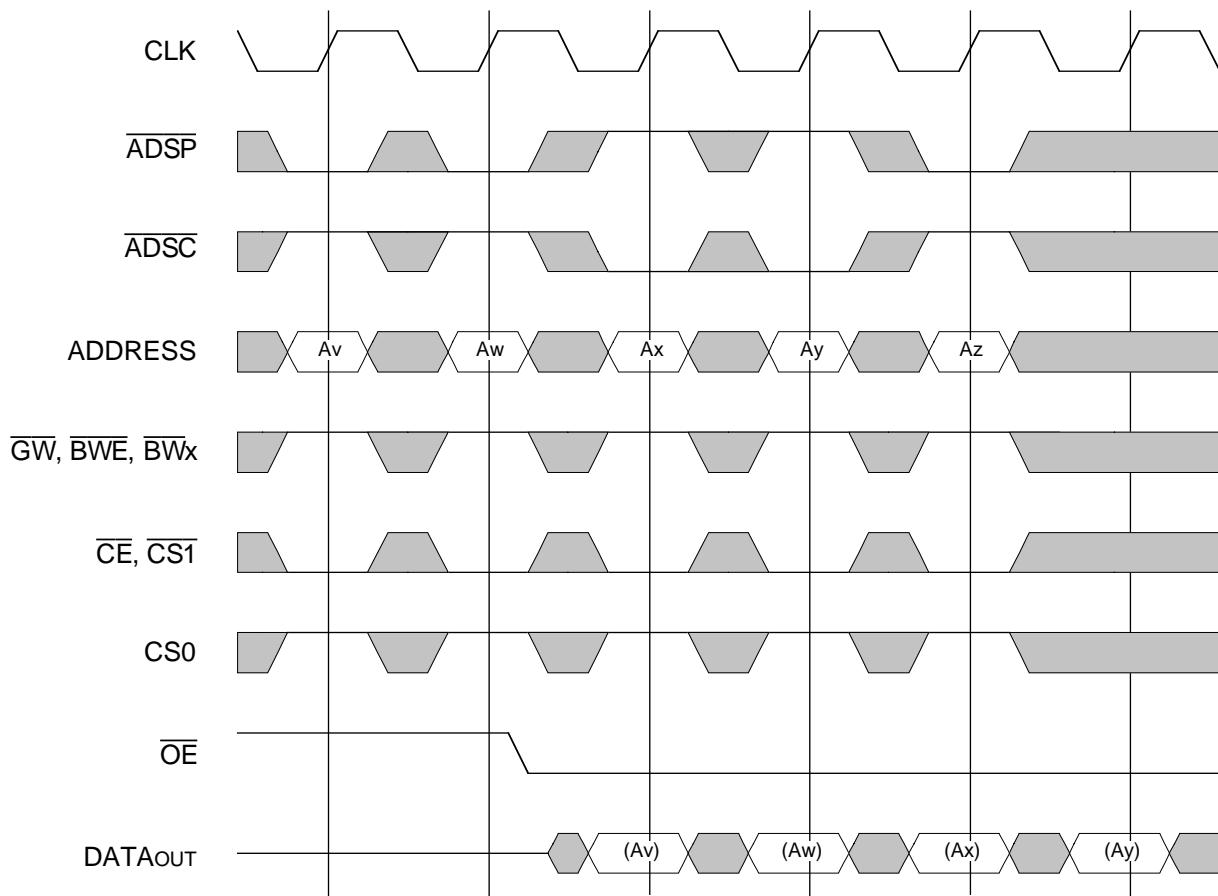
NOTES:

1. ZZ input is LOW, \overline{GW} is HIGH, and \overline{BO} is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{BO} input.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

TIMING WAVEFORM OF SLEEP (ZZ) AND POWER-DOWN MODES^(1, 2, 3)**NOTES:**

1. ZZ input is LOW, \overline{GW} is HIGH, and \overline{LBO} is Don't Care for this cycle.
2. $O_1(A_x)$ represents the first output from the external address A_x ; $O_2(A_y)$ represents the next output data in the burst sequence of the base address A_y , etc. where A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and \overline{CS}_1 signals. For example, when \overline{CE} and \overline{CS}_1 are LOW on this waveform, CS0 is HIGH.

NON-BURST READ CYCLE TIMING WAVEFORM

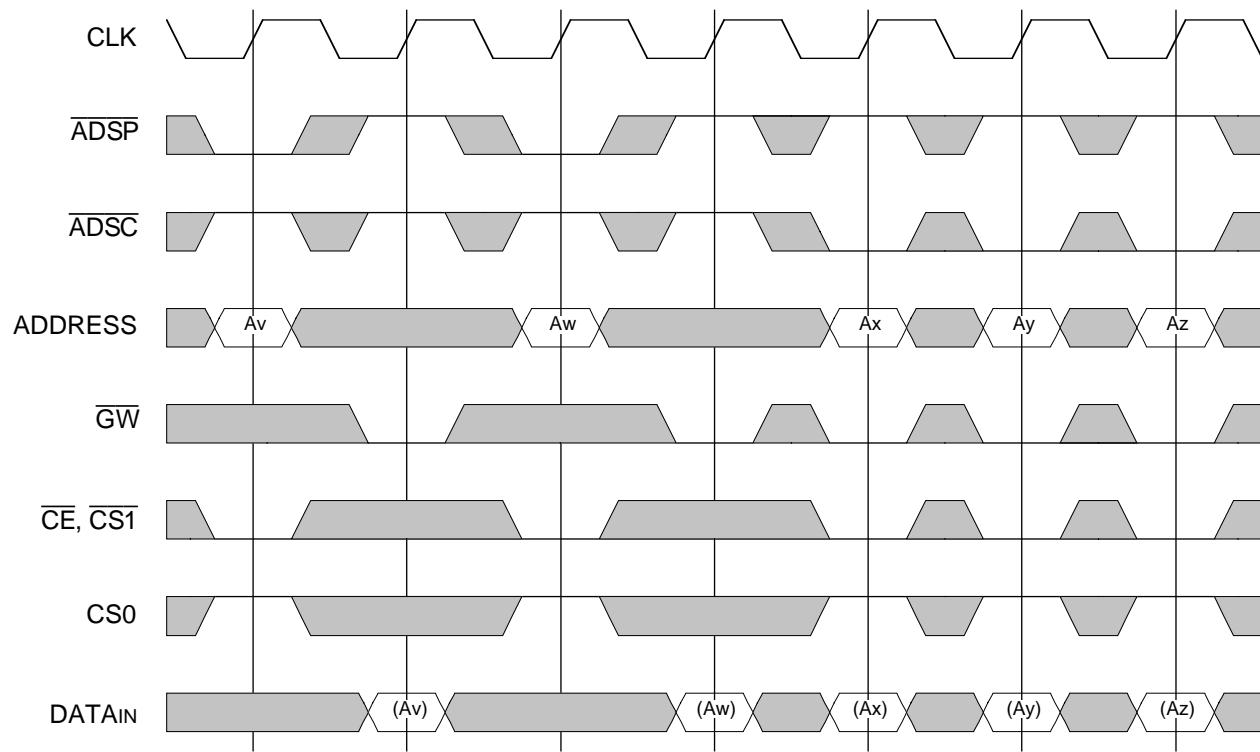


NOTES:

1. ZZ input is LOW, \overline{ADV} is HIGH, and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, \overline{ADSP} and \overline{ADSC} function identically and are therefore interchangeable.

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NON-BURST WRITE CYCLE TIMING WAVEFORM



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NOTES:

1. ZZ input is LOW, ADV and OE are HIGH, and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only GW writes are shown, the functionality of BWE and BWx together is the same as GW.
4. For write cycles, ADSP and ADSC have different limitations.

ORDERING INFORMATION

IDT	71V536	S	X	PF
Device Type		Power	Speed	Package
				PF } Plastic Thin Quad Flatpack, 100 pin (PK100-1)
				5 } Speed (clock to data valid) in nanoseconds
				6 }
				7 }

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