High-Speed CMOS 256 x 36 x 2 Bi-directional FIFO

QS725420A

FEATURES/BENEFITS

- Fast cycle times: 20/25/30/35 ns
- Two 256 x 36-bit FIFO buffers
- Full 36-bit word width
- Selectable 36/18/9-bit word width on port B
- Fully asynchronous operation of port A and port B
- Synchronous control at both ports
- Enable, request, and address control inputs are sampled on the rising clock edge
- Synchronous request/acknowledge “handshake” capability
- Device comes up into a known default state at reset
- Asynchronous output enables
- Five status flags per port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Almost-Full flag and Almost-Empty flag are programmable
- Mailbox registers with synchronized flags
- Data-retransmit function
  – Automatic byte parity checking
- I_{OL} = 8 mA, three-state outputs
- TTL CMOS-compatible I/O
- Space-saving PQFP & TQFP packages
- Pin-compatible and functionally equivalent to Sharp LH5420 and LH543601

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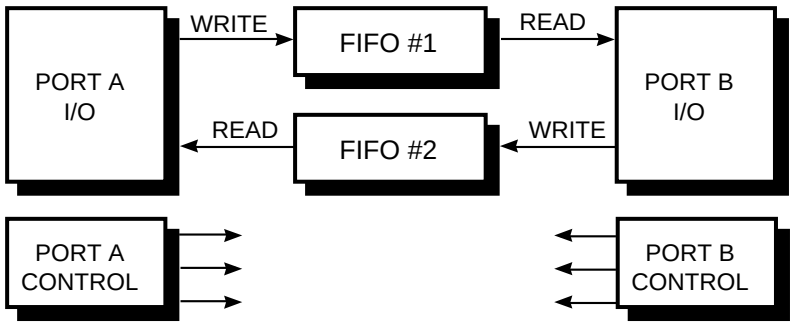
DESCRIPTION

The QS725420A contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bi-directional data buffering. FIFO #1 and FIFO #2 each are organized as 256 words by 36 bits.

The QS725420A is ideal either for wide unidirectional applications or for bi-directional data applications where component count and board area need to be reduced.

The QS725420A has two 36-bit ports, port A and port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the QS725420A is a fully static part.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION *(Continued)*

Conceptually, the port clocks CKA and CKB are free-running, periodic "clock" waveforms, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that these "clock" waveforms must be periodic. An "asynchronous" mode of operation is possible, in one or both directions, independently, if the appropriate enable and request inputs are continuously asserted, and enough aperiodic "clock" pulses of suitable duration are generated by external logic to cause all necessary actions to occur.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/acknowledge handshake resolves FIFO full and empty boundary conditions when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for each FIFO. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 256 or fewer words may be retransmitted any desired number of times.

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a new-mail-alert flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths.

A byte parity check flag at each port monitors data integrity. Control-register bit 0 (zero) selects the parity mode, odd or even. This bit is initialized for odd data parity at reset; but it may be reprogrammed for even parity, or back again to odd parity, as desired.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

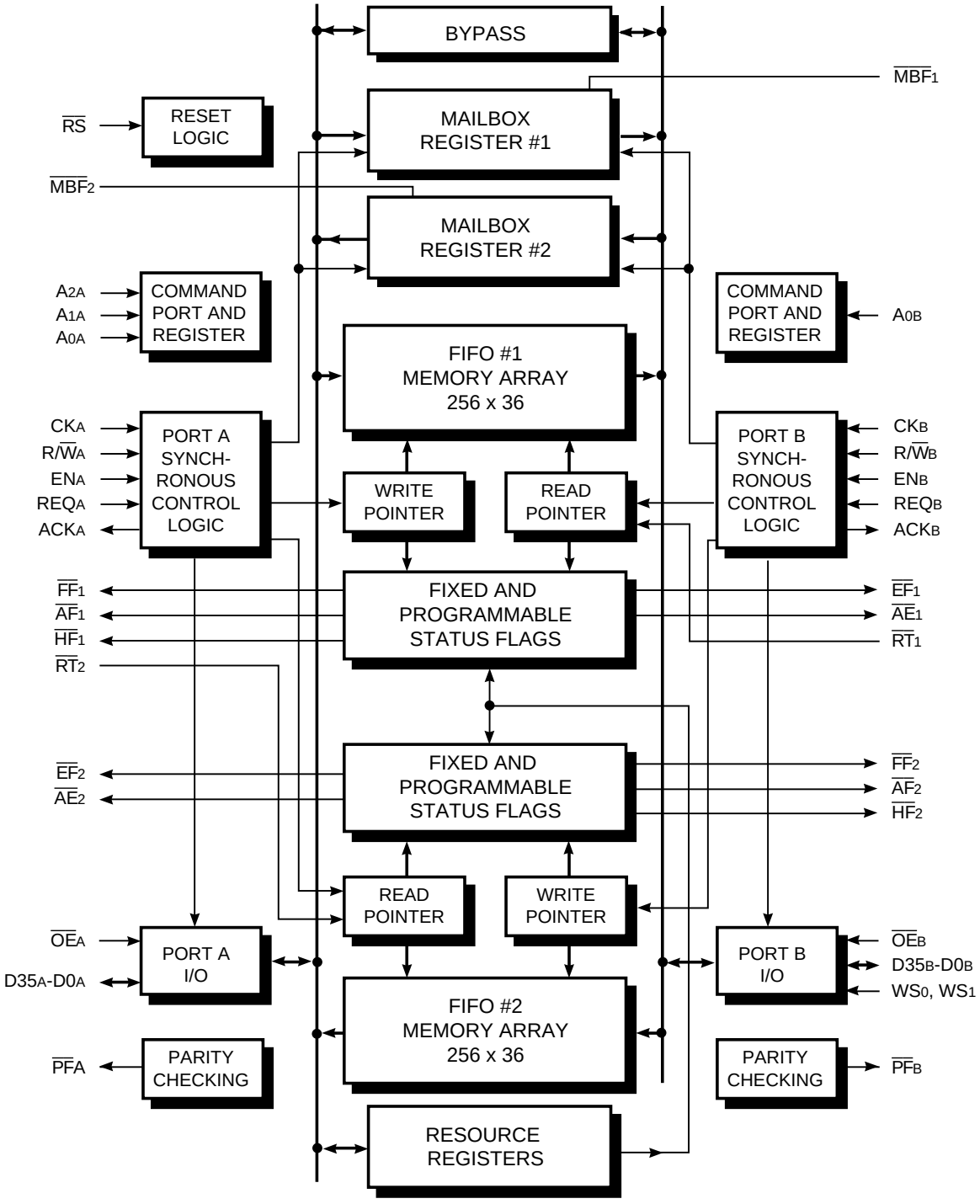


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FIGURE 3. PINOUTS

132-Pin Quad Flat Package
(Top view)

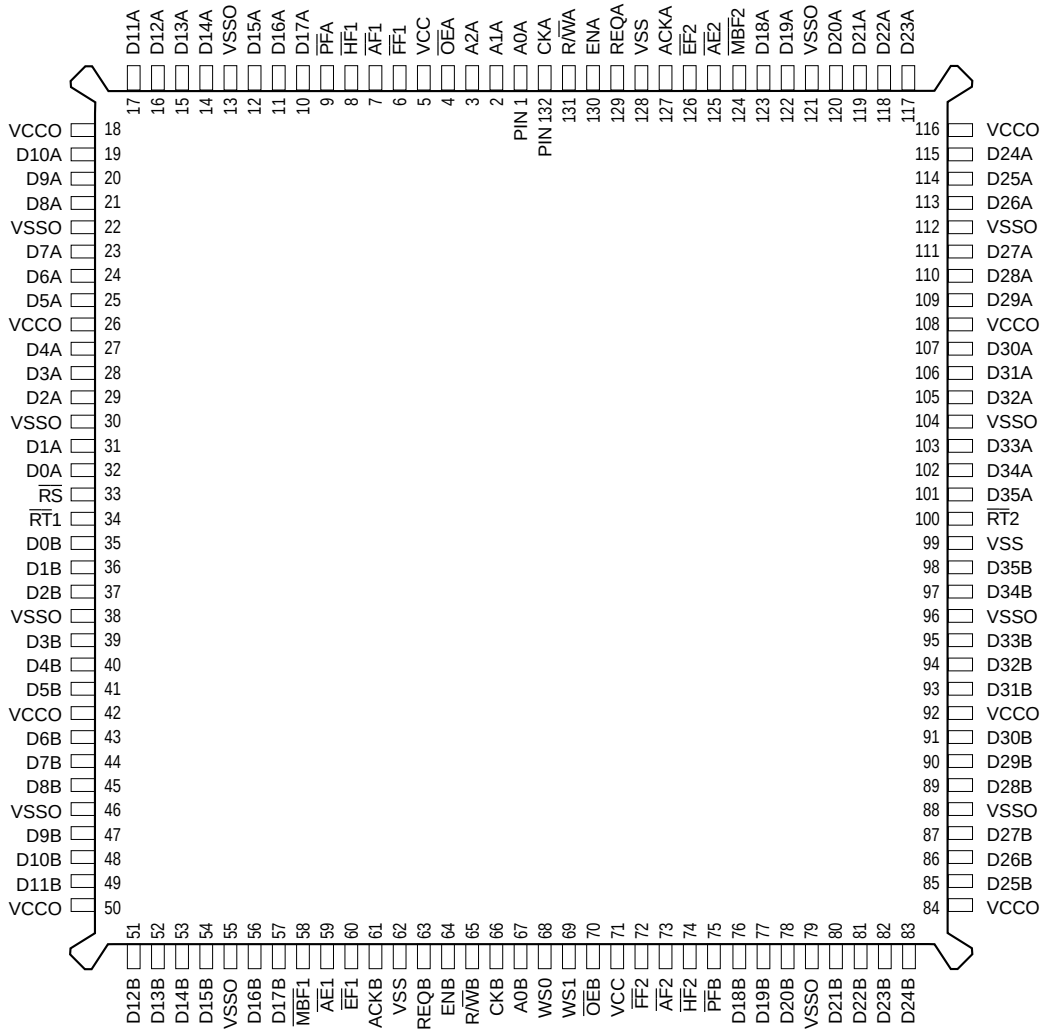
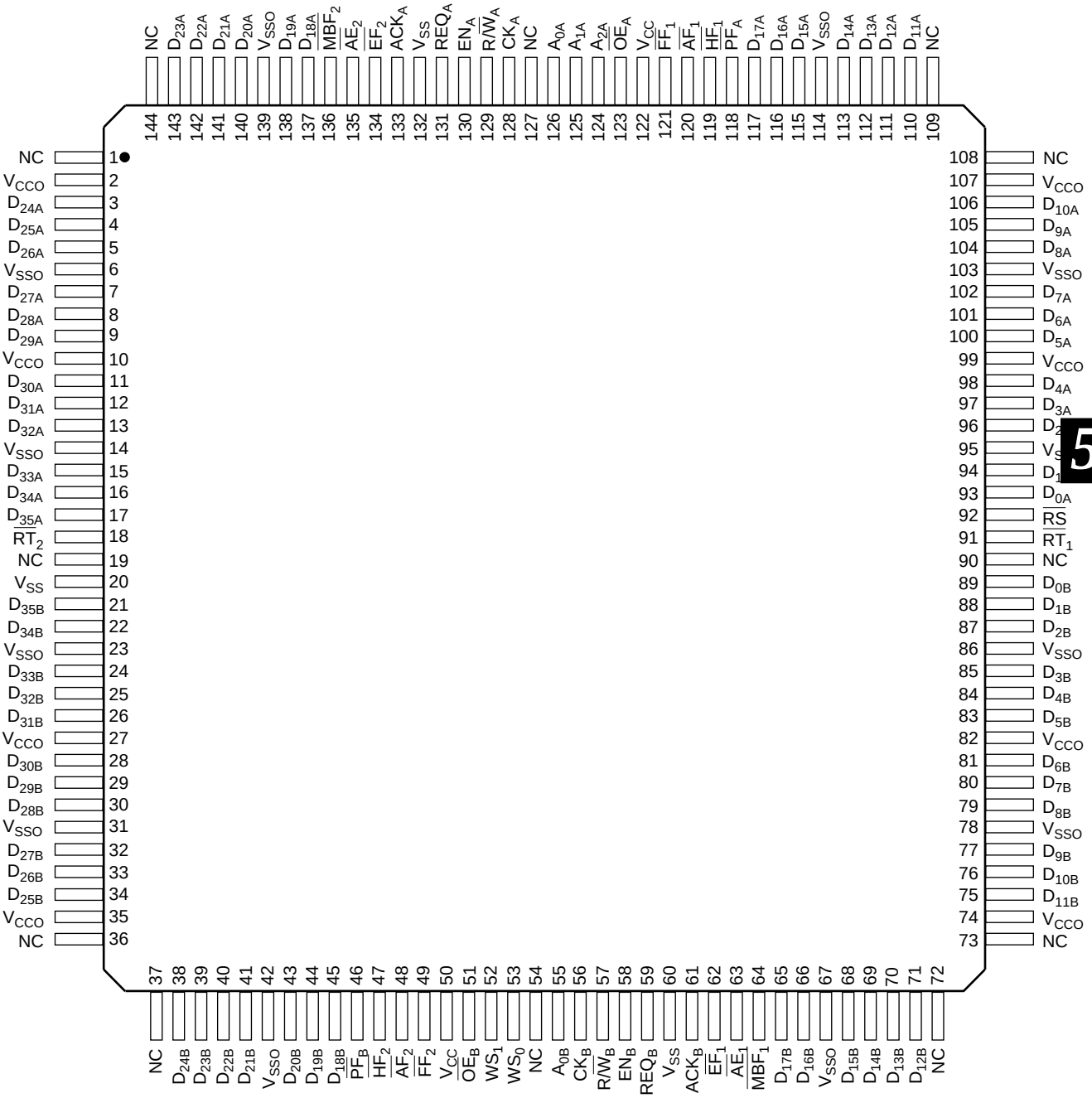


FIGURE 4. PINOUTS

144-Pin Quad Flat Package
(Top view)



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PIN DESCRIPTION

Signal Name	PQFP Pin No.	TQFP Pin No.
A0A	1	126
A1A	2	125
A2A	3	124
$\overline{OE}$A	4	123
$\overline{FF}$1	6	121
$\overline{AF}$1	7	120
$\overline{HF}$1	8	119
$\overline{PF}$A	9	118
D17A	10	117
D16A	11	116
D15A	12	115
D14A	14	113
D13A	15	112
D12A	16	111
D11A	17	110
D10A	19	106
D9A	20	105
D8A	21	104
D7A	23	102
D6A	24	101
D5A	25	100
D4A	27	98
D3A	28	97
D2A	29	96
D1A	31	94
D0A	32	93
$\overline{RS}$	33	92
$\overline{RT}$1	34	91
D0B	35	89
D1B	36	88
D2B	37	87
D3B	39	85
D4B	40	84
D5B	41	83
D6B	43	81
D7B	44	80
D8B	45	79
D9B	47	77
D10B	48	76
D11B	49	75
D12B	51	71
D13B	52	70
D14B	53	69
D15B	54	68
D16B	56	66
D17B	57	65
$\overline{MBF}$1	58	64
$\overline{AE}$1	59	63

Signal Name	PQFP Pin No.	TQFP Pin No.
$\overline{EF}$1	60	62
ACKB	61	61
REQB	63	59
ENB	64	58
R/$\overline{W}$B	65	57
CKB	66	56
A0B	67	55
WS0	68	53
WS1	69	52
$\overline{OE}$B	70	51
$\overline{FF}$2	72	49
$\overline{AF}$2	73	48
$\overline{HF}$2	74	47
$\overline{PF}$B	75	46
D18B	76	45
D19B	77	44
D20B	78	43
D21B	80	41
D22B	81	40
D23B	82	39
D24B	83	38
D25B	85	34
D26B	86	33
D27B	87	32
D28B	89	30
D29B	90	29
D30B	91	28
D31B	93	26
D32B	94	25
D33B	95	24
D34B	97	22
D35B	98	21
$\overline{RT}$2	100	18
D35A	101	17
D34A	102	16
D33A	103	15
D32A	105	13
D31A	106	12
D30A	107	11
D29A	109	9
D28A	110	8
D27A	111	7
D26A	113	5
D25A	114	4
D24A	115	3
D23A	117	143
D22A	118	142
D21A	119	141

Signal Name	PQFP Pin No.	TQFP Pin No.
D20A	120	140
D19A	122	138
D18A	123	137
$\overline{MBF}$2	124	136
$\overline{AE}$2	125	135
$\overline{EF}$2	126	134
ACKA	127	133
REQA	129	131
ENA	130	130
R/$\overline{W}$A	131	129
CKA	132	128
VCC	5	122
VSSO	13	114
NC	—	109
NC	—	108
VCCO	18	107
VSSO	22	103
VCCO	26	99
VSSO	30	95
NC	—	90
VSSO	38	86
VCCO	42	82
VSSO	46	78
VCCO	50	74
NC	—	73
NC	—	72
VSSO	55	67
VSS	62	60
NC	—	54
VCC	71	50
VSSO	79	42
NC	—	37
NC	—	36
VCCO	84	35
VSSO	88	31
VCCO	92	27
VSSO	96	23
VSS	99	20
NC	—	19
VSSO	104	14
VCCO	108	10
VSSO	112	6
VCCO	116	2
NC	—	1
NC	—	144
VSSO	121	139
VSS	128	132
NC	—	127

NOTES:
VCC = Supply internal logic. Connected to each other.
VCCO = Supply output drivers only. Connected to each other.
VSS = Supply internal logic. Connected to each other.
VSSO = Supply output drivers only. Connected to each other.

PIN DESCRIPTION

Name	Type[1]	Description
		GENERAL
Vcc, Vss	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CKA	I	Port A Free-Running Clock
R/$\overline{W}$A	I	Port A Edge-Sampled Read/Write Control
ENA	I	Port A Edge-Sampled Enable
A0A, A1A, A2A	I	Port A Edge-Sampled Address Pins
$\overline{OE}$A	I	Port A Level-Sensitive Output Enable
REQA	I	Port A Request/Enable
$\overline{RT}$2	I	FIFO #2 Retransmit
D35A-D0A	I/O/Z	Port A Bi-directional Data Bus
$\overline{FF}$1	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}$1	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}$1	O	FIFO #1 Half-Full Flag
$\overline{AE}$2	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}$2	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}$2	O	New-Mail-Alert Flag for Mailbox #2
$\overline{PF}$A	O	Port A Parity Flag
ACKA	O	Port A Acknowledge
		PORT B
CKB	I	Port B Free-Running Clock
R/$\overline{W}$B	I	Port B Edge-Sampled Read/Write Control
ENB	I	Port B Edge-Sampled Enable
A0B	I	Port B Edge-Sampled Address Pin
$\overline{OE}$B	I	Port B Level-Sensitive Output Enable
WS0, WS1	I	Port B Word-Width Select
REQB	I	Port B Request/Enable
$\overline{RT}$1	I	FIFO #1 Retransmit
D35B-D0B	I/O/Z	Port B Bi-directional Data Bus
$\overline{FF}$2	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}$2	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}$2	O	FIFO #2 Half-Full Flag
$\overline{AE}$1	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}$1	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}$1	O	New-Mail-Alert Flag for Mailbox #1
$\overline{PFB}$	O	Port B Parity Flag
ACKB	O	Port B Acknowledge

NOTES:
1. V = Power Voltage Level, I = Input, O = Output, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Input Voltage V_{IN}[1]	–0.5V to Vcc + 0.5V
DC Output Current Max. Sink Current/Pin[2]	±40 mA
Maximum Power Dissapation	2W
Temperature Range with Power Applied	–55° to +125°C
T_{STG} Storage Temperature	–65° to +125°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional- or reliability-type failures.

Notes:
1. Negative undershoot of 1.5V in amplitude is permited for up to 10 ns, once per cycle.
2. Only one output may be shorted at a time, for a period not exceeding 30 Seconds.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.2	Vcc + 0.5	V
V_{IL}	Input LOW Voltage[1]	Logic LOW for All Inputs	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –8 mA	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	—	0.4	V
I_{LO}	I/O Leakage	0V ≤ V_{OUT} ≤ V_{CC}, $\overline{OE}$ ≥V_{IH}	–10	+10	µA
I_{IL}	Input Leakage	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–10	+10	µA

Note:
1. Negative undershoot of 1.5V in amplitude is permited for up to 10 ns, once per cycle.

POWER SUPPLY CHARACTERISTICS

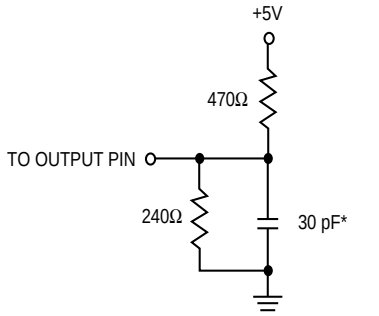
Symbol	Parameter	Min	Max	Units
I_{CC}	Operating Current[1,2] f_C = Max.	—	280	mA
I_{CC2}	Standby Current[1] All Inputs = V_{IHMIN} (Clocks Idle)	—	25	mA
I_{CC3}	Power Down Current[1] All Inputs at V_{CC} – 0.2V (Clocks Idle)	—	0.1	mA
I_{CC4}	Power Down Current[1] All Inputs at V_{CC} – 0.2V (Clocks at f_C = Max.)	—	10	mA

Notes:
1. I_{CC}, I_{CC2}, I_{CC3}, and I_{CC4} are dependent upon actual output loading, and I_{CC} and I_{CC4} are also dependent on cycle rates. Specified values are with outputs open (for I_{CC}: C_{LSD} = 0 pF); and, for I_{CC} and I_{CC4}, operating at minimum cycle times.
2. I_{CC} using worst case conditions and data pattern.

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3V
Input Rise/Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	30 pF

FIGURE 5. OUTPUT LOAD CIRCUIT



* Includes jig and scope capacitances.

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CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Name	Description[1]	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	—	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF

Note:
1. Capacitance is guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

Symbol	Parameter[1]	Speed (ns) -20 Min	-20 Max	-25 Min	-25 Max	-30 Min	-30 Max	-35 Min	-35 Max	Units
f_{CC}	Clock Cycle Frequency	—	50	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	20	—	25	—	30	—	35	—	ns
t_{CH}	Clock HIGH Time	8	—	10	—	12	—	15	—	ns
t_{CL}	Clock LOW Time	8	—	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	9.6	—	12	—	13	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time	10.4	—	13	—	15	—	15	—	ns
t_{EH}	Enable Hold Time	0	—	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	10.4	—	13	—	15	—	18	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time	12	—	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time	0	—	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time[6]	12	—	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time[6]	0	—	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	12.8	—	16	—	20	—	25	ns
t_{ACK}	Acknowledge Access Time	—	12	—	15	—	20	—	25	ns
t_{OH}	Output Hold Time[6]	2	—	2	—	2	—	2	—	ns
t_{ZX}	Output Enable Time[2] $\overline{OE}$ LOW to D35-D0 LOW-Z	1.5	—	2	—	3	—	3	—	ns
t_{XZ}	Output Disable Time[2] $\overline{OE}$ HIGH to D35-D0 HIGH-Z	—	9	—	12	—	15	—	20	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	17.6	—	22	—	25	—	30	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	17.6	—	22	—	25	—	30	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full Flag)	—	17.6	—	22	—	25	—	30	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty Flag)	—	16	—	20	—	25	—	30	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full Flag)	—	16	—	20	—	25	—	30	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	12	—	15	—	20	—	25	ns
t_{PF}	Data to Parity Flag Valid	—	13.6	—	17	—	20	—	25	ns
t_{RS}	Reset/Retransmit Pulse Width[7]	32/20	—	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time[3]	16	—	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time[3]	8	—	10	—	15	—	20	—	ns
t_{RF}	Reset LOW to Flag Valid	—	28	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency[4]	20	—	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency[5]	20	—	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	12	—	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	3	—	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	18	—	20	—	25	—	30	ns

Notes:

1. Timing measurements performed at AC TEST CONDITION levels.
2. Values are guaranteed by design, not currently production tested.
3. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CK_A occurs while EN_A is being asserted, or else a rising edge of CK_B occurs while EN_B is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.
6. t_{AS}, t_{AH} address setup times and hold times need only be satisfied at clock edges which occur while the corresponding enables are being asserted.
7. First number used only when CK_A or CK_B is enabled: $t_{RS} = t_{RSS} + t_{CH} + t_{RSH}$.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset ($\overline{RS}$) input is taken LOW, and at least one rising edge and the falling edge of both CLK_A and CLK_B occur while $\overline{RS}$ is LOW. A reset operation is required after power-up, before the first write operation may occur. The QS725420A is fully ready for operation after being reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFOs' first physical memory locations. If the respective outputs are enabled, the initial contents of these first locations appear at the outputs. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE1}$/$\overline{AE2}$ flags get asserted within eight locations of an empty condition, and the $\overline{AF1}$/$\overline{AF2}$ flags likewise get asserted within eight locations of a full condition, for FIFO #1/FIFO #2, respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on port A during reset transfers data directly to or from port B. Port B is considered to be the slave, and cannot perform write or read operations independently on its own during reset.

The direction of the bypass data transmission is determined by the R/$\overline{W}$A control input, which does not get overridden by the $\overline{RS}$ input. Here, a "write" operation means passing data from Port A to Port B, and a"read" operation means passing data from Port B to Port A.

The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device during reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A0, A1 and A2, which select between FIFO access, mailbox-register access, control-register access (write only), and programmable flag-offset-value register access. Port B has a single address input, $A0_B$, to select between FIFO access or mailbox-register access.

The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Resource-register select-input address definitions are summarized in Table 1.

FIFO Write

Port A writes to FIFO #1, and port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate read/write control (R/$\overline{W}_A$ a R/$\overline{W}_B$) is held LOW; the FIFO address is selected for the address inputs ($A2_A$-$A0_A$ or $A0_B$); and the prescribed setup times and hold times are observed for all of these signals. Setup times and hold times must also be observed on the data-bus pins ($D0_A$-$D35_A$ or $D0_B$-$D35_B$).

TABLE 1. RESOURCE-REGISTER ADDRESSES

$A2_A$	$A1_A$	$A0_A$	Resource
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ Flag Offset Registers (36-bit Mode)
H	L	L	Control Registers (Parity Mode)
L	H	H	$\overline{AE}_1$ Flag Offset Registers
L	H	L	$\overline{AF}_1$ Flag Offset Registers
L	L	H	$\overline{AE}_2$ Flag Offset Registers
L	L	L	AF_2 Flag Offset Registers
$A0_B$			**Resource**
PORT B			
		H	FIFO
		L	Mailbox

Normally, the appropriate output enable signal ($\overline{OE}_A$ or $\overline{OE}_B$) is HIGH, to disable the outputs at that port, so that the data word present on the bus from external sources gets stored. However, a “loopback” mode of operation also is possible, in which the data word supplied by the outputs of one internal FIFO is “turned around” at the port and read back into the other FIFO. In this mode, the outputs at the port are not disabled. To remain within specification for all timing parameters, the clock cycle frequency must be reduced slightly below the value which otherwise would be permissible for that speed grade of QS725420A.

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding full flag is de-asserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a first write latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data are retrieved.

FIFO Read

Port A reads from FIFO #2 and port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate read/write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; the FIFO address is selected for the address inputs ($A2_A$-$A0_A$ or A0); and the prescribed setup times and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins ($D35_A$-$D0_A$ or $D35_B$-$D0_B$) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive LOW, asynchronous, output enable control input signals. Their effect is only to enable or disable the output drivers of the respective port. Disabling the outputs does not disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs again are enabled, unless it subsequently is overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be asserted (HIGH). The first read operation should begin no earlier than a first read latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for full ($\overline{FF}$ and $\overline{FF}2$), half-full ($\overline{HF}$ and $\overline{HF}2$), and empty ($\overline{EF}$ and $\overline{EF}2$). $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$ indicate the status of FIFO #1; and $\overline{FF}2$, $\overline{HF}2$, and $\overline{EF}2$ indicate the status of FIFO #2.

A Full flag is asserted following the rising clock edge for a write operation that fills the FIFO. A Full flag is de-asserted following the falling clock edge for a read operation to a full FIFO. A Half-Full flag is updated following the rising clock edge of a read or write operation to a FIFO. An Empty flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Empty flag is de-asserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided: two for almost-full ($\overline{AF}$ and $\overline{AF}2$), and two for almost-empty ($\overline{AE}1$ and $\overline{AE}2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset but can be reprogrammed over the entire FIFO depth.

An Almost-Full flag is asserted following the rising clock edge for a write operation that fills the FIFO. An Almost-Full flag is de-asserted following the falling clock edge for a read operation to a full FIFO. An Almost-Empty flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Almost-Empty flag is de-asserted following the falling clock edge for a write operation to an empty FIFO.

Flag offsets may be written or read through the port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word, or each programmable flag offset can be set individually through one of four 8-bit status words. Table 3 illustrates the data format for flag-programming words Also, Table 4 defines the meaning of each of the five flags, both the dedicated flags and the flag-programming flags, for the QS725420A.

WARNING: Control inputs which may affect the computation of flag values at a port generally should not change while the clock for that port is HIGH, since some updating of flag values takes place on the falling edge of the clock.

Mailbox Operation

Two mailbox registers are provided for passing system hardware or software control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable HIGH. That is, writing to mailbox register #1, or reading from mailbox register #2, is synchronized to CK_A; and writing to mailbox register #2, or reading from mailbox register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register accesses. Each mailbox register has its own New-Mail-Alert Flag ($\overline{MBF}1$ and $\overline{MBF}2$), which is synchronized to the reading port's clock. These new-mail-alert flags are status indicators only and cannot inhibit mailbox-register read or write operations.

Request/Acknowledge Handshake

A synchronous, request/acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronous-operated ports. The use of this feature is optional. When it is used, the request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read operation or a FIFO write operation is being requested. The acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does not prove that a FIFO write access or a FIFO read access actually took place. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a synchronized predictor of the Almost-Full flag $\overline{AF}$ for write operations, or as a synchronized predictor of the Almost-Empty flag $\overline{AE}$ for read operations.

Outside the "almost-full" region and the "almost-empty" region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the "almost-full" region or the "almost-empty" region, $ACK_{A/B}$ occurs only on every third cycle, to prevent an overrun of the FIFO's actual full or empty boundaries, and to ensure that the t_{FWL} (first-write latency) and t_{FRL} (first-read latency) specifications are satisfied before $ACK_{A/B}$ is received.

The "almost-full region" is defined as "that region, where the Almost-Full flag is being asserted"; and the "almost-empty region" as "that region, where the Almost-Empty flag is being asserted." Thus, the extent of these "almost" regions depends on how the system has programmed the offset values for the Almost-Full flags and the Almost-Empty flags. If the system has not programmed them, then these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is not asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port must be asserted for the corresponding FIFO to operate.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical memory location, so that data may be reread. The write pointer is not affected. The status flags are updated, and a block of up to 256 data words, which previously had been written into and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO memory location and the FIFO memory location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT}$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT}$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding retransmit signal is being asserted.

Parity Check

The Parity check flags, $\overline{PF}_A$ and $\overline{PF}_B$, are asserted (LOW) whenever there is a parity error in the data word present on the port A data bus or the port B data bus, respectively. The inputs to the parity-evaluation logic come directly (via isolation transistors) from the data-bus bonding pads, in each case. Thus, $\overline{PF}_A$ and $\overline{PF}_B$ provide parity-error indications for whatever 36-bit words are present at port A and port B, respectively, regardless of whether these words originated within the QS725420A or in the external system.

The four bytes of a 36-bit data word are grouped as D0-D8, D9-D17, D18-D26, and D27-D35. The parity of each 9-bit byte is individually checked, and the four single-bit parity indications are logically inclusive-ORed to produce the parity-flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even parity or for odd parity during operation. Control-register bit 0 (zero) selects the parity mode, odd or even (see Table 3).

All nine bits of each byte are treated alike by the parity logic. The byte parity over the nine bits is compared with the parity mode bit in the control register, to generate a byte-parity-error indication. Then, the four byte-parity-error signals are NORed together to compute the assertive-LOW parity-flag value.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS0 and WS1 control inputs. WS0 and WS1 both are tied HIGH for 36-bit access; they both are tied LOW for single-byte access. For double-byte access, WS0 is tied HIGH and WS1 is tied LOW.

In the single byte-access or double-byte access modes, FIFO write operations on port B essentially pack the data to form 36-bit words, as viewed from port <N> A. Similarly, single-byte or double-byte FIFO read operations on port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Since the values for each status flag are computed by logic directly associated with one of the two FIFO-memory arrays, and not by logic associated with port B, the flag values reflect the array fullness situation in terms of complete 36-bit words, and not in terms of bytes or double bytes.

However, there is no such restriction for switching from writing to reading, or from reading to writing, at port B. As long as t_{RWS}, t_{DS}, and t_A are satisfied, $R/\overline{W}_B$ may change state after any single-byte or double-byte access, and not only after a full 36-bit-word access.

Also, the word-width-matching feature continues to operate properly in “loopback” mode.

Note that the programmable word-width-matching feature is only supported for FIFO accesses. Mailbox and data bypass operations do not support word-width matching between port A and port B. Tables 2, 3, and 4, and Figures 6a, 6b, 7a, and 7b summarize word-width selection for Port B.

TABLE 2. PORT B WORD-WIDTH SELECTION

WS1	WS0	Port B Data Width
H	H	36-Bit
H	L	(Reserved)
L	H	18-Bit
L	L	9-Bit

TABLE 3. RESOURCE-REGISTER PROGRAMMING

Resource-Register Address A_{2A}	A_{1A}	A_{0A}	Resource-Register Contents							
			NORMAL FIFO OPERATION							
			D35A							**D0A**
H	H	H	X...							...X
			MAILBOX							
			D35A							**D0A**
H	H	L	X...							...X
			$\overline{AF}$2, $\overline{AE}$2, $\overline{AF}$1, $\overline{AE}$1 FLAG REGISTER (36-BIT MODE)							
			D35A	**D34A-D27A**	**D26A**	**D25A-D18A**	**D17A**	**D16A-D9A**	**D8A**	**D7A-D0A**
H	**L**	**H**	X	$\overline{AF}$2 Offset[1]	X	$\overline{AE}$2 Offset[1]	X	$\overline{AF}$1 Offset[1]	X	$\overline{AE}$1 Offset[1]
			CONTROL REGISTER (WRITE-ONLY) PARITY							
			D35A						**D1A**	**D0A**
H	L	L	X...						...X	Parity Mode[2]
			8-BIT $\overline{AE}$1 FLAG OFFSET REGISTER							
			D35A						**D8A**	**D7A-D0A**
L	H	H	X...						...X	$\overline{AE}$1 Offset[1]
			8-BIT $\overline{AF}$1 FLAG OFFSET REGISTER							
			D35A						**D8A**	**D7A-D0A**
L	H	L	X...						...X	$\overline{AF}$1 Offset[1]
			8-BIT $\overline{AE}$2 FLAG OFFSET REGISTER							
			D35A						**D8A**	**D7A-D0A**
L	L	H	X...						...X	$\overline{AE}$2 Offset[1]
			8-BIT $\overline{AF}$2 FLAG OFFSET REGISTER							
			D35A						**D8A**	**D7A-D0A**
L	L	L	X...						...X	$\overline{AF}$2 Offset[1]

Notes:
1. All four programmable-flag offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

TABLE 4. FLAG DEFINITION TABLE[1]

Flag	Valid Full-Word Read Cycles Remaining				Valid Full-Word Write Cycles Remaining			
	Flag = LOW		Flag = HIGH		Flag = LOW		Flag = HIGH	
	Min	Max	Min	Max	Min	Max	Min	Max
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256 – p	256	0	255 – p	0	p	p + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	q	q + 1	256	256 – q	256	0	255 – q
$\overline{EF}$	0	0	1	256	256	256	0	255

Note:
1. q = Programmable almost-empty offset value (default value: q = 8).
   p = Programmable almost-full offset value (default value: p = 8).

FIGURE 6A. 36-18 FUNNELING THROUGH FIFO #1

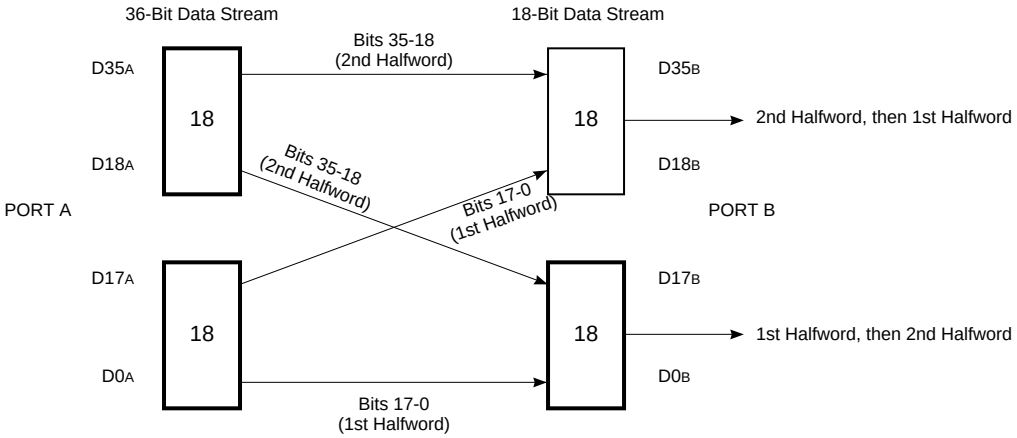
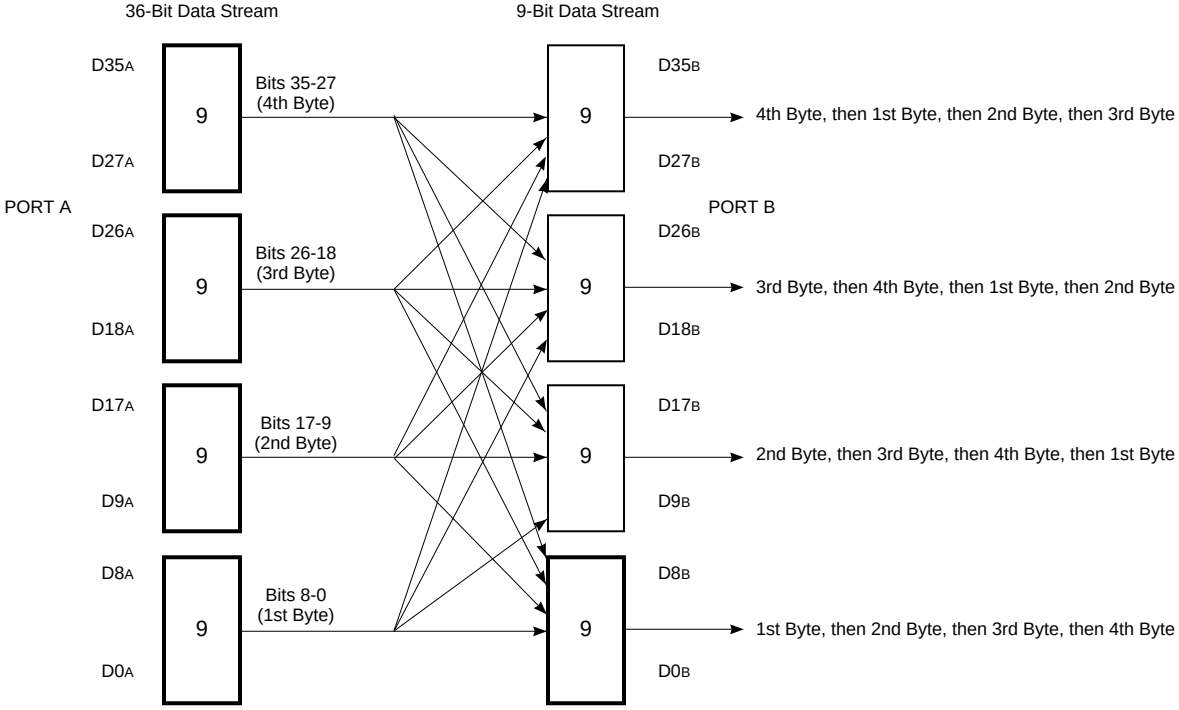


FIGURE 6B. 36-9 FUNNELING THROUGH FIFO #1



Notes:

1. The heavy black borders on the register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 6a) or bytes (Figure 6b) are transferred in parallel form from port A to port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle before again attempting to read data D35-D0, and three dummy words should be passed through initially. Also, incomplete data words may occur when the word width is changed from shorter to longer at an inappropriate point in the data block passing through the FIFO.

FIGURE 7A. 18-36 DEFUNNELING THROUGH FIFO #2

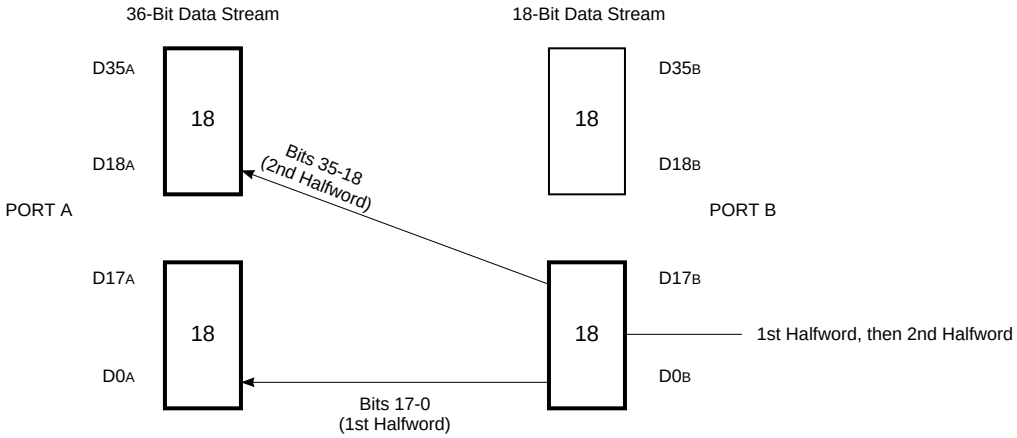
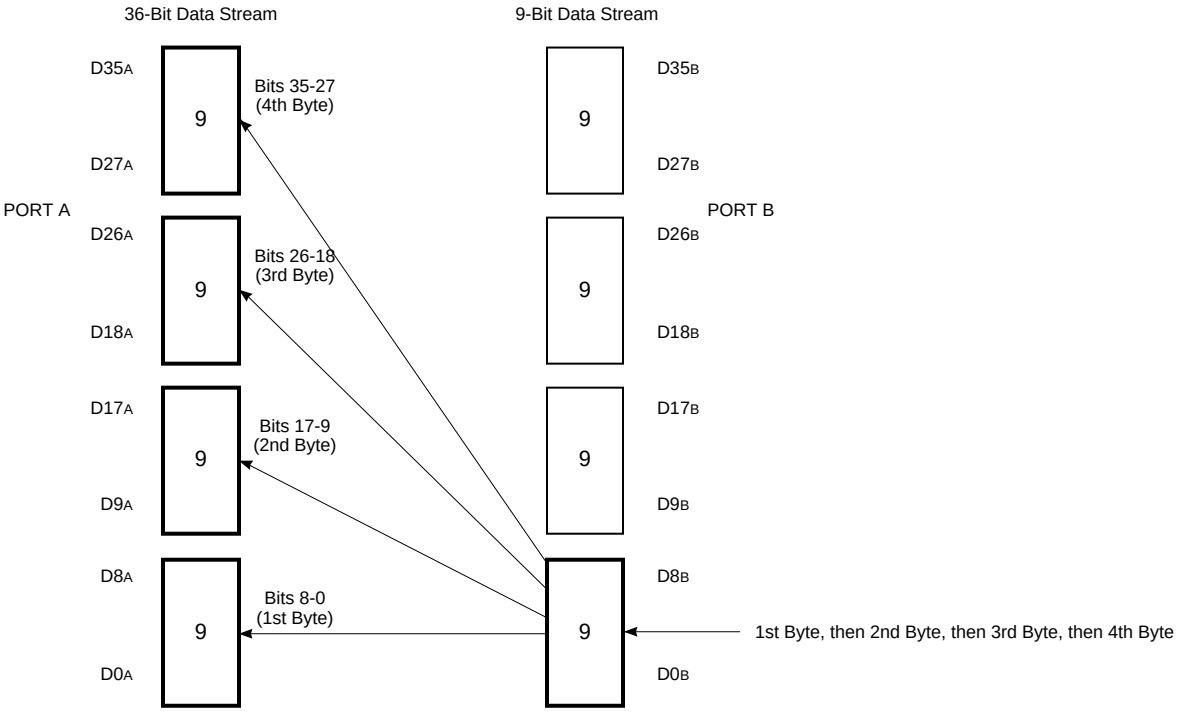


FIGURE 7B. 9-36 DEFUNNELING THROUGH FIFO #2

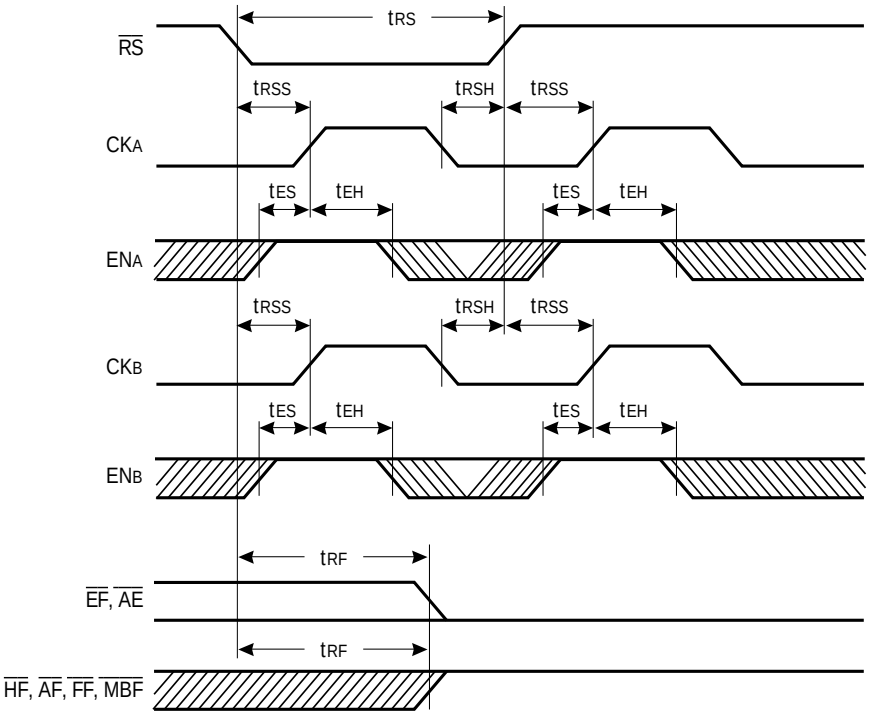


Notes:

1. The heavy black borders on the register segments indicate the only data paths used. The other byte seqments of port B do not participate in the data path during defunneling.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 7a) or bytes (Figure 7b) are transferred in parallel form from port A to port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle before again attempting to send data, and three dummy words should be passed through initially. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

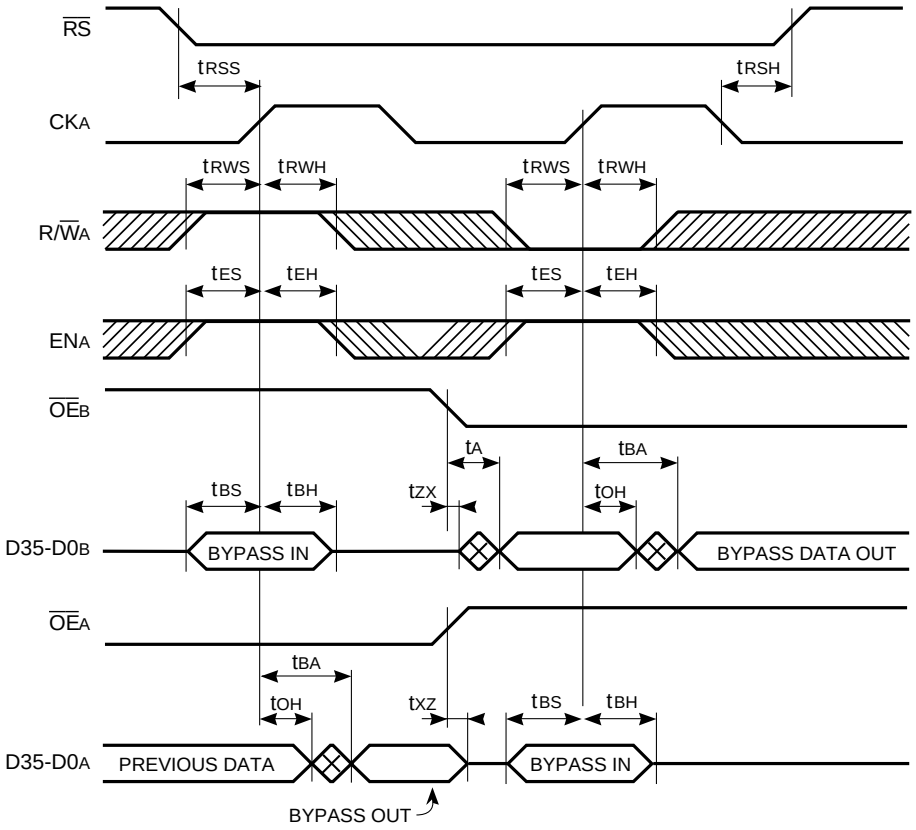
TIMING DIAGRAMS

FIGURE 8. RESET TIMING



Notes:
1. $\overline{RS}$ overrides all other input signals, except for R/$\overline{W}_A$, and operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted. However, at least one rising edge and one falling edge of both CK_A and CK_B must occur while $\overline{RS}$ is being asserted (is LOW), with timing as defined by t_{RSS} and t_{RSH}.
2. Otherwise, t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity check is initialized to odd-byte parity at reset.
4. The $\overline{AE}$ and $\overline{AF}$ flag offsets are initialized to eight locations from the boundary at reset.

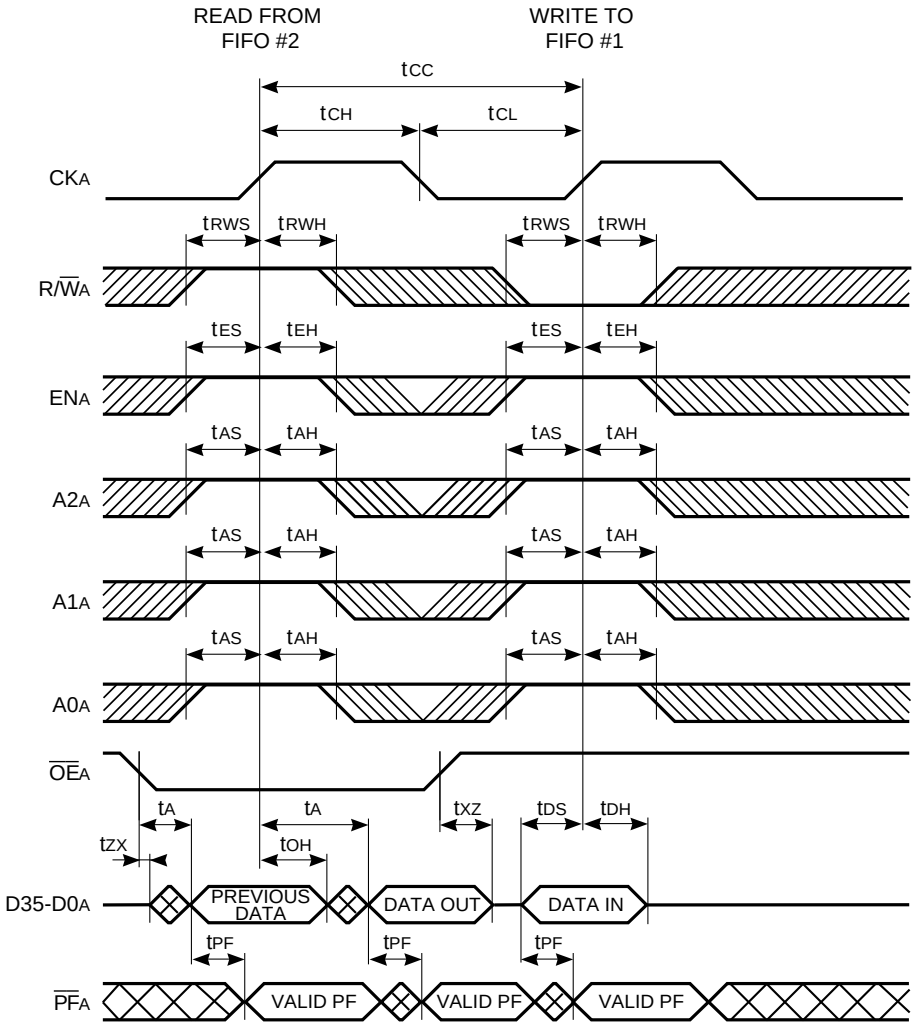
FIGURE 9. DATA BYPASS TIMING



Notes:
1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, and EN_A control the transmission of data between ports at reset.

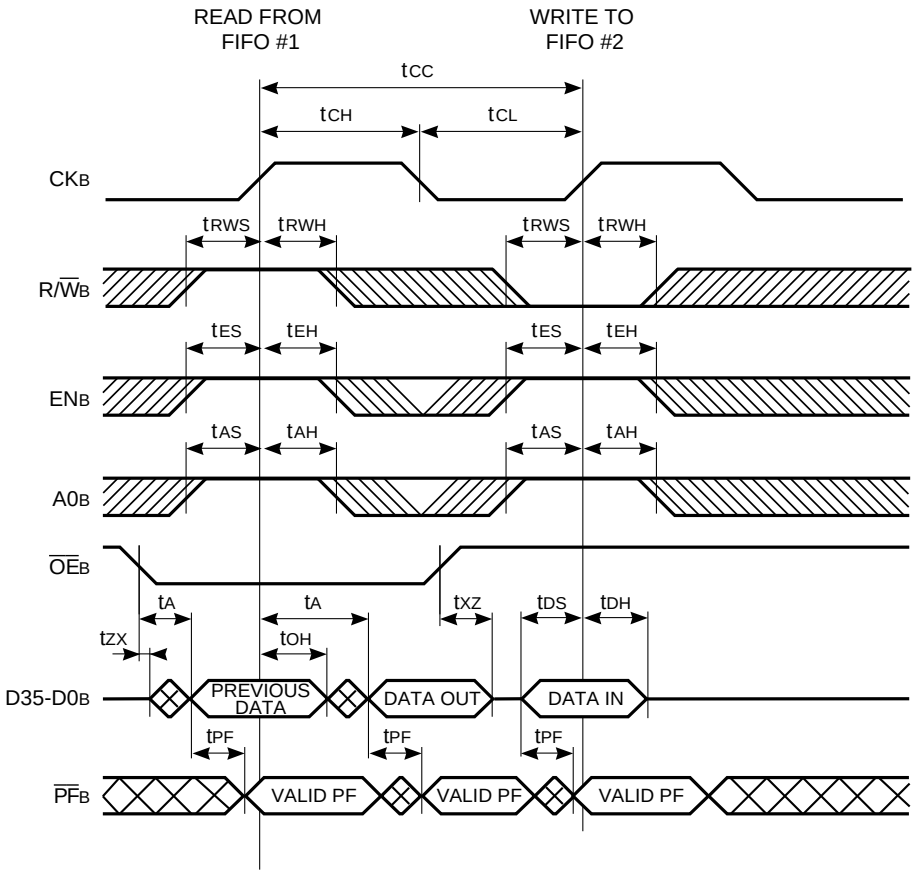
5

FIGURE 10. PORT A FIFO READ/WRITE



Notes:
1. The port A parity error flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

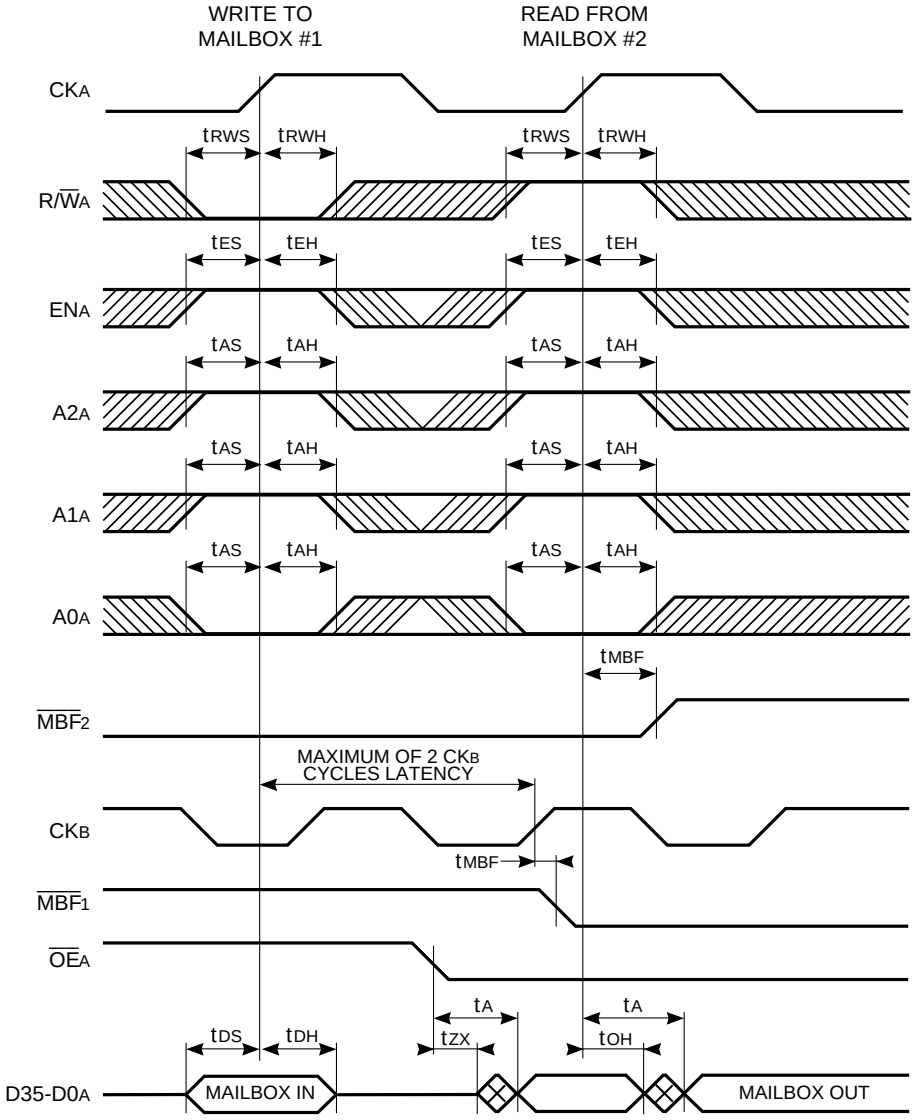
FIGURE 11. PORT B FIFO READ/WRITE



Notes:
1. The port B parity error flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

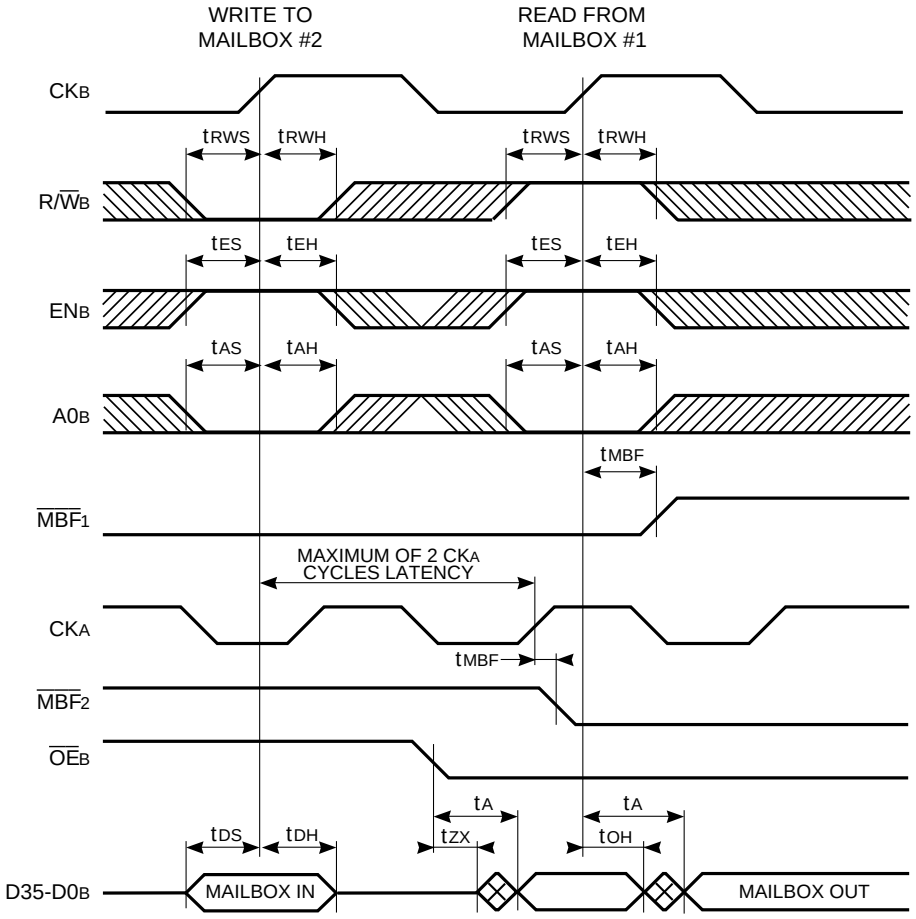
5

FIGURE 12. PORT A MAILBOX ACCESS



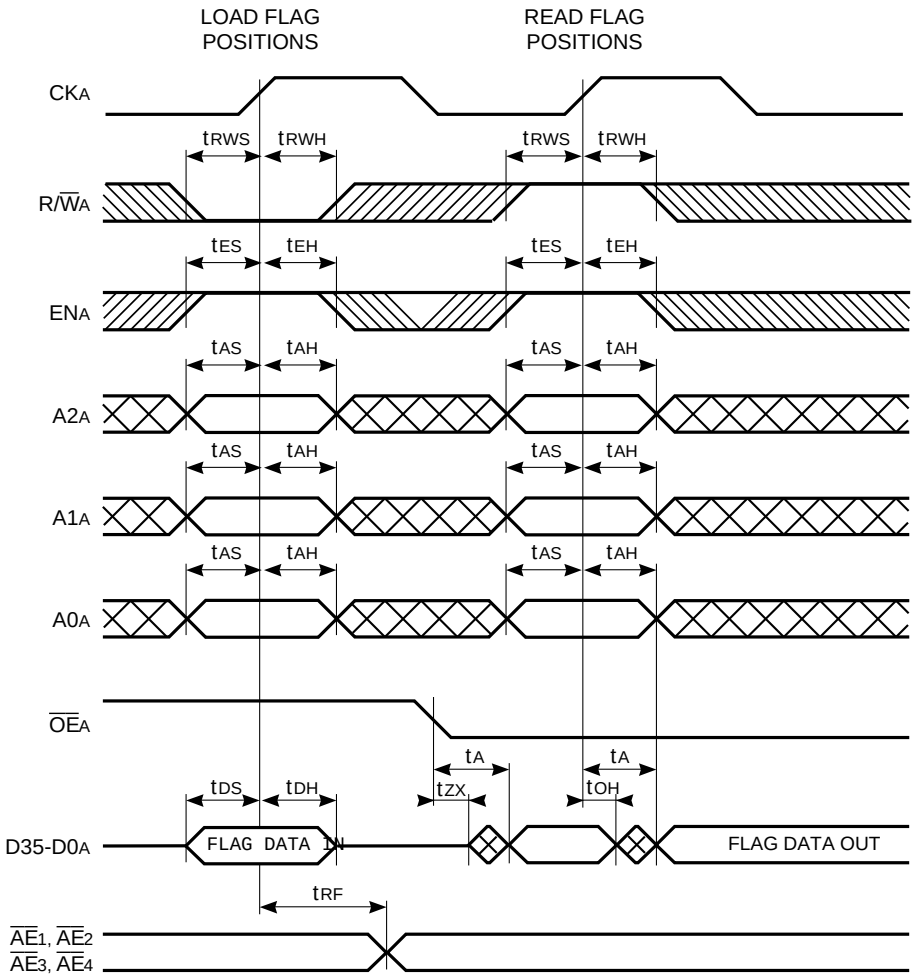
Notes:
1. Both edges of $\overline{MBF}2$ are synchronized to the port A clock, CK_A.
2. Both edges of $\overline{MBF}1$ are synchronized to the port A clock, CK_B.
3. There is a maximum of two CK_B clock cycles of synchronization latency before $\overline{MBF}1$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

FIGURE 13. PORT B MAILBOX ACCESS



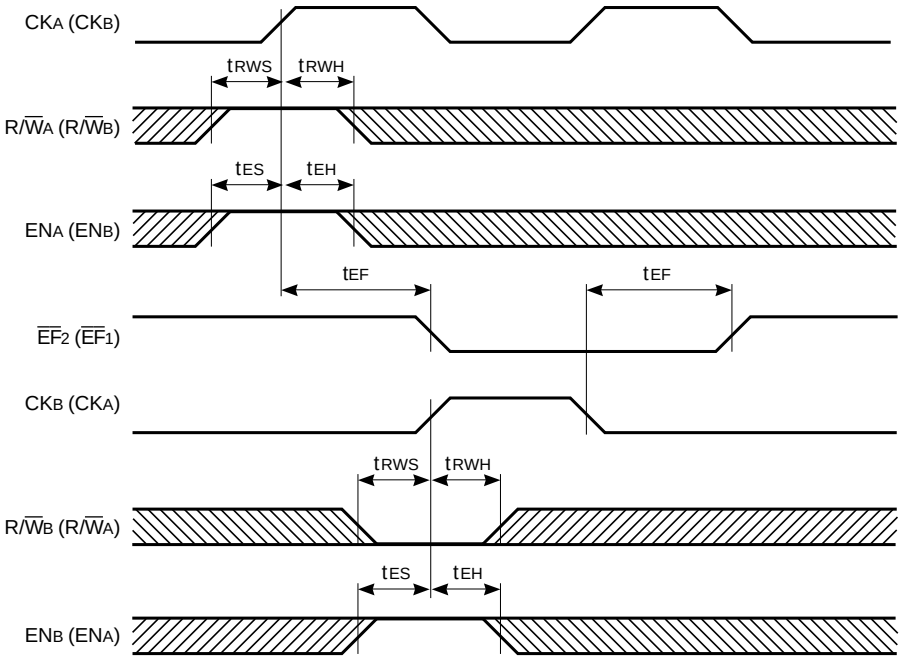
Notes:
1. Both edges of $\overline{MBF}2$ are synchronized to the port A clock, CK_A.
2. Both edges of $\overline{MBF}1$ are synchronized to the port A clock, CK_B.
3. There is a maximum of two CK_A clock cycles of synchronization latency before $\overline{MBF}2$ is asserted to indicate valid new mailbox data. If CK_B and CK_A are identical there is a maximum of one clock cycle.
4. The status of mailbox flags does not prevent mailbox read or write operations.

FIGURE 14. FLAG PROGRAMMING



Notes:
1. For valid flag address codes and data formats, see flag programming words table.
2. If flag status is altered by flag programming, the updated flags will be valid within the time t_{RF}.
3. The control register may be loaded as shown here, with A2A, A1A, A0A = HLL.
   However, it is not available for reading back.

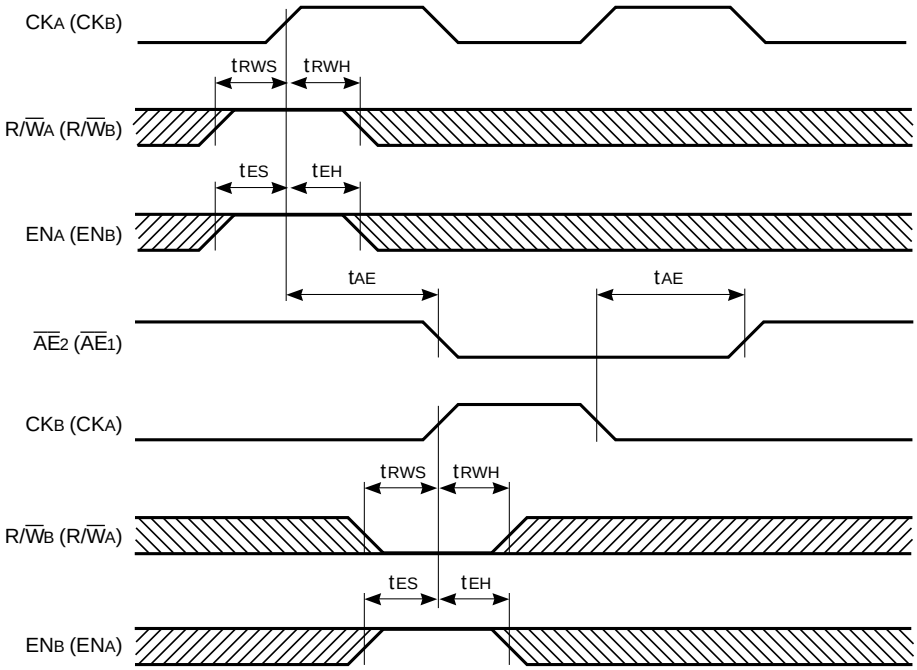
FIGURE 15. EMPTY FLAG TIMING



Notes:
1. A2A, A1A, A0A, and A0B all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. Parameters without parentheses apply to FIFO #2 operation.
   Parameters with parentheses apply to FIFO #1 operation.

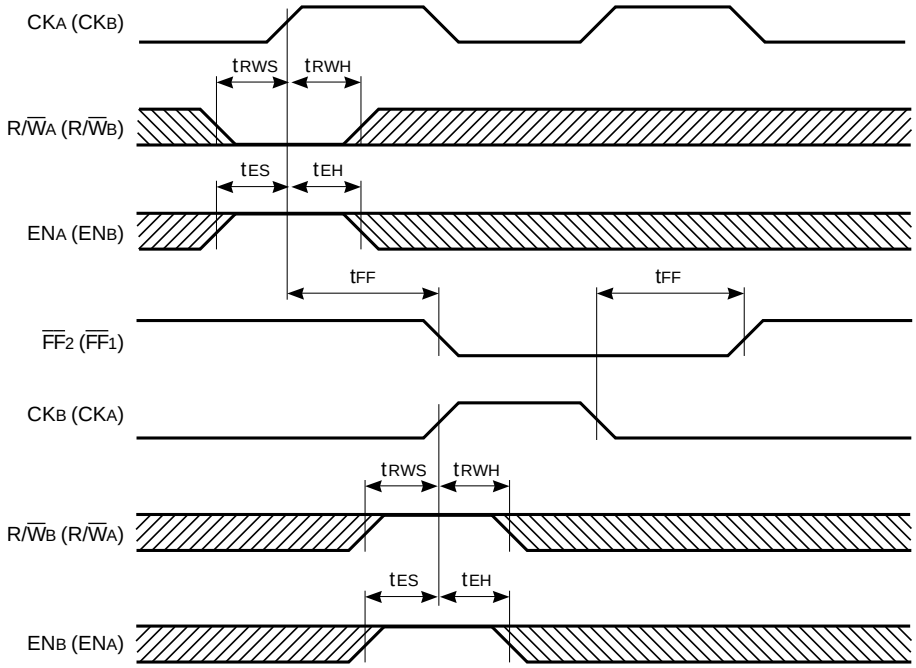
5

FIGURE 16. ALMOST-EMPTY FLAG TIMING



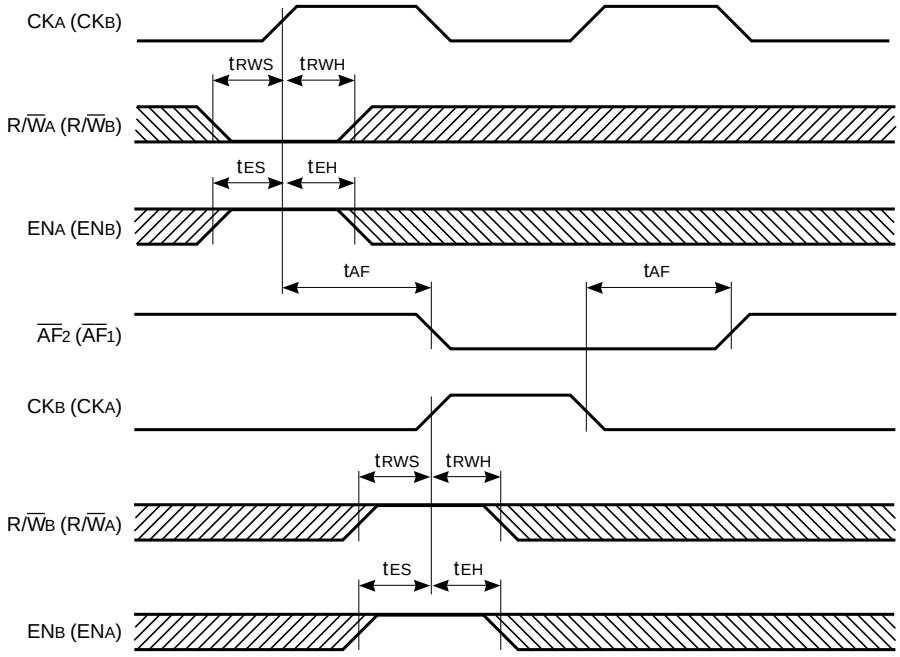
Notes:
1. A2A, A1A, A0A, and A0B all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. Parameters without parentheses apply to FIFO #2 operation.
   Parameters with parentheses apply to FIFO #1 operation.

FIGURE 17. FULL FLAG TIMING



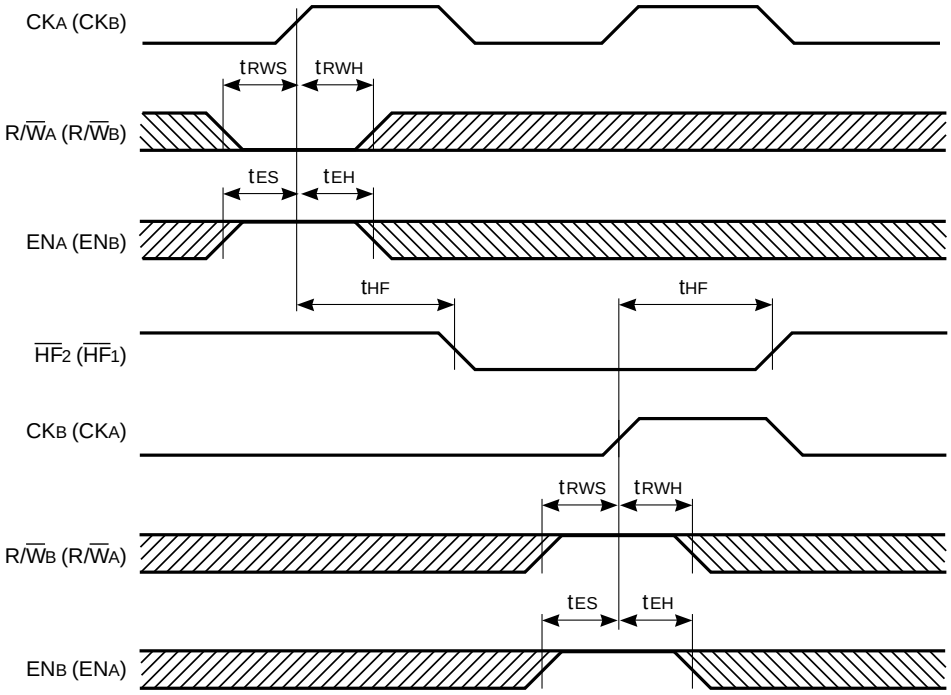
Notes:
1. A2A, A1A, and A0A all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. Parameters without parentheses apply to FIFO #1.
   Parameters with parentheses apply to FIFO #2.

FIGURE 18. ALMOST-FULL FLAG TIMING



Notes:
1. A2A, A1A, and A0A all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. Parameters without parentheses apply to FIFO #1.
   Parameters with parentheses apply to FIFO #2.

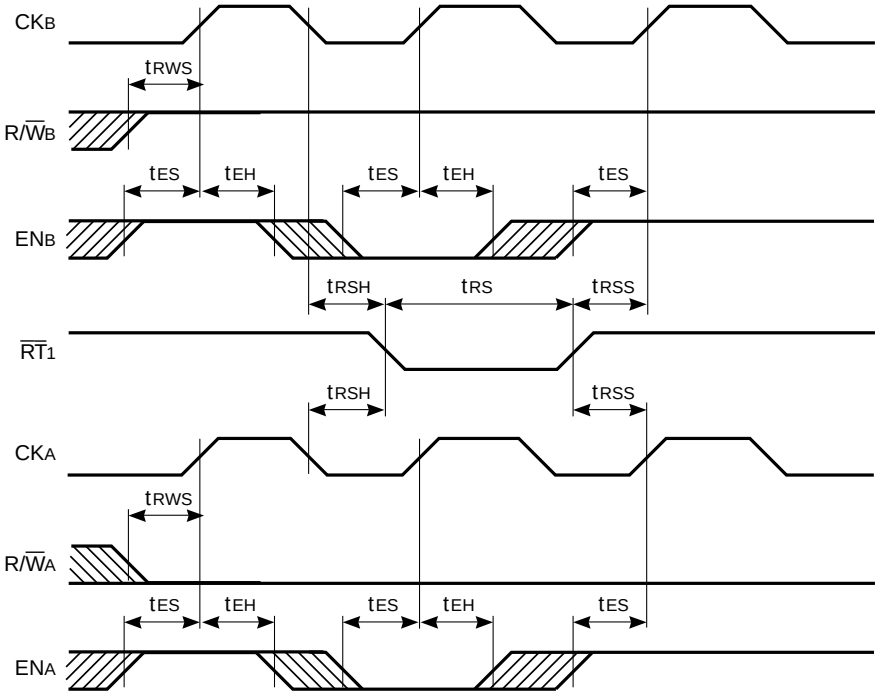
FIGURE 19. HALF-FULL FLAG TIMING



Notes:
1. A2A, A1A, and A0A all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. Parameters without parentheses apply to FIFO #1.
   Parameters with parentheses apply to FIFO #2.

5

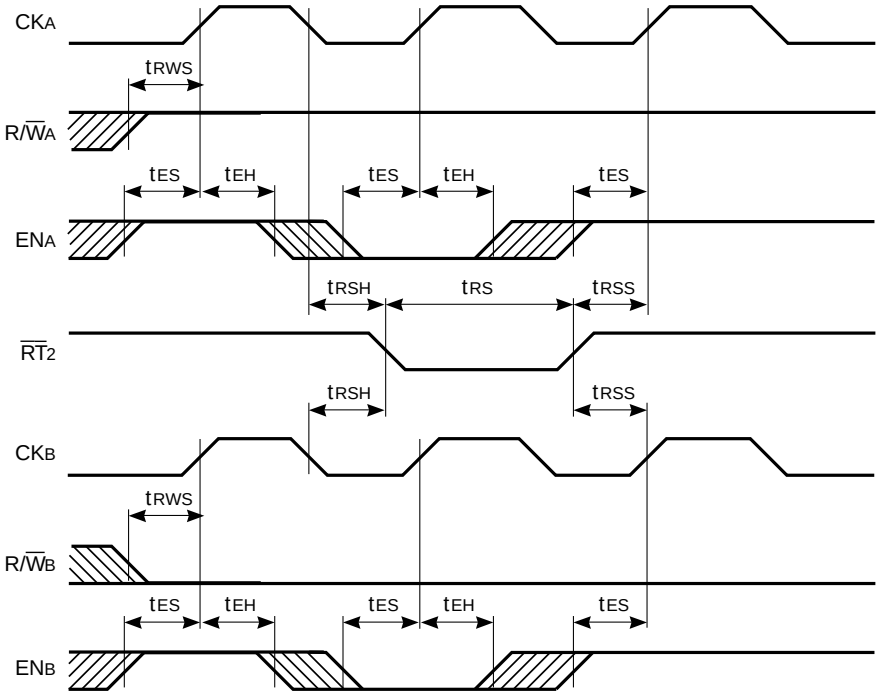
FIGURE 20. FIFO #1 RETRANSMIT TIMING



Notes:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while the clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}1$ after a normal FIFO cycle.
4. Read write operations to FIFO #1 should be disabled while $\overline{RT}1$ is being asserted.

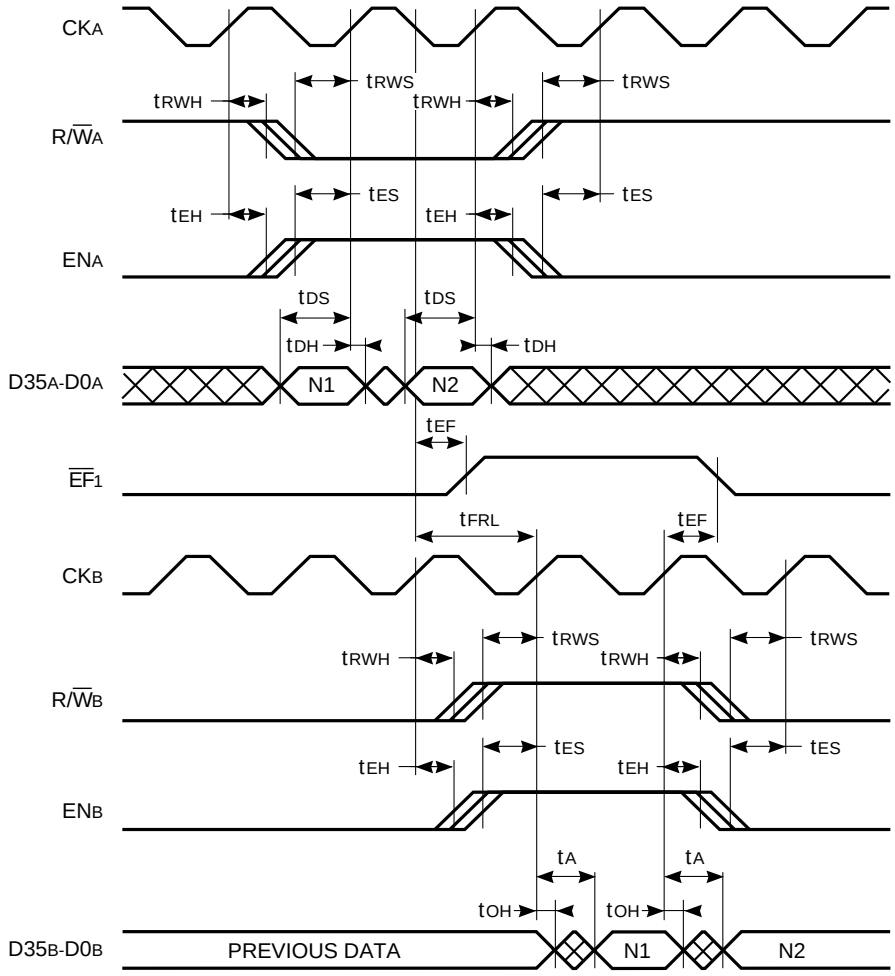
FIGURE 21. FIFO #2 RETRANSMIT TIMING



Notes:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while the clock is enabled.
2. t_{RSS} is the time needed to de-assert $\overline{RT}2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}2$ after a normal FIFO cycle.

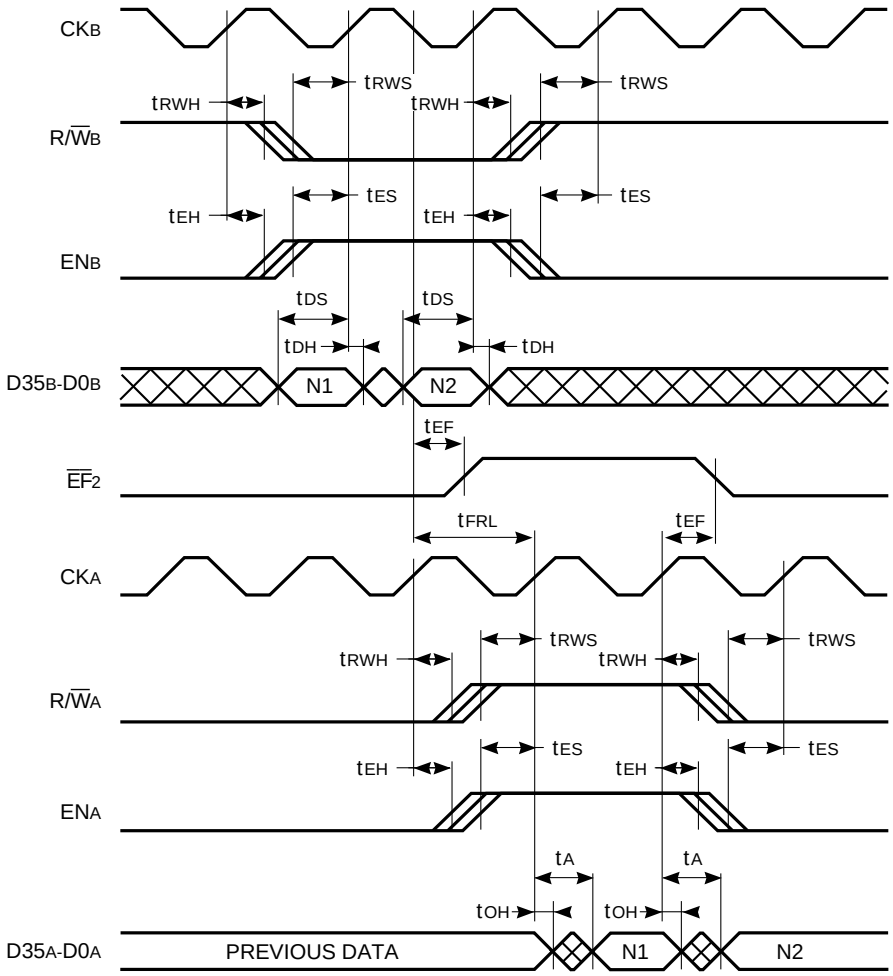
FIGURE 22. FIFO #1 WRITE AND READ OPERATION IN NEAR-EMPTY REGION



Notes:

1. A2A, A1A, A0A, and A0B all are held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (first-read latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

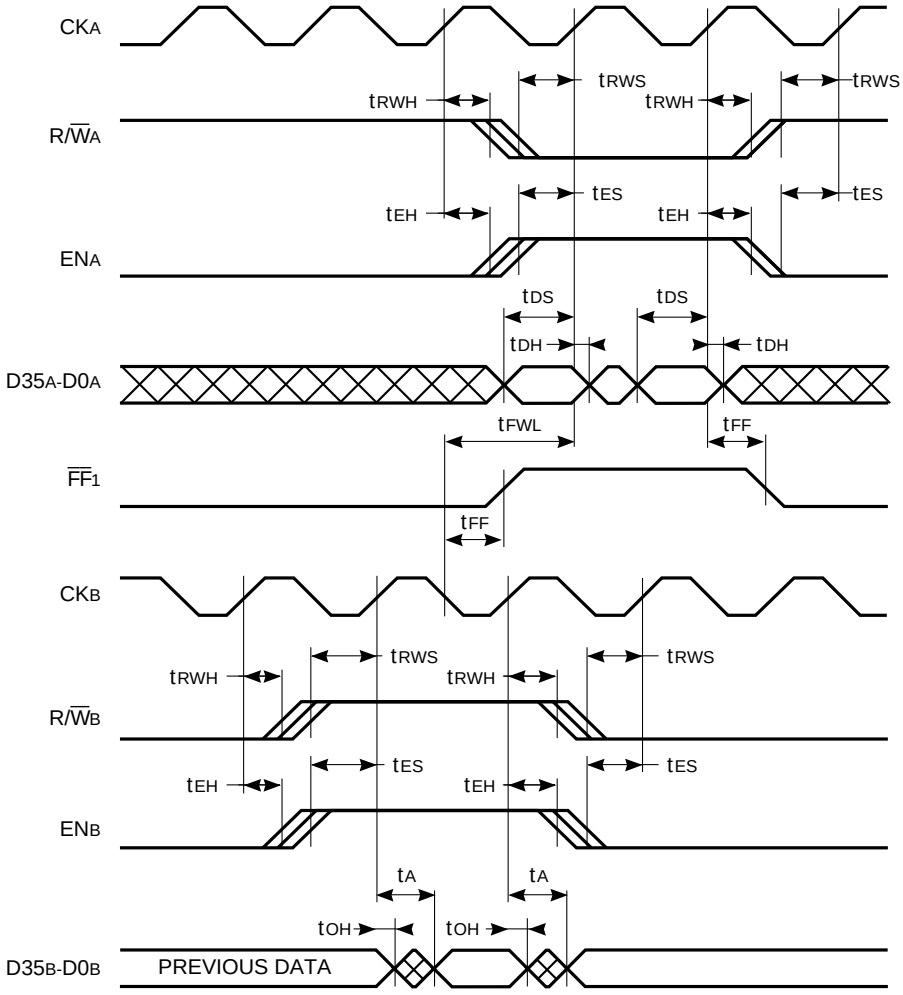
FIGURE 23. FIFO #2 WRITE AND READ OPERATION IN NEAR-EMPTY REGION



Notes:

1. A2A, A1A, A0A, and A0B all are held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (first-read latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

FIGURE 24. FIFO #1 WRITE AND READ OPERATION IN NEAR-FULL REGION

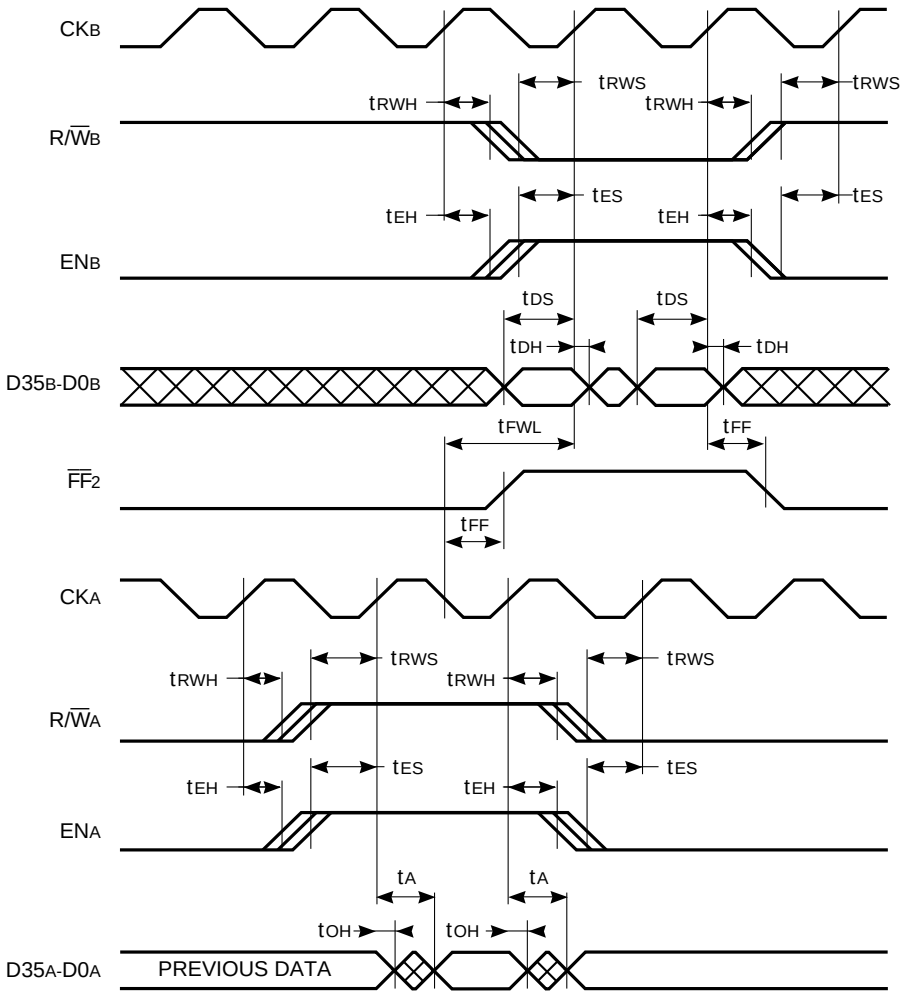


Notes:

1. A2A, A1A, A0A, and A0B all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (first-write latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5

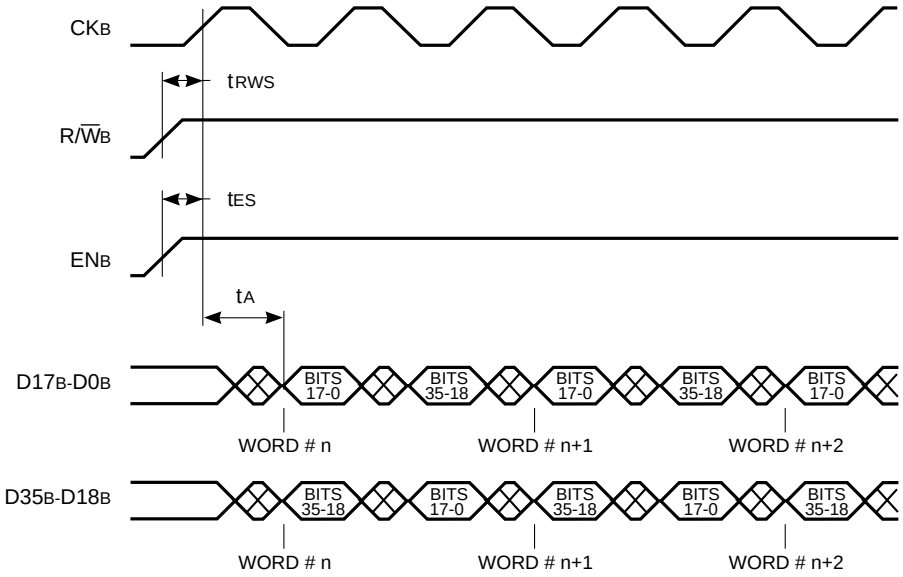
FIGURE 25. FIFO #2 WRITE AND READ OPERATION IN NEAR-FULL REGION



Notes:

1. A2A, A1A, A0A, and A0B all are held HIGH for FIFO access at port A.
   A0B is held HIGH for FIFO access at port B.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (first-write latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

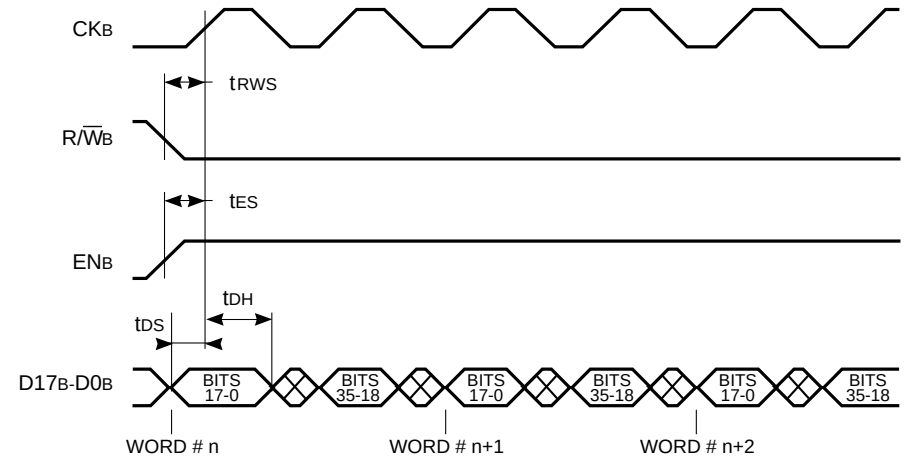
FIGURE 26. PORT B DOUBLE-BYTE FIFO #1 READ ACCESS FOR 36-TO-18 FUNNELING



Notes:
1. A0B is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS0 is held HIGH and WS1 is held LOW for double-byte access.

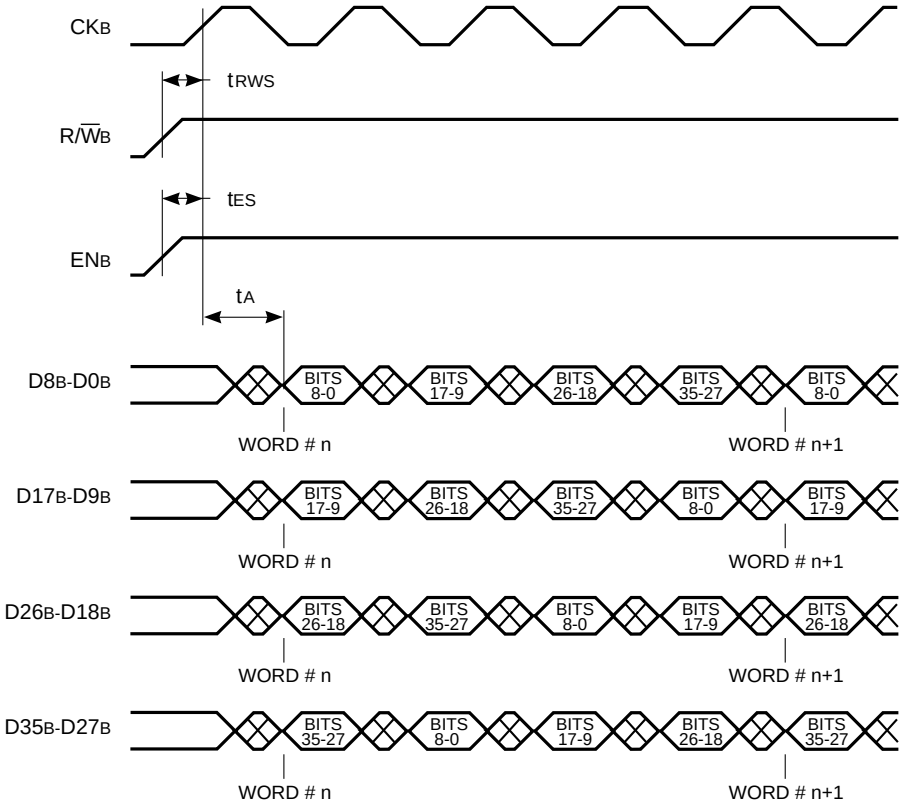
5

FIGURE 27. DOUBLE-BYTE FIFO #2 WRITE ACCESS FOR 18-TO-36 DEFUNNELING



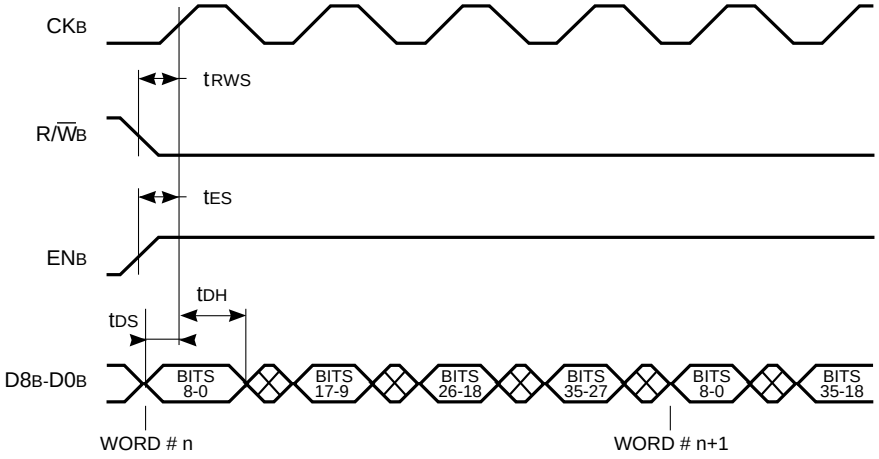
Notes:
1. A0B is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS0 is held HIGH and WS1 is held LOW for double-byte access.

FIGURE 28. PORT B SINGLE-BYTE FIFO #1 READ ACCESS FOR 9-TO-36 DEFUNNELING



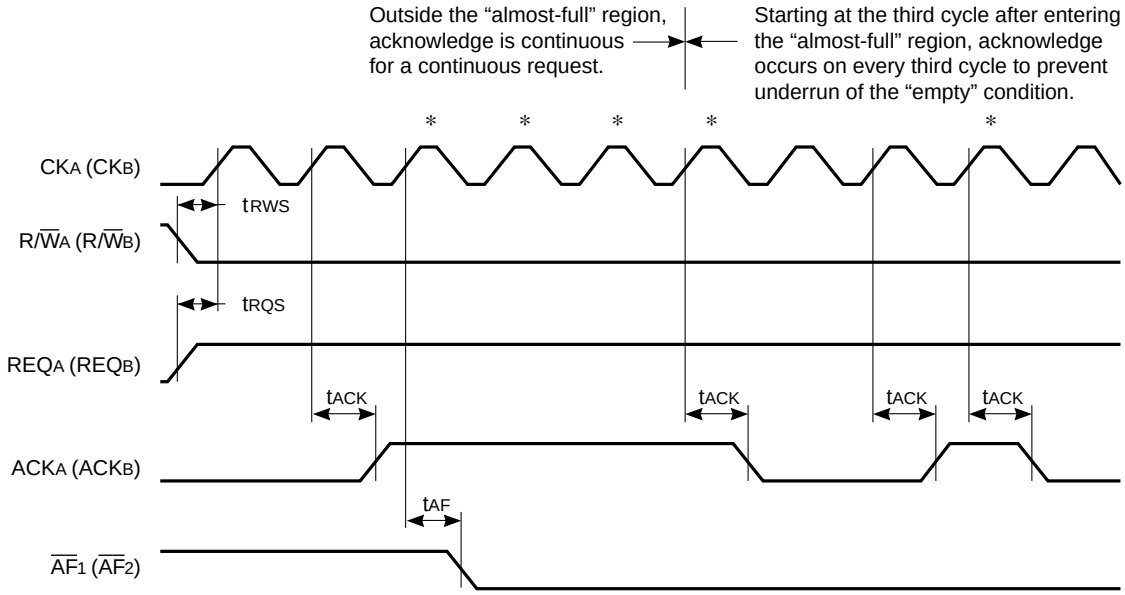
Notes:
1. A0B is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS0 and WS1 both are held LOW for single-byte access.

FIGURE 29. PORT B SINGLE-BYTE FIFO #2 WRITE ACCESS FOR 9-TO-36 DEFUNNELING



Notes:
1. A0B is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS0 and WS1 both are held LOW for single-byte access.

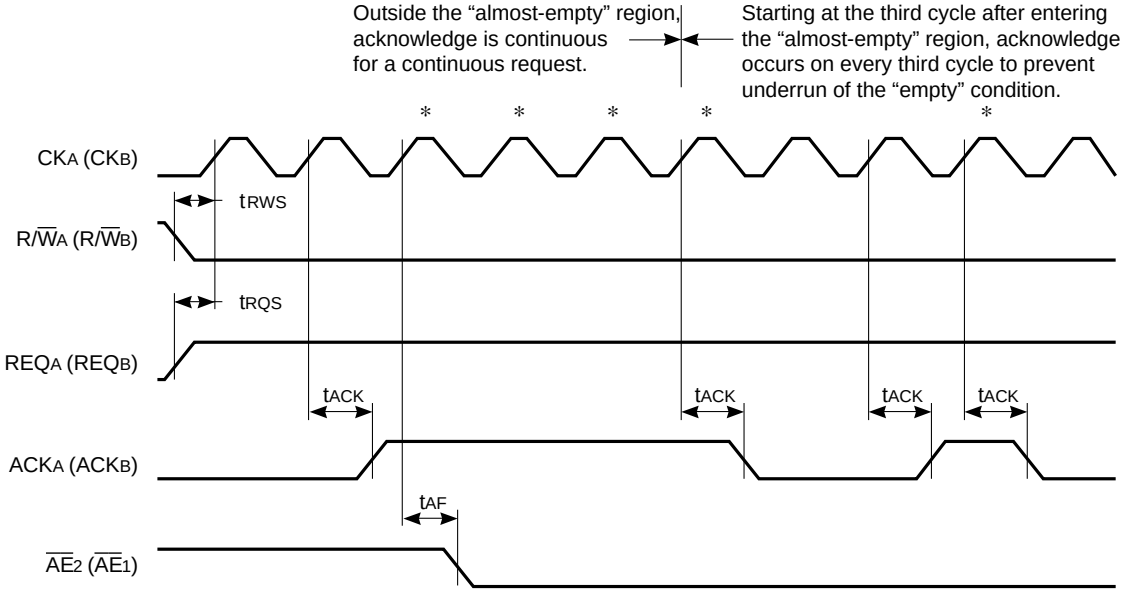
FIGURE 30. WRITE REQUEST/ACKNOWLEDGE HANDSHAKE



Notes:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.
5. Parameters without parentheses apply to port A. Parameters with parentheses apply to port B.

5

FIGURE 31. READ REQUEST/ACKNOWLEDGE HANDSHAKE



Notes:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.
5. Parameters without parentheses apply to port A. Parameters with parentheses apply to port B.

ORDERING INFORMATION

Example: