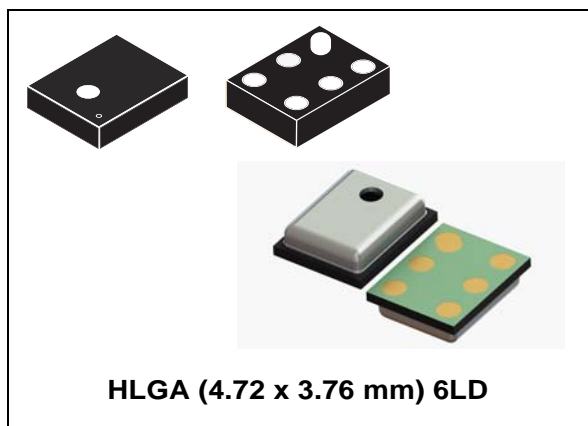


## MEMS audio sensor omnidirectional digital microphone

Datasheet - production data



### Features

- Single supply voltage
- Low power consumption
- 120 dB SPL acoustic overload point
- Omnidirectional sensitivity
- PDM single-bit output with option for stereo configuration
- HLGA package (SMD-compliant) plastic or metal
- ECOPACK®, RoHS, and “Green” compliant

### Applications

- Mobile terminals
- Laptop and notebook computers
- Portable media players
- VoIP

- Speech recognition
- A/V eLearning devices
- Gaming and virtual reality input devices
- Digital still and video cameras
- Antitheft systems

### Description

The MP45DT02 is a compact, low-power, top-port, omnidirectional, digital MEMS microphone. The MP45DT02 is built with a sensing element and an IC interface with stereo capability.

The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process to produce audio sensors.

The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit able to provide a digital signal externally in PDM format.

The MP45DT02 has an acoustic overload point of 120 dB SPL with a best on the market 61 dB signal-to-noise ratio and -26 dB sensitivity.

The MP45DT02 is available in an SMD-compliant package metal (M) or plastic and is guaranteed to operate over an extended temperature range from -30 °C to +85 °C.

The MP45DT02's digital output and package size (1.25 mm thick) make this device the best solution for laptop and portable computing applications.

**Table 1. Device summary**

Order code	Temperature range [°C]	Package	Packing
MP45DT02	-30 to +85	HLGA 4.72 x 3.76 6LD	Tray
MP45DT02TR	-30 to +85	HLGA 4.72 x 3.76 6LD	Tape and reel
MP45DT02TR-M	-30 to +85	HLGA 4.72 x 3.76 6LD	Tape and reel

## Contents

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1 Pin description

Figure 1. Pin connections

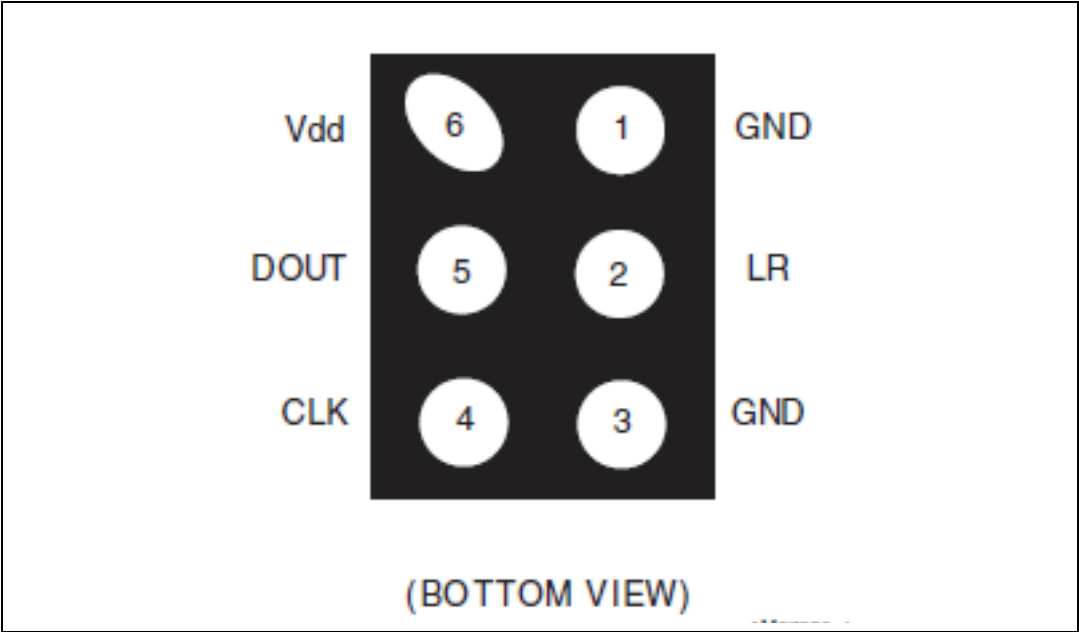


Table 2. Pin description

Pin n°	Pin name	Function
1	GND	0 V supply
2	LR	Left/right channel selection; MIC1 LR is connected to GND or Vdd and MIC2 LR is connected to Vdd or GND (see <a href="#">Figure 5</a> )
3	GND	0 V supply
4	CLK	Synchronization input clock
5	DOUT	Left/right PDM data output
6	Vdd	Power supply

## 2 Acoustic and electrical specifications

### 2.1 Acoustic and electrical characteristics

The values listed in the table below are specified for Vdd = 1.8 V, Clock = 2.4 MHz, T = 25 °C, unless otherwise noted.

**Table 3. Acoustic and electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vdd	Supply voltage		1.64	1.8	3.6	V
Idd	Current consumption in normal mode	No load on data line		0.65		mA
IddPdn	Current consumption in power-down mode <sup>(2)</sup>			20		μA
Sc	Short-circuit current		1		10	mA
AOP	Acoustic overload point			120		dB SPL
So	Sensitivity		-29	-26	-23	dB FS
SNR	Signal-to-noise ratio	A-weighted @ 1 kHz, 1 Pa		61		dB
PSR	Power supply rejection	Guaranteed by design <sup>(3)</sup>		-70		dB FS
Clock	Input clock frequency <sup>(4)</sup>		1	2.4	3.25	MHz
TWK	Wake-up time <sup>(5)</sup>	Guaranteed by design			10	ms
Top	Operating temperature range		-30		+85	°C
V <sub>IOL</sub>	Low level logic input/output voltage	I <sub>out</sub> = 1 mA	-0.3		0.35xVdd	V
V <sub>IOH</sub>	High level logic input/output voltage	I <sub>out</sub> = 1 mA	0.65xVdd		Vdd+0.3	V

1. Typical specifications are not guaranteed.
2. Input clock in static mode.
3. Test signal: 217 Hz square wave, 100 mVpp on Vdd pin.
4. Duty cycle: min = 40% max = 60%.
5. Time from the first clock edge to valid output data.

**Table 4. Distortion specifications**

Parameter	Test condition	Value
Distortion	100 dB SPL (50 Hz - 4 kHz)	< 1% THD + N
Distortion	115 dB SPL (1 kHz)	< 5% THD + N

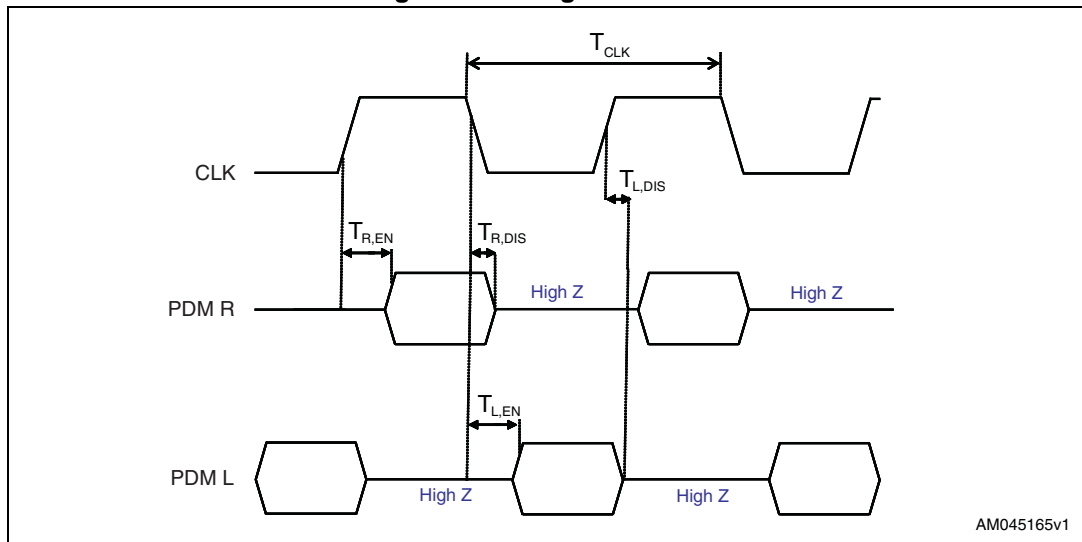
## 2.2 Timing characteristics

Table 5. Timing characteristics

Parameter	Description	Min	Max	Unit
$f_{CLK}$	Clock frequency for normal mode	1	3.25	MHz
$f_{PD}$	Clock frequency for power-down mode		0.23	MHz
$T_{CLK}$	Clock period for normal mode	308	1000	ns
$T_{R,EN}$	Data enabled on DATA line, L/R pin = 1	30 <sup>(1)</sup>		ns
$T_{R,DIS}$	Data disabled on DATA line, L/R pin = 1		16 <sup>(1)</sup>	ns
$T_{L,EN}$	Data enabled on DATA line, L/R pin = 0	30 <sup>(1)</sup>		ns
$T_{L,DIS}$	Data disabled on DATA line, L/R pin = 0		16 <sup>(1)</sup>	ns

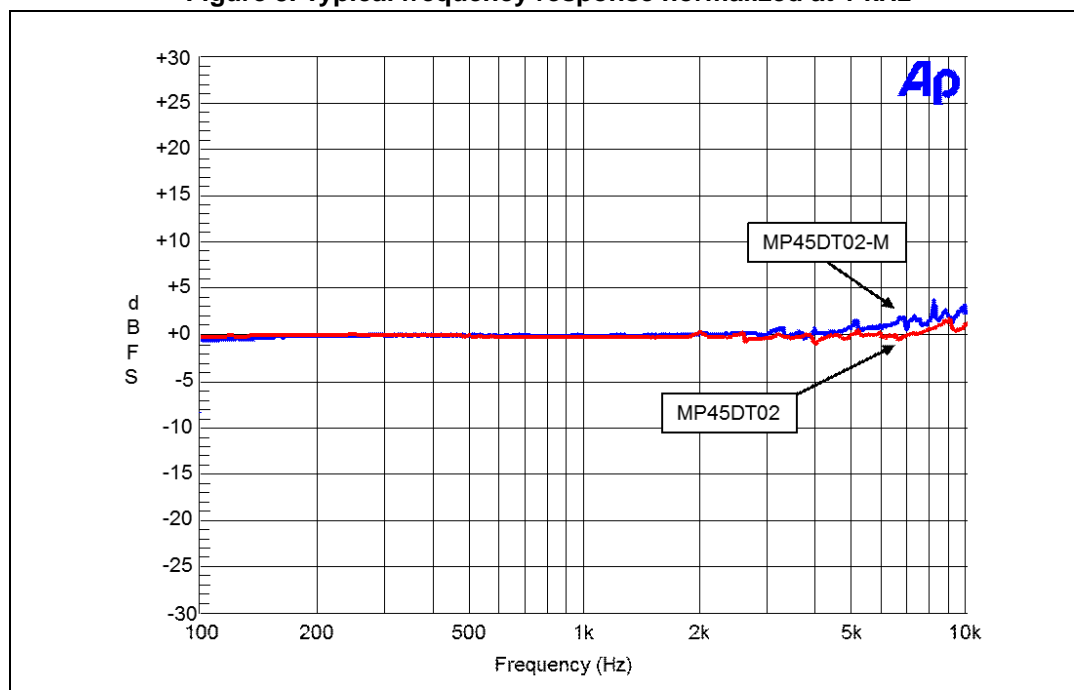
1. From design simulations

Figure 2. Timing waveforms



## 2.3 Frequency response

Figure 3. Typical frequency response normalized at 1 kHz



### 3      **Sensing element**

The sensing element shall mean the acoustic sensor consisting of a conductive movable plate and a fixed plate placed in a tiny silicon chip. This sensor transduces the sound pressure into the changes of coupled capacity between those two plates.

Omron Corporation supplies this element for STMicroelectronics.

## 4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 6. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
V <sub>dd</sub>	Supply voltage	-0.3 to 6	V
V <sub>in</sub>	Input voltage on any control pin	-0.3 to V <sub>dd</sub> +0.3	V
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is ESD-sensitive, improper handling can cause permanent damage to the part.



## 5 Functionality

### 5.1 L/R channel selection

The L/R digital pad lets the user select the DOUT signal pattern as explained in [Table 7](#). The L/R pin must be connected to Vdd or GND.

**Table 7. L/R channel selection**

L/R	CLK low	CLK high
GND	Data valid	High impedance
Vdd	High impedance	Data valid

## 6 Application recommendations

Figure 4. MP45DT02 electrical connections

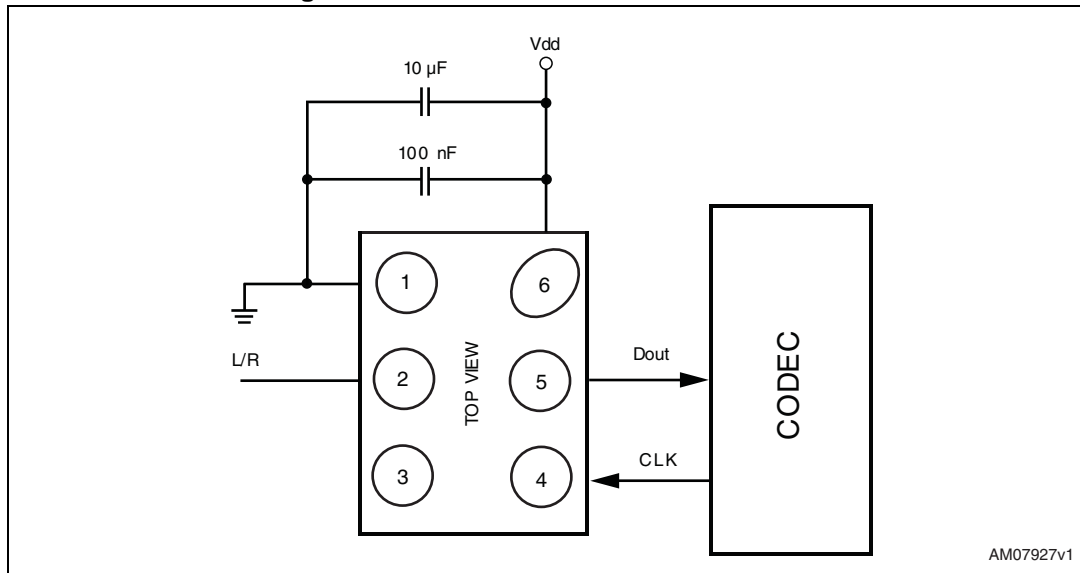
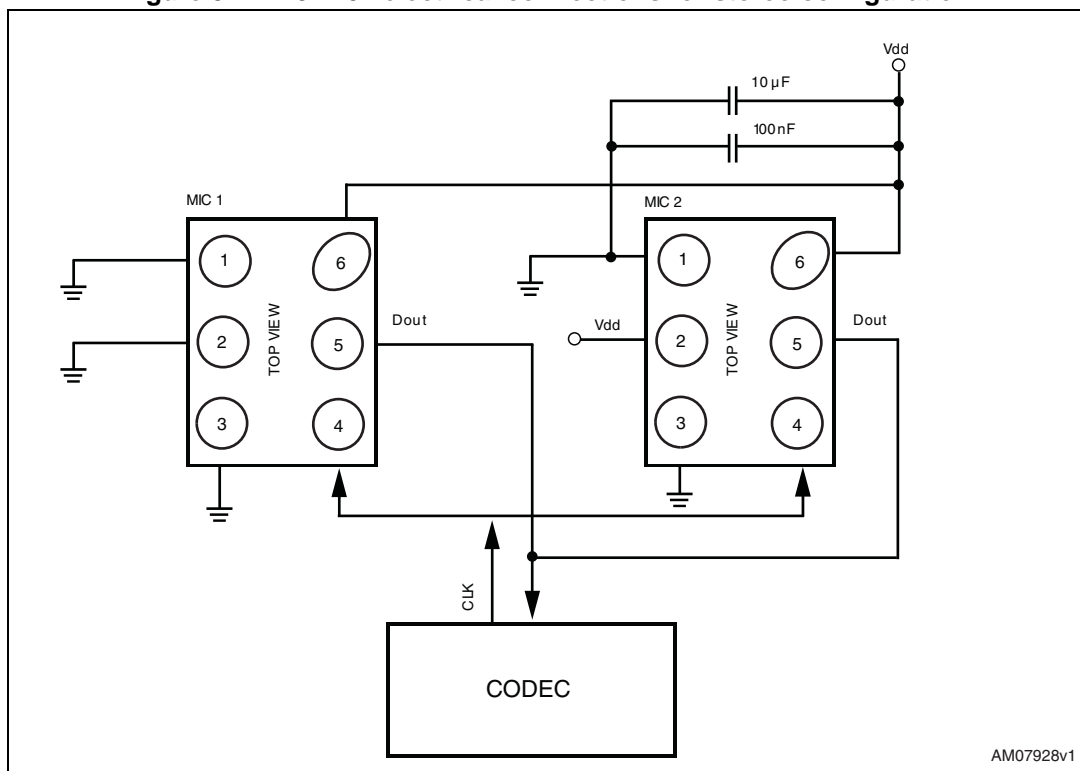


Figure 5. MP45DT02 electrical connections for stereo configuration



Power supply decoupling capacitors (100 nF ceramic, 10 µF ceramic) should be placed as near as possible to pin 6 of the device (common design practice).

The L/R pin must be connected to Vdd or GND (refer to [Table 7](#)).

## 7 Package mechanical data

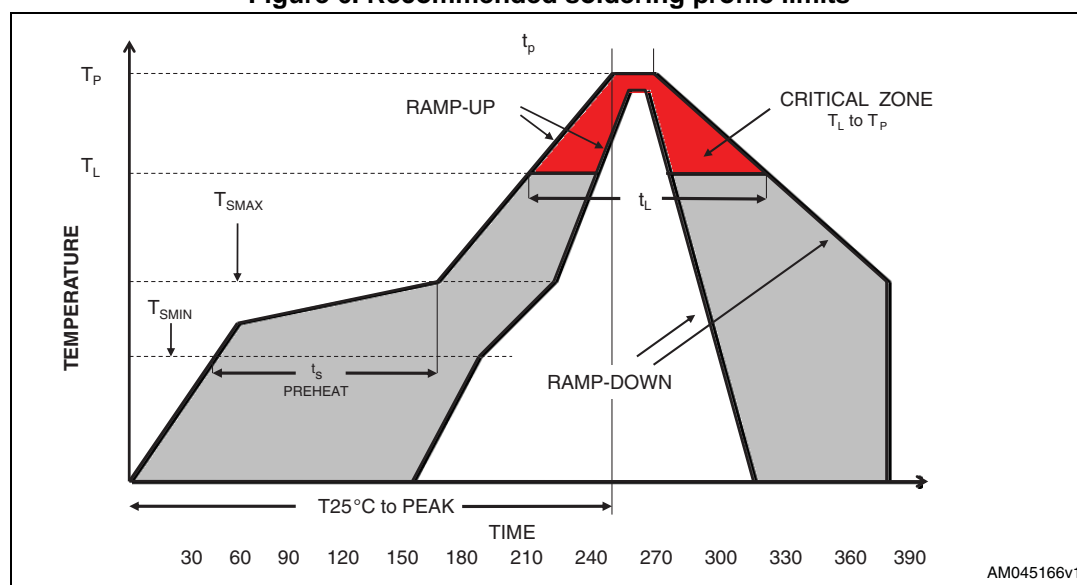
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### Soldering information

The HLGA (4.72 x 3.76 x 1.25) mm package is also compliant with the RoHS and “Green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

Landing pattern and soldering recommendations are available at [www.st.com](http://www.st.com).

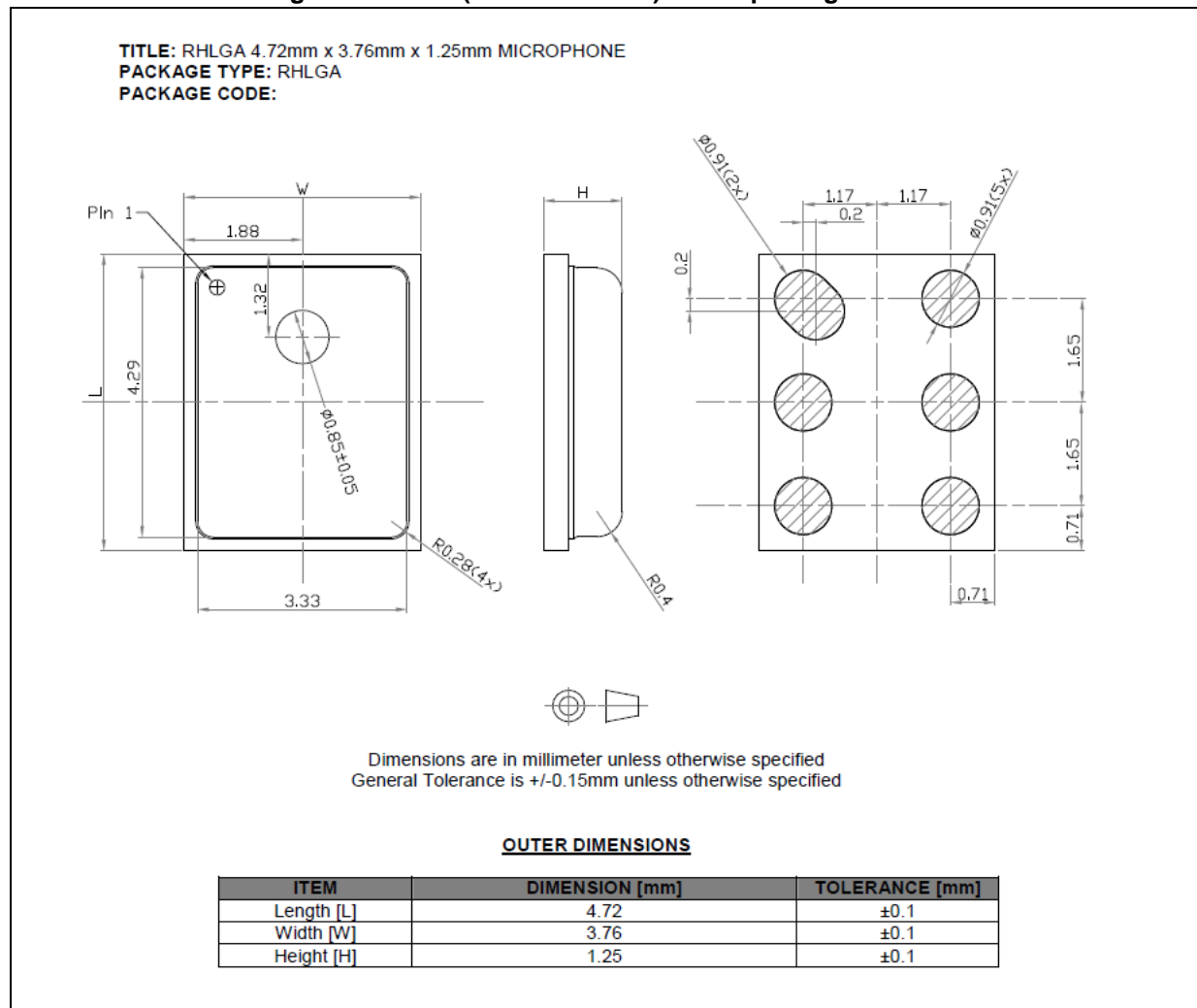
**Figure 6. Recommended soldering profile limits**



**Table 8. Recommended soldering profile limits**

Description	Parameter	Pb free
Average ramp rate	$T_L$ to $T_P$	3 °C/sec max
Preheat		
Minimum temperature	$T_{SMIN}$	150 °C
Maximum temperature	$T_{SMAX}$	200 °C
Time ( $T_{SMIN}$ to $T_{SMAX}$ )	$t_s$	60 sec to 120 sec
Ramp-up rate	$T_{SMAX}$ to $T_L$	
Time maintained above liquidus temperature	$t_L$	60 sec to 150 sec
Liquidus temperature	$T_L$	217 °C
Peak temperature	$T_P$	260 °C max
Time within 5 °C of actual peak temperature		20 sec to 40 sec
Ramp-down rate		6 °C/sec max
Time 25 °C ( $t_{25\text{ °C}}$ ) to peak temperature		8 minutes max

Figure 7. HLGA (4.72 x 3.76 mm) 6-lead package outline



**Note:** The MEMS microphone metal cap can exhibit some level of variation in color when the device is subjected to a thermal process.

Figure 8. HLGA (4.72 x 3.76 mm) 6-lead package outline

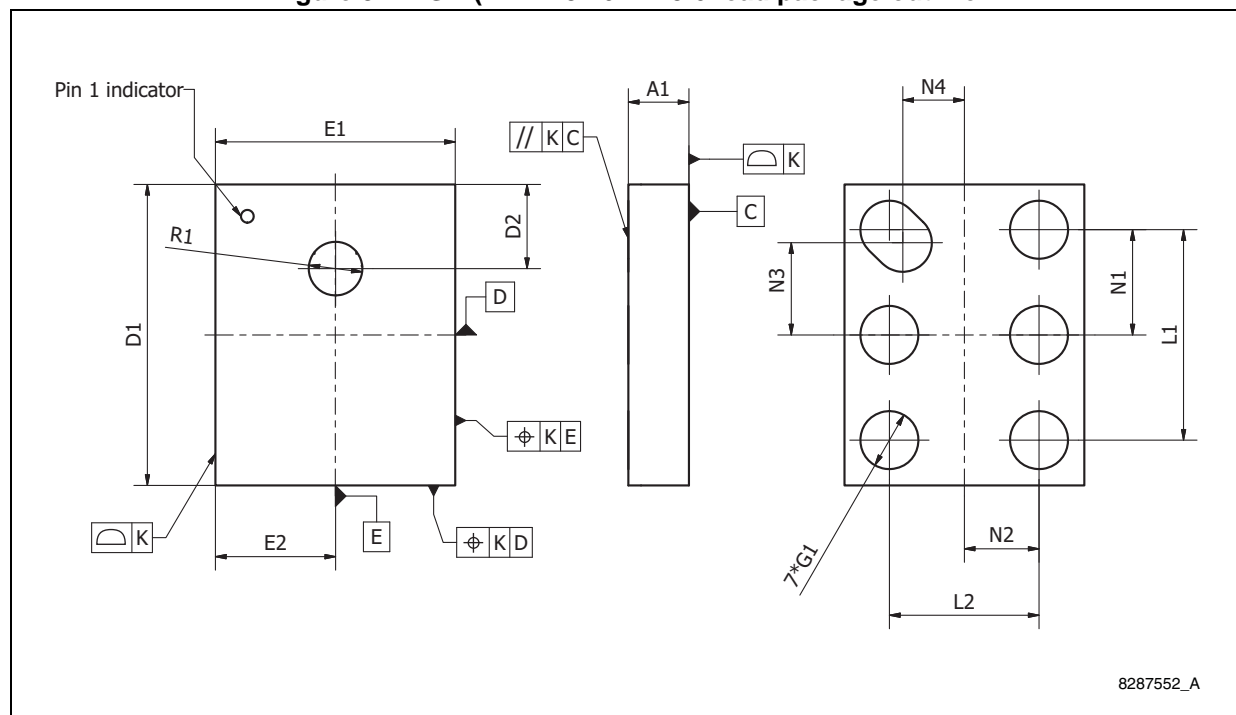


Table 9. HLGA (4.72 x 3.76 mm) 6-lead package dimensions

Symbol	mm.		
	Min.	Typ.	Max.
A1	1.125	1.250	1.375
D1	4.670	4.720	4.770
D2		1.320	
R1	0.750	0.840	0.930
E1	3.710	3.760	3.810
E2		1.880	
L1	3.200	3.300	3.400
L2	2.250	2.350	2.450
N1	1.550	1.650	1.750
N2	1.075	1.175	1.275
N3	1.350	1.450	1.550
N4	0.865	0.965	1.065
G1	0.810	0.910	1.010
K		0.050	

## 8 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
28-Mar-2011	1	Initial release
21-Oct-2011	2	Added max. peak temperature $T_P$ to <a href="#">Table 8</a> Added min. and max. sensitivity $S_o$ to <a href="#">Table 3</a>
01-Mar-2012	3	Document status promoted from preliminary to production data Updated SNR to 61 dB ( <a href="#">Description</a> and <a href="#">Table 3</a> )
07-May-2012	4	Added $V_{IOL}$ , $V_{IOH}$ to <a href="#">Table 3: Acoustic and electrical characteristics</a>
05-Jul-2012	5	Added <a href="#">Section 3: Sensing element</a>
21-Mar-2014	6	Added new package <a href="#">Figure 7: HLGA (4.72 x 3.76 mm) 6-lead package outline</a>

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