

### UltraCMOS® RF Digital Step Attenuator, 7-bit, 31.75 dB 50 MHz – 8 GHz

#### Features

- Attenuation options: covers a 31.75 dB range in 0.25 dB, 0.5 dB, or 1.0 dB steps
  - 0.25 dB monotonicity for  $\leq 6$  GHz
  - 0.50 dB monotonicity for  $\leq 7$  GHz
  - 1.00 dB monotonicity for  $\leq 8$  GHz
- Safe attenuation state transitions
- High power handling
  - 31 dBm, Pulsed @ 8 GHz
  - 28 dBm, CW @ 8 GHz
- High linearity: +65 dBm IIP3
- 1.8V control logic compatible
- 105°C operating temperature
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
  - Serial Addressable
- High-attenuation state @ power-up (PUP)
- ESD performance
  - 1.5kV HBM on all pins

#### Product Description

The PE43705 is a 50Ω, HaRP™ technology-enhanced, 7-bit RF Digital Step Attenuator (DSA) designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

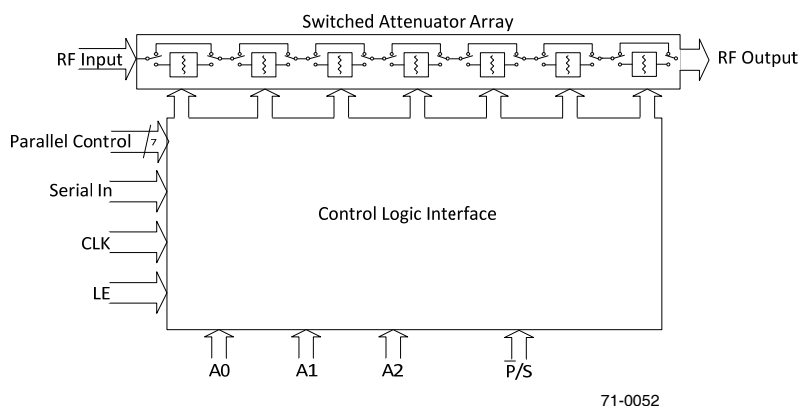
This DSA is a pin-compatible upgraded version of PE43703 with higher power handling and a wider frequency, control voltage and operating temperature range. An integrated digital control interface supports both Serial and Parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up.

Covering a 31.75 dB attenuation range in 0.25 dB, 0.50 dB, or 1 dB steps, it maintains a monotonic step response from 50 MHz through 8 GHz. PE43705 also features safe attenuation state transitions and is offered in a 32-lead 5x5 mm QFN package. In addition, no external blocking capacitors are required if 0V DC is present on the RF ports.

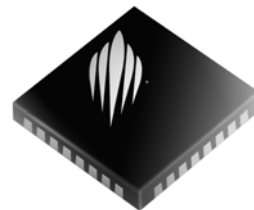
The PE43705 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

**Figure 1. Functional Diagram**



**Figure 2. Package Type**  
32-lead 5x5 mm QFN



**Table 1. Electrical Specifications: 0.25 dB steps @ +25°C,  $V_{DD} = 2.3V$  to  $5.5V$ , ( $Z_S = Z_L = 50\Omega$ ) unless otherwise noted**

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			50		6000	MHz
Attenuation range	0.25 dB step			0 – 31.75		dB
Insertion loss		50 MHz – 2.2 GHz		1.3	1.6	dB
		2.2 GHz – 4 GHz		1.7	2.0	dB
		4 GHz – 6 GHz		2.4	2.8	dB
Attenuation error	0 dB – 15.75 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 3% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 6 GHz			+ (0.2 + 6% of attenuation setting) - (0.15 + 1% of attenuation setting)	dB dB
	16 dB – 31.75 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% of attenuation Setting) - (0.1 + 1.5% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 4% of attenuation Setting) - (0.1 + 0.75% of attenuation setting)	dB dB
		>4 GHz – 6 GHz			+ (0.25 + 7.5% of attenuation setting) - (0.2 + 0% of attenuation setting)	dB dB
Return loss	Input port	50 MHz – 4 GHz		20		dB
		4 GHz – 6 GHz		15		dB
Return loss	Output port	50 MHz – 4 GHz		17		dB
		4 GHz – 6 GHz		13		dB
Relative phase	0 dB – 31.75 dB Attenuation settings	50 MHz – 6 GHz		55		deg
Input 0.1dB compression point <sup>1</sup>		50 MHz – 6 GHz		34		dBm
Input IP3	Two tones at +18 dBm, 20 MHz spacing	6 GHz		65		dBm
RF Trise/Tfall	10% / 90% RF			568		ns
Switching time	50% CTRL to 90% or 10% RF			1		µs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to Table 5 for the operating RF input power (50Ω)

**Table 2. Electrical Specifications: 0.5 dB steps @ +25°C,  $V_{DD} = 2.3V$  to  $5.5V$ , ( $Z_S = Z_L = 50\Omega$ ) unless otherwise noted**

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			50		7000	MHz
Attenuation range	0.5 dB step			0 – 31.5		dB
Insertion loss		50 MHz – 2.2 GHz		1.3	1.6	dB
		2.2 GHz – 4 GHz		1.7	2.0	dB
		4 GHz – 6 GHz		2.4	2.8	dB
		6 GHz – 7 GHz		2.5	2.9	dB
Attenuation error	0 dB – 15.5 dB Attenuation settings	50 MHz – 2.2 GHz			(0.15 + 1.5% of attenuation setting) - (0.1 + 2% of attenuation setting)	dB
		>2.2 GHz – 4 GHz			(0.15 + 3.5% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB
		>4 GHz – 7 GHz			+ (0.25 + 6% of attenuation setting) - (0.25 + 0% of attenuation setting)	dB
	16 dB – 31.5 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.2 + 1.5% of attenuation setting) - (0.1 + 2% of attenuation setting)	dB
		>2.2 GHz – 4 GHz			(0.2 + 4% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB
		>4 GHz – 7 GHz			+ (0.3 + 7% of attenuation setting) - (0.25 + 2.5% of attenuation setting)	dB
						dB
	Return loss	Input port	50 MHz – 4 GHz		20	
4 GHz – 7 GHz				17		dB
Return loss	Output port	50 MHz – 4 GHz		17		dB
		4 GHz – 7 GHz		15		dB
Relative phase	0 dB – 31.5 dB Attenuation settings	50 MHz – 7 GHz		66		deg
Input 0.1dB compression point <sup>1</sup>		50 MHz – 7 GHz		34		dBm
Input IP3	Two tones at +18 dBm, 20 MHz spacing	6 GHz		65		dBm
RF Trise/Tfall	10% / 90% RF			568		ns
Switching time	50% CTRL to 90% or 10% RF			1		µs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to Table 5 for the operating RF input power (50Ω)

**Table 3. Electrical Specifications: 1 dB steps @ +25°C, V<sub>DD</sub> = 2.3V to 5.5V, (Z<sub>S</sub> = Z<sub>L</sub> = 50Ω) unless otherwise noted**

Parameter	Condition	Frequency	Min	Typ	Max	Unit	
Operating frequency			50		8000	MHz	
Attenuation range	1 dB step			0 - 31		dB	
Insertion loss		50 MHz – 2.2 GHz		1.3	1.6	dB	
		2.2 GHz – 4 GHz		1.7	2.0	dB	
		4 GHz – 6 GHz		2.4	2.8	dB	
		6 GHz – 8 GHz		2.8	3.2	dB	
Attenuation error	0 dB – 15 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB	
		>2.2 GHz – 4 GHz			+ (0.15 + 3.5% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB	
		>4 GHz – 8 GHz			+ (0.3 + 6.5% of attenuation setting) - (0.25 + 2% of attenuation setting)	dB dB	
		50 MHz – 2.2 GHz			+ (0.2 + 1.5% of attenuation setting) - (0.1 + 1.5% of attenuation setting)	dB dB	
	16dB – 31 dB Attenuation settings	>2.2 GHz – 4 GHz				+ (0.2 + 4% of attenuation setting) - (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 8 GHz				+ (0.3 + 7% of attenuation setting) - (0.3 + 4.5% of attenuation setting)	dB dB
		Return loss	Input port	50 MHz – 4 GHz 4 GHz – 8 GHz	20 15		dB dB
		Return loss	Output port	50 MHz – 4 GHz 4 GHz – 8 GHz	17 13		dB dB
Relative phase	0 dB – 31 dB Attenuation settings	50 MHz – 8 GHz		77		deg	
Input 0.1dB compression point <sup>1</sup>		50 MHz – 8 GHz		34		dBm	
Input IP3	Two tones at +18 dBm, 20 MHz spacing	6 GHz		65		dBm	
RF Trise/Tfall	10% / 90% RF			568		ns	
Switching time	50% CTRL to 90% or 10% RF			1		µs	

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to Table 5 for the operating RF input power (50Ω)

Figure 3. Pin Configuration (Top View)

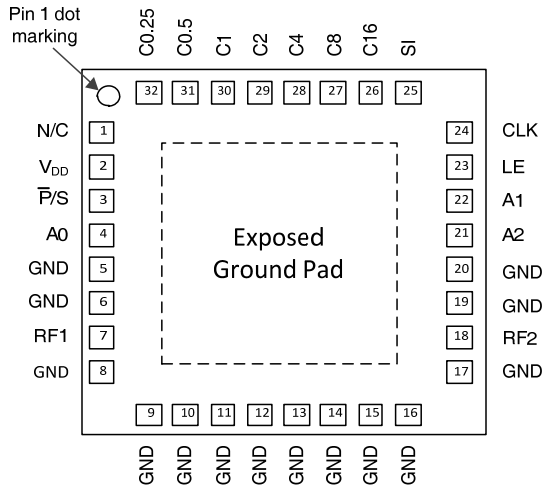


Table 4. Pin Descriptions

Pin #	Pin Name	Description
1	N/C	No connect
2	V <sub>DD</sub>	Supply voltage
3	P/S	Serial/Parallel mode select
4	A0	Address bit A0 connection
5, 6, 8-17, 19, 20	GND	Ground
7	RF1 <sup>1</sup>	RF1 port (RF input)
18	RF2 <sup>1</sup>	RF2 port (RF output)
21	A2	Address bit A2 connection
22	A1	Address bit A1 connection
23	LE	Serial interface latch enable input
24	CLK	Serial interface clock input
25	SI	Serial interface data input
26	C16 (D6) <sup>2</sup>	Parallel control bit, 16 dB
27	C8 (D5) <sup>2</sup>	Parallel control bit, 8 dB
28	C4 (D4) <sup>2</sup>	Parallel control bit, 4 dB
29	C2 (D3) <sup>2</sup>	Parallel control bit, 2 dB
30	C1 (D2) <sup>2</sup>	Parallel control bit, 1 dB
31	C0.5 (D1) <sup>2</sup>	Parallel control bit, 0.5 dB
32	C0.25 (D0) <sup>2</sup>	Parallel control bit, 0.25 dB
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. RF pins 7 and 18 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met  
2. Ground C0.25, C0.5, C1, C2, C4, C8, C16 if not in use

Table 5. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>	2.3		5.5	V
Supply current	I <sub>DD</sub>		130	200	μA
Digital input high	V <sub>IH</sub>	1.17		3.6	V
Digital input low	V <sub>IL</sub>	-0.3		0.6	V
Digital input current	I <sub>CTRL</sub>			15	μA
RF input power, CW	P <sub>MAX,CW</sub>			+28	dBm
RF input power, pulsed <sup>1</sup>	P <sub>MAX,PULSED</sub>			+31	dBm
Operating temperature range	T <sub>OP</sub>	-40		+105	°C

Note 1: Pulsed, 2.5% duty cycle of 4620 μs period, 50Ω

Table 6. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V <sub>DD</sub>	-0.3	5.5	V
Digital input voltage	V <sub>CTRL</sub>	-0.3	3.6	V
Maximum input power	P <sub>MAX,ABS</sub>		+34	dBm
Storage temperature range	T <sub>ST</sub>	-65	150	°C
ESD voltage HBM <sup>1</sup> , all pins	V <sub>ESD,HBM</sub>		1500	V
ESD voltage MM <sup>2</sup> , all pins	V <sub>ESD,MM</sub>		200	V
ESD voltage CDM <sup>3</sup> , all pins	V <sub>ESD,CDM</sub>		250	V

Notes: 1. Human Body Model (MIL-STD 883 Method 3015)  
2. Machine Model (JEDEC JESD22-A115)  
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

### **Safe Attenuation State Transitions**

The PE43705 features a novel architecture to provide safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are prevented during attenuation state changes by optimized internal timing control.

### **Electrostatic Discharge (ESD) Precautions**

When handling this UltraCMOS<sup>®</sup> device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

### **Latch-Up Avoidance**

Unlike conventional CMOS devices, UltraCMOS<sup>®</sup> devices are immune to latch-up.

### **Moisture Sensitivity Level**

The Moisture Sensitivity Level rating for the PE43705 in the 32-lead 5x5 mm QFN package is MSL1.

### **Switching Frequency**

The PE43705 has a maximum 25 kHz switching rate.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

### **Spurious Performance**

The typical low-frequency spurious performance of the PE43705 is -140 dBm.



## Programming Options

### Parallel/Serial Selection

Either a Parallel or Serial Addressable interface can be used to control the PE43705. The P/S bit provides this selection, with  $\overline{P/S}$  = LOW selecting the Parallel interface and  $\overline{P/S}$  = HIGH selecting the Serial Addressable interface.

### Parallel Mode Interface

The Parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 7*.

The Parallel interface timing requirements are defined by *Figure 5* (Parallel Interface Timing Diagram), *Table 13* (Parallel and Direct Interface AC Characteristics) and switching time (*Tables 1-3*).

For Latched Parallel programming, the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (*per Figure 5*) to latch new attenuation state into device.

For Direct Parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

### Serial Interface

The Serial Addressable interface is a 16-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the Attenuation Word, which controls the state of the DSA. The second word is the Address Word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state will remain unchanged. *Figure 4* illustrates an example timing diagram for programming a state. It is required that all parallel control inputs be grounded when the DSA is used in Serial Addressable mode.

The Serial interface is controlled using three CMOS-compatible signals: Serial-In (SI), Clock (CLK), and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first, beginning with the Attenuation Word.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Attenuation Word and Address Word truth tables are listed in *Table 8* and *Table 9*. A programming example of the serial register is illustrated in *Table 10*. The serial timing diagram is illustrated in *Figure 4*.

### Power-up Control Settings

The PE43705 will always initialize to the maximum attenuation setting (31.75 dB) on power-up for both the Serial Addressable and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word. In Direct Parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400  $\mu$ s delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between Serial and Parallel programming modes is possible.

If the DSA powers up in Serial mode ( $\overline{P/S}$  = HIGH), all the parallel control inputs DI[6:0] must be set to logic LOW. Prior to toggling to Parallel mode, the DSA *must* be programmed serially to ensure D[7] is set to logic low.

If the DSA powers up in either Latched or Direct Parallel mode, all parallel pins DI[6:0] must be set to logic LOW prior to toggling to Serial Addressable mode ( $\overline{P/S}$  = HIGH), and *held* low until the DSA has been programmed serially to ensure bit D[7] is set to logic low.

The sequencing is only required once on power-up. Once completed, the DSA may be toggled between Serial and Parallel programming modes at will.



Figure 4. Serial Timing Diagram

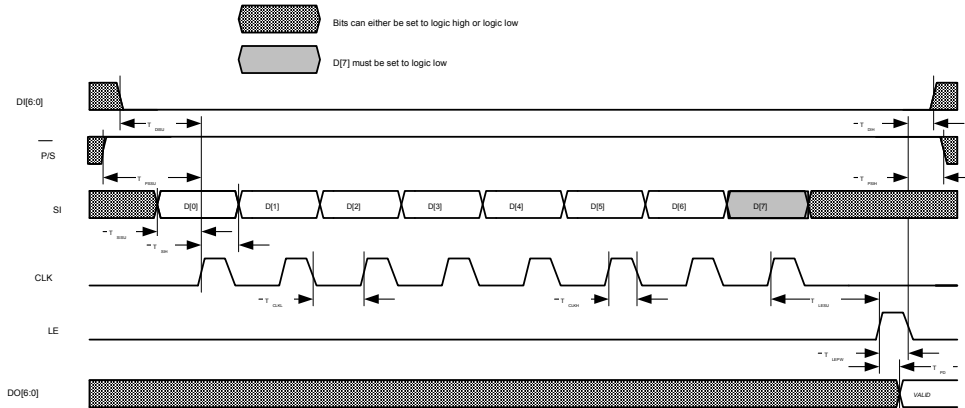


Figure 5. Latched Parallel/Direct Parallel Timing Diagram

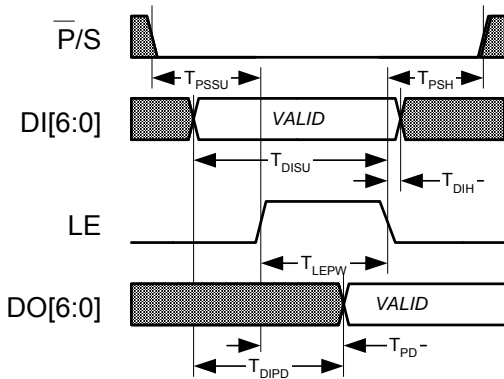


Table 11. Latch and Clock Specifications

Latch Enable	Shift Clock	Function
0	↑	Shift register clocked
↑	X	Contents of shift register transferred to attenuator core

Table 12. Serial Interface AC Characteristics

V<sub>DD</sub> = 3.4V or 5.0V, -40°C < T<sub>A</sub> < 105°C, unless otherwise specified

Parameter	Symbol	Min	Max	Unit
Serial clock frequency	F <sub>CLK</sub>		10	MHz
Serial clock HIGH time	T <sub>CLKH</sub>	30		ns
Serial clock LOW time	T <sub>CLKL</sub>	30		ns
Last serial clock rising edge setup time to Latch Enable rising edge	T <sub>LESU</sub>	10		ns
Latch enable min. pulse width	T <sub>LEPW</sub>	30		ns
Serial data setup time	T <sub>SISU</sub>	10		ns
Serial data hold time	T <sub>SIH</sub>	10		ns
Parallel data setup time	T <sub>DISU</sub>	100		ns
Parallel data hold time	T <sub>DIH</sub>	100		ns
Address setup time	T <sub>ASU</sub>	100		ns
Address hold time	T <sub>AH</sub>	100		ns
Parallel/serial setup time	T <sub>PSSU</sub>	100		ns
Parallel/serial hold time	T <sub>PSH</sub>	100		ns
Digital register delay (internal)	T <sub>PD</sub>		10	ns

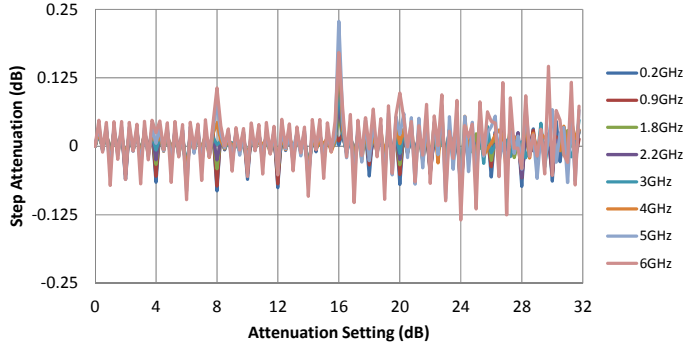
Table 13. Parallel and Direct Interface AC Characteristics

V<sub>DD</sub> = 3.4V or 5.0V, -40°C < T<sub>A</sub> < 105°C, unless otherwise specified

Parameter	Symbol	Min	Max	Unit
Latch enable minimum pulse width	T <sub>LEPW</sub>	30		ns
Parallel data setup time	T <sub>DISU</sub>	100		ns
Parallel data hold time	T <sub>DIH</sub>	100		ns
Parallel/serial setup time	T <sub>PSSU</sub>	100		ns
Parallel/serial hold time	T <sub>PSH</sub>	100		ns
Digital register delay (internal)	T <sub>PD</sub>		10	ns
Digital register delay (internal, direct mode only)	T <sub>DIPD</sub>		5	ns

Typical Performance Data, 0.25 dB Step @ 25°C and V<sub>DD</sub> = 3.3V unless otherwise specified

Figure 6. 0.25 dB Step Attenuation vs. Frequency\*



\* Monotonicity is held so long as step-attenuation does not cross below -0.25 dB

Figure 7. 0.25 dB Step, Actual vs. Frequency

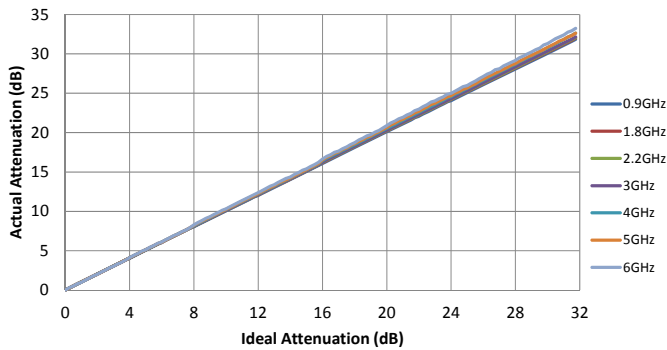


Figure 8. 0.25 dB Major State Bit Error vs. Attenuation Setting

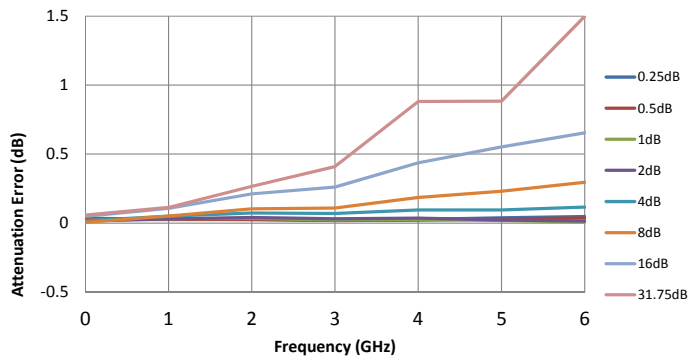
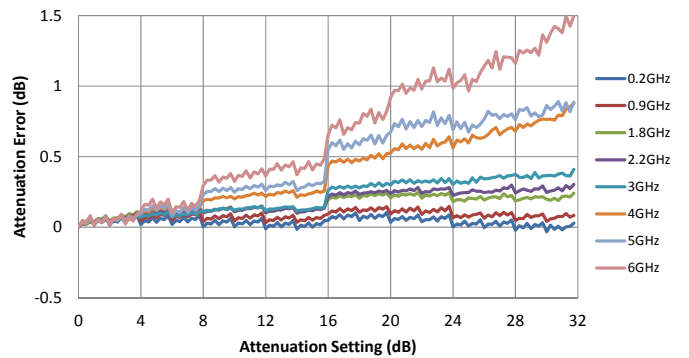
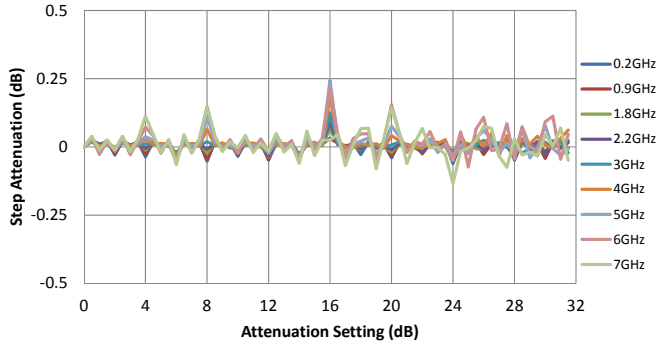


Figure 9. 0.25 dB Attenuation Error vs. Frequency



Typical Performance Data, 0.5 dB Step @ 25°C and  $V_{DD} = 3.3V$  unless otherwise specified

Figure 10. 0.5 dB Step Attenuation vs. Frequency\*



\* Monotonicity is held so long as step-attenuation does not cross below -0.5 dB

Figure 11. 0.5 dB Step, Actual vs. Frequency

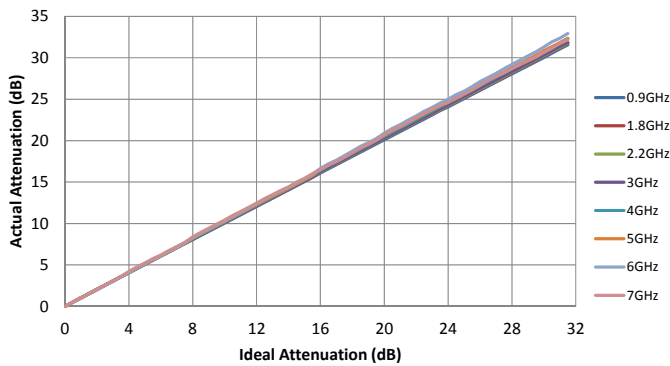


Figure 12. 0.5 dB Major State Bit Error vs. Attenuation Setting

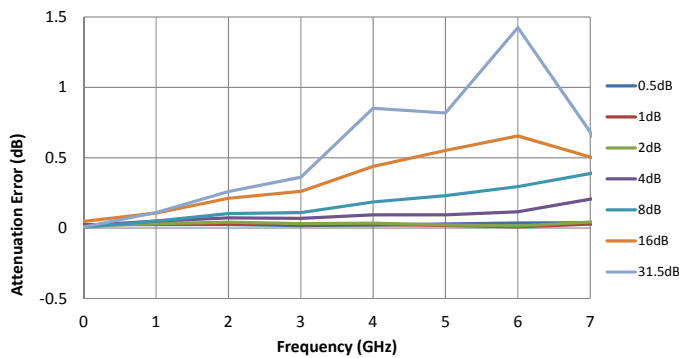
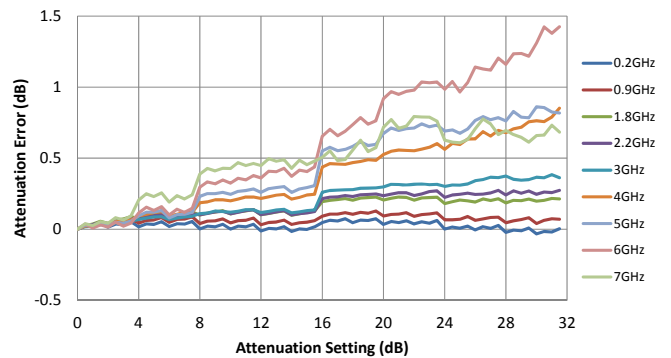
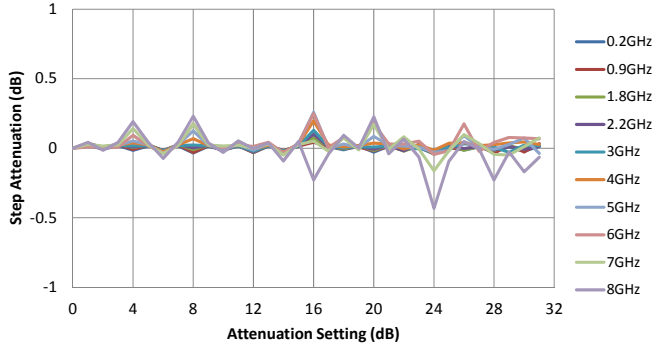


Figure 13. 0.5 dB Attenuation Error vs. Frequency



Typical Performance Data, 1 dB Step @ 25°C and  $V_{DD} = 3.3V$  unless otherwise specified

Figure 14. 1 dB Step Attenuation vs. Frequency\*



\* Monotonicity is held so long as step-attenuation does not cross below -1.0 dB

Figure 15. 1 dB Step, Actual vs. Frequency

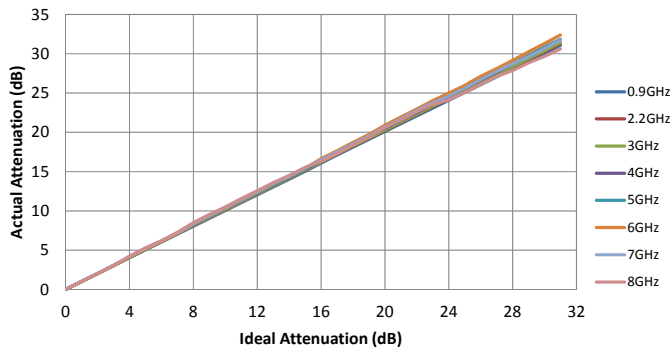


Figure 16. 1 dB Major State Bit Error vs. Attenuation Setting

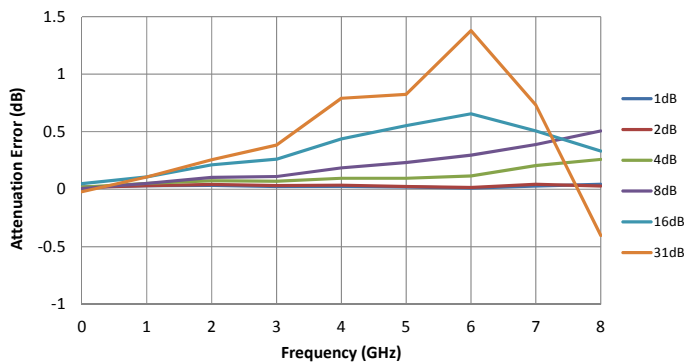
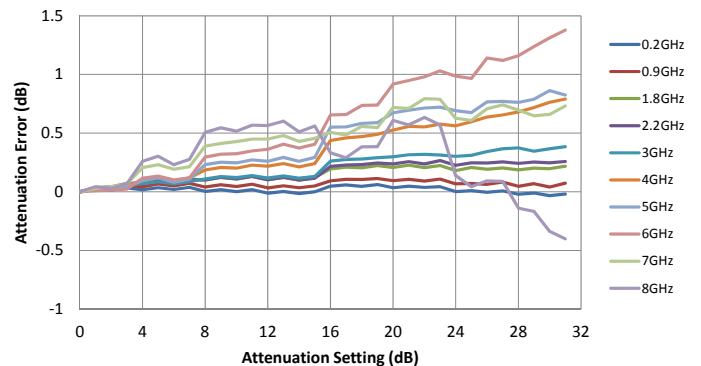


Figure 17. 1 dB Attenuation Error vs. Frequency



Typical Performance Data, 1 dB Step @ 25°C and V<sub>DD</sub> = 3.3V unless otherwise specified

Figure 18. Insertion Loss vs. Temperature

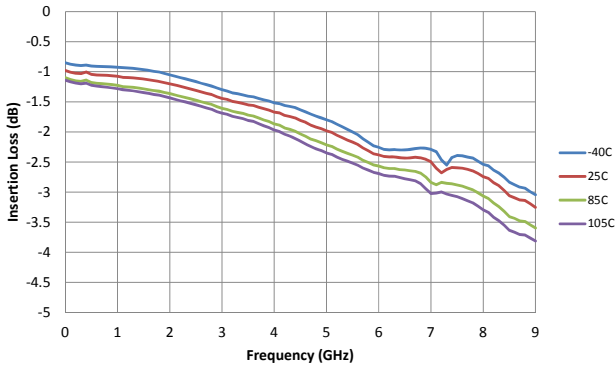


Figure 19. Input Return Loss vs. Attenuation Setting

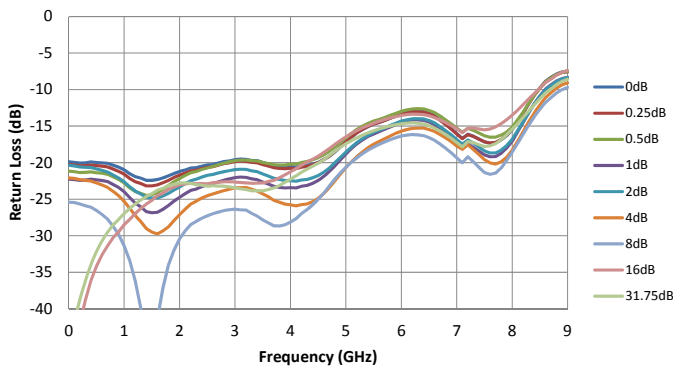


Figure 20. Output Return Loss vs. Attenuation Setting

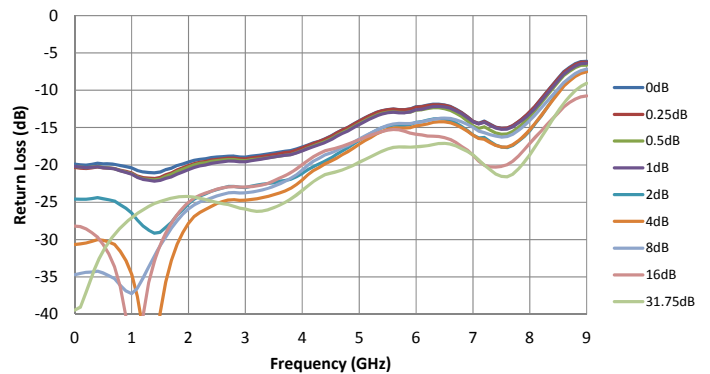


Figure 21. Input Return Loss vs. Temperature for 16 dB Attenuation Setting

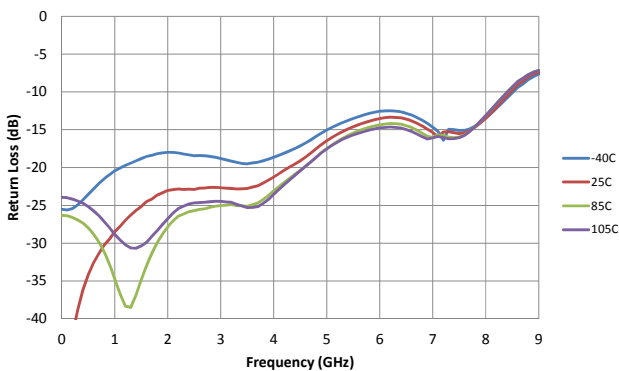
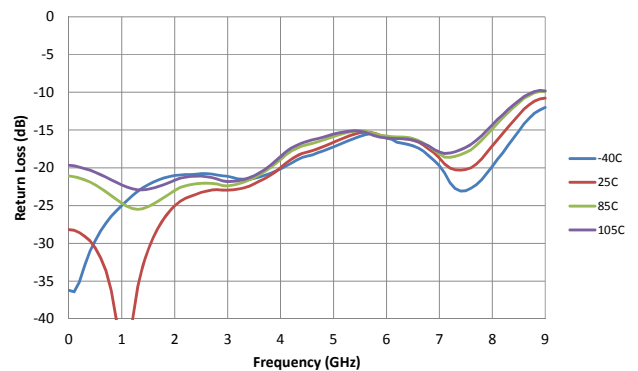


Figure 22. Output Return Loss vs. Temperature for 16 dB Attenuation Setting



Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$  unless otherwise specified

Figure 23. Relative Phase Error vs. Attenuation Setting

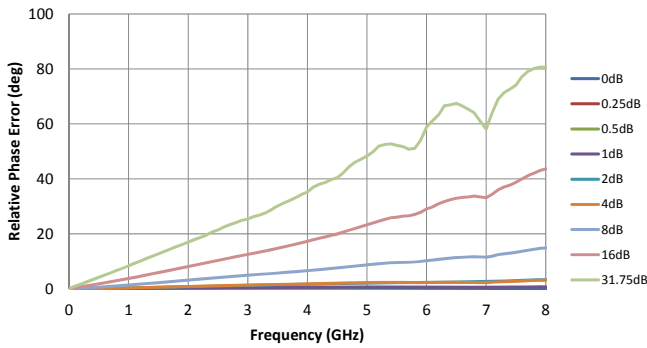


Figure 24. Relative Phase Error for 31.75 dB Attenuation Setting vs. Frequency

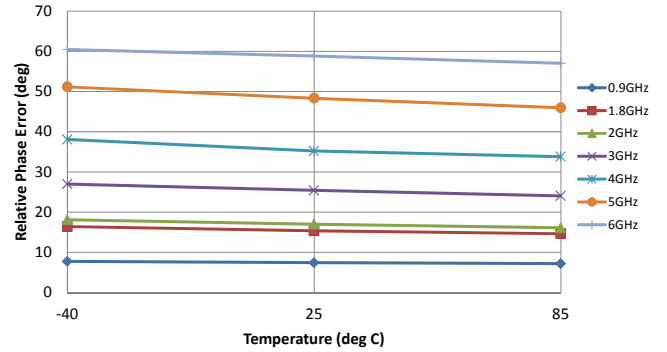


Figure 25. Attenuation Error @ 900 MHz vs. Temperature

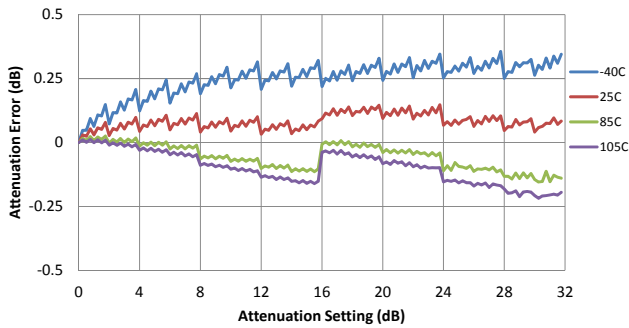


Figure 26. Attenuation Error @ 1800 MHz vs. Temperature

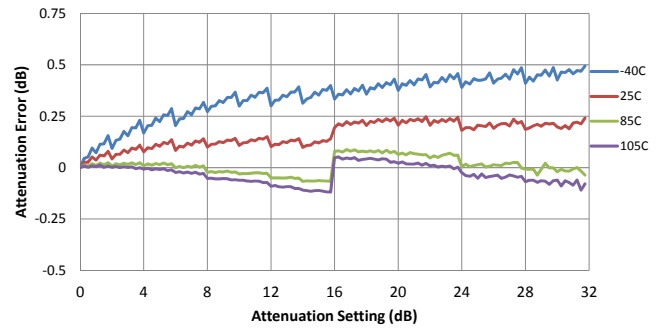


Figure 27. Attenuation Error @ 3000 MHz vs. Temperature

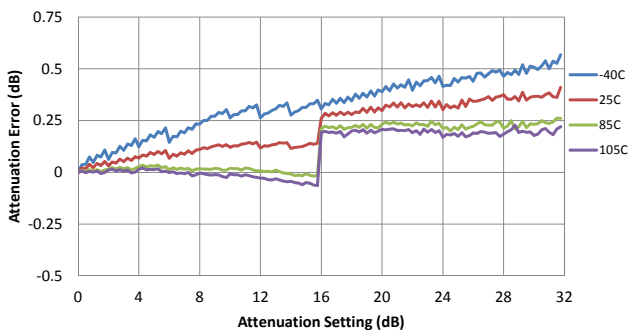
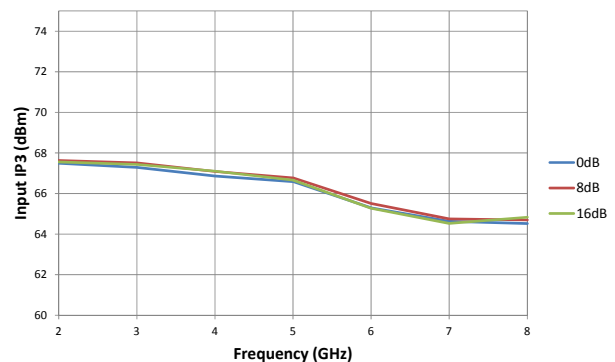


Figure 28. IIP3 vs. Attenuation Setting



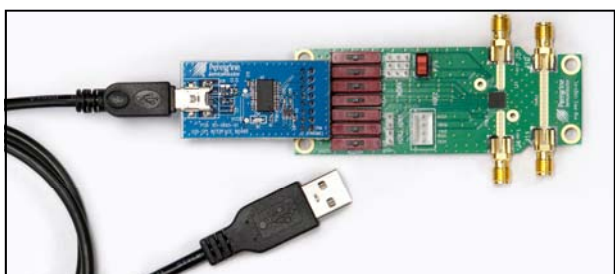
## Evaluation Kit

The Digital Attenuator Evaluation Board (EVB) was designed to ease customer evaluation of the PE43705 Digital Step Attenuator. PE43705 EVB supports Direct Parallel, Latched Parallel, and Serial modes.

### Evaluation Kit Setup

Connect the EVB with the USB dongle board and USB cable as shown in *Figure 29*.

**Figure 29. Evaluation Kit**



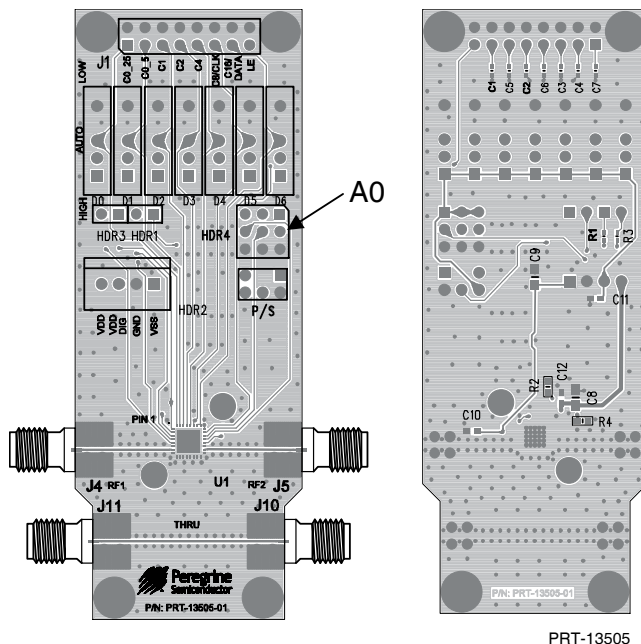
### Direct Parallel Programming Procedure

Direct Parallel programming is suitable for manual operation without software programming. For manual Direct Parallel programming, position the Parallel/Serial (P/S) select switch to the Parallel (or left) position. The LE pin of J1 (pin 15) must be tied to HIGH voltage. Switches D0–D6 are SP3T switches that enable the user to manually program the parallel bits. When D0–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting D0–D6 to the AUTO position presents as OPEN, which is set for software programming of Latched Parallel and Serial mode. *Table 7* depicts the parallel programming truth table.

### Latched Parallel Programming Procedure

For automated Latched Parallel programming, connect the USB dongle board and cable that is provided with the Evaluation Kit (EVK) from the USB port of the PC to the J1 header of the PE43705 EVB, and set the D0–D6 SP3T switches to the AUTO position. Position the Parallel/Serial ( $\bar{P}/S$ ) select switch to the Parallel (or left) position. The evaluation software is written to operate the

**Figure 30. Evaluation Board Layout**

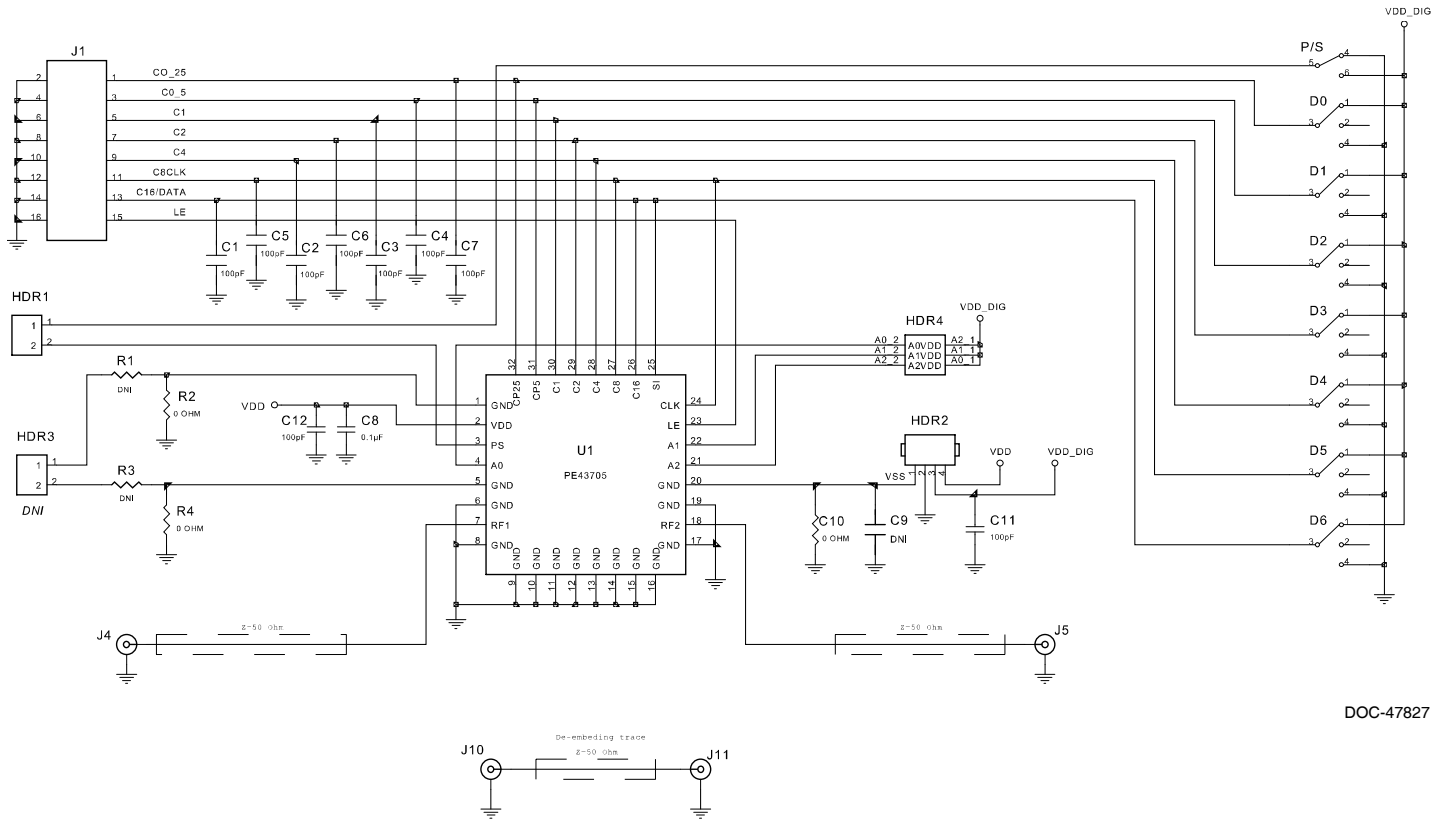


DSA in Parallel mode. Ensure that the software GUI is set to Latched Parallel mode. Use the software GUI to enable the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

### Serial Addressable Programming Procedure

For automated serial programming, connect the USB dongle board and cable that is provided with the Evaluation Kit (EVK) from the USB port of the PC to the J1 header of the PE43705 EVB, and set the D0–D6 SP3T switches to the AUTO toggle position. Position the Parallel/Serial ( $\bar{P}/S$ ) select switch to the Serial (or right) position. Prior to programming, the user must define an address setting using the HDR4 header pin. Jump the middle row of pins on the HDR4 header (A0–A2) to the lower row of pins to set logic LOW, or jump the middle row of pins to the upper row of pins to set logic HIGH. If the HDR4 pins are left open, then 000 becomes the default address. The software GUI is written to operate the DSA in Serial mode. Use the software GUI to enable each setting to the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

**Figure 31. Evaluation Board Schematic**

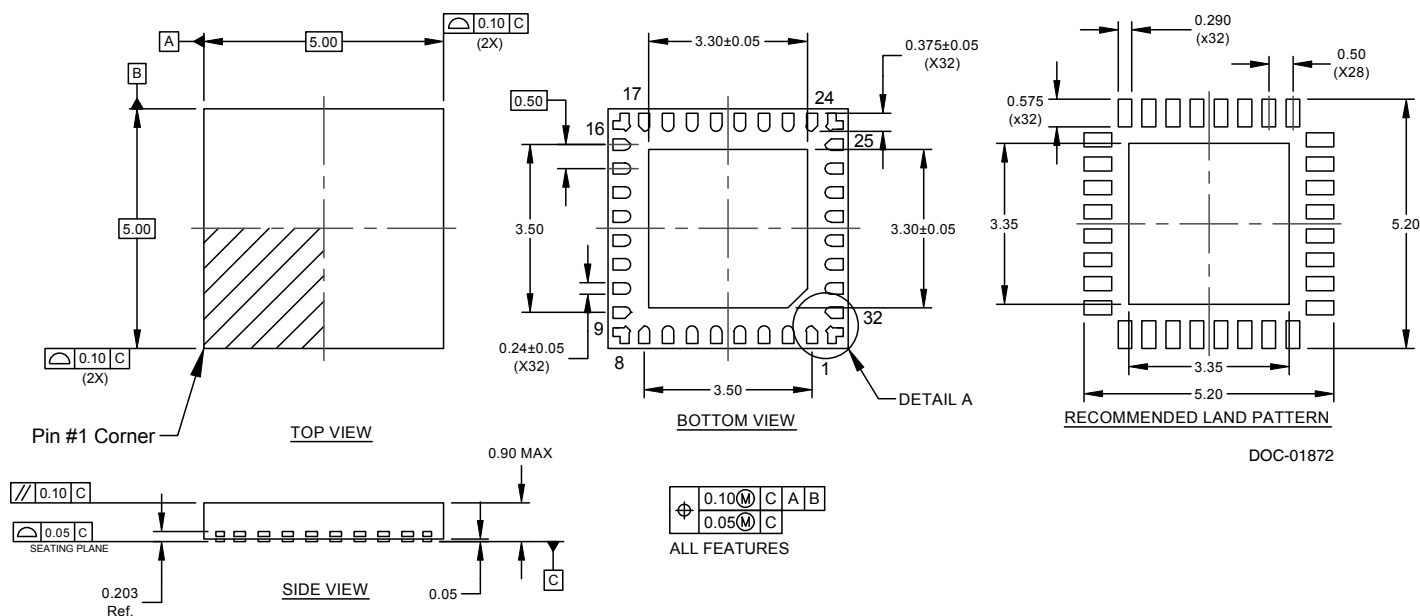


DOC-47827

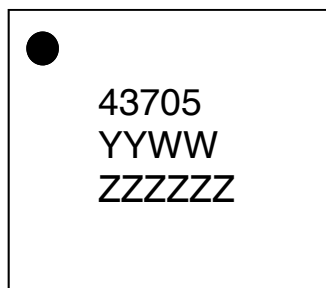
- Notes: 1. Use PRT-13505 PCB  
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)



**Figure 32. Package Drawing**  
32-lead 5x5 QFN



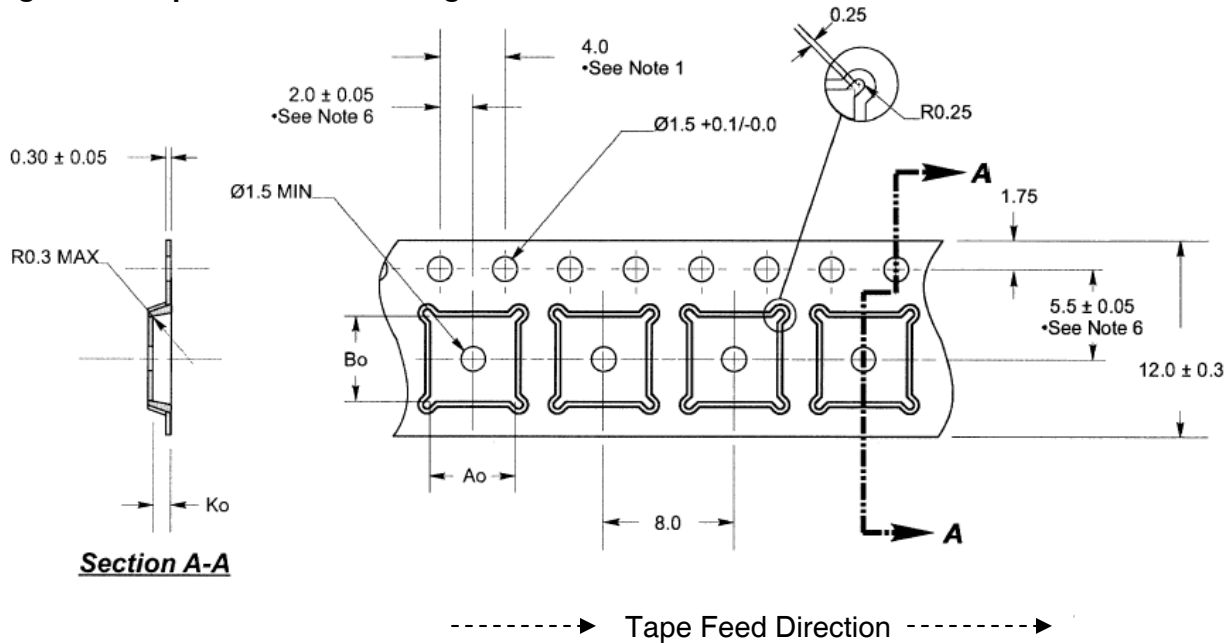
**Figure 33. Top Marking Specification**



17-0091

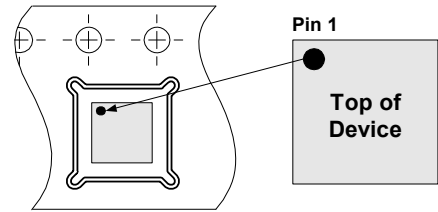
- = Pin 1 designator
- YYWW = Date Code, last two digits of the year and work week
- ZZZZZZ = Six digits of the lot number

**Figure 34. Tape and Reel Drawing**



- Notes:
1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.02$
  2. Camber not to exceed 1 mm in 100 mm
  3. Material: PS + C
  4.  $A_o$  and  $B_o$  measured as indicated
  5.  $K_o$  measured from a plane on the inside bottom of the pocket to the top surface of the carrier
  6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

$A_o = 5.25$  mm  
 $B_o = 5.25$  mm  
 $K_o = 1.1$  mm



Device Orientation in Tape

**Table 14. Ordering Information**

Order Code	Description	Package	Shipping Method
PE43705A-Z	PE43705 Digital step attenuator	32-lead 5x5 mm QFN	3000 units / T&R
EK43705-11	PE43705 Evaluation kit	Evaluation kit	1 / Box

**Sales Contact and Information**

For sales and contact information please visit [www.psemi.com](http://www.psemi.com).

**Advance Information:** The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.  
**Preliminary Specification:** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.  
**Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).  
 The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.  
 The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: <http://patents.psemi.com>.