MICRF008

QwikRadio® Sweep-Mode Receiver

General Description

The MICRF008 QwikRadio® UHF receiver is a single-chip OOK (on-off keyed) receiver IC designed for remote wireless applications. This device is a true single-chip, “antenna-in, data-out” device, and it is easy to implement. MICRF008 receiver requires very few peripheral passive components. All tunings, RF and IF, are accomplished within the IC. Ease of use and minimal parts count translate to cost savings and shorter time to market. MICRF008 receiver offers a robust and low-cost solution for high volume wireless applications.

The MICRF008 sweeps the internal local oscillator at rates greater than the baseband data rate. This effectively broadens the RF bandwidth of the receiver to a value equivalent to conventional superregenerative receivers. This allows the MICRF008 to operate with less expensive LC transmitters without additional components or tuning, even though the receiver topology is still superheterodyne. In this mode the reference crystal can be replaced with a less expensive ±0.5% ceramic resonator.

Since all post-detection (demodulator) data filtering is provided on the MICRF008, no external IF filters are required. One of the two internal filter bandwidths must be externally selected based on data rate and code modulation format.

Data sheets and support documentation can be found on Micrel’s web site at: www.micrel.com.

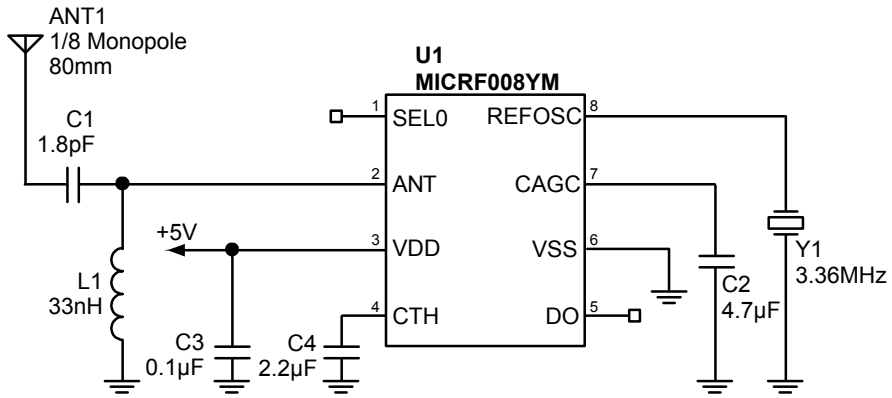
Features

Complete UHF receiver on a monolithic chip
300MHz to 440MHz frequency range
Up to 4.8kbps data rate.
Automatic tuning, no manual adjustment
Very low RF antenna reradiation
CMOS logic interface for standard ICs
Low external part count
Replaces superregenerative receivers design
Manufacturability and same performance over the years
Very small PCB area required

Applications

Garage door and gate openers
Security systems
Remote appliances control
Toys
Fan and light control

Typical Application

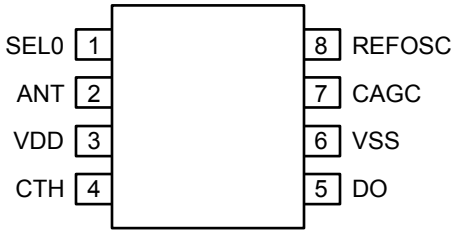


433.92MHz Receiver

Ordering Information

Part Number	Junction Temperature Range	Package	Lead Finish
MICRF008YM	–40°C to +85°C	8-Pin SOIC	Pb-Free

Pin Configuration



8-Pin SOIC (M)

Pin Description

Pin Number SOIC-8	Pin Name	Pin Name
1	SEL0	Bandwidth Selection Bit 0 (Digital Input): Sets the desired demodulator filter bandwidth. See Table 1. Internally pulled-up to VDD.
2	ANT	Antenna (Input): High-impedance, internally AC-coupled receiver input. Connect this pin to the matching network. See "Applications Information" for optional band-pass filter information.
3	VDD	Positive Supply Input: Connect a low ESL, low ESR decoupling capacitor from this pin to VSS, as short as possible.
4	CTH	Data Slicing Threshold Capacitor (External Component): Capacitor extracts the DC average value from the demodulated waveform which becomes the reference for the internal data slicing comparator. See "Applications Information" for selection.
5	DO	Data Output (Output): CMOS-level compatible data output signal.
6	VSS	Negative Supply Input: Connect this pin to the RF ground.
7	CAGC	AGC Capacitor (External Component): Integrating capacitor for on-chip AGC (automatic gain control). The decay/attack time-constant (τ) ratio is nominally 10:1. See "Applications Information" for capacitor selection.
8	REFOSC	Reference Oscillator (External Component or Input): Timing reference for on-chip tuning and alignment. Connect either a ceramic resonator or a crystal between this pin and VSS, or drive the input with an AC-coupled 0.5VPP input clock.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DDRF}, V_{DDBB}).....+7V
Reference Oscillator Input Voltage (V_{REFOSC})..... V_{DDBB}
Input/Output Voltage ($V_{I/O}$). .....V_{SS}–0.3 to V_{DD}+0.3
Junction Temperature (T_J) .....+150°C
Storage Temperature (T_s) .....–65°C to 150°C
Lead Temperature (soldering, 10 sec.)..... 260°C
ESD Rating[3]

Operating Ratings[2]

Supply Voltage (V_{DD})..... +4.75V to +5.5V
Ambient Temperature (T_A) .....–40°C to +85°C
RF Frequency Range..... 300MHz to 440Hz
Data Duty-Cycle .....20% to 80%
Reference Oscillator Input Range..... $0.2V_{PP}$ to $1.5V_{PP}$
Demon Bandwidth..... 0.1 to 4.8kHz

Electrical Characteristics[4]

+4.75V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V; C_{AGC} = 4.7µF, C_{TH} = 2.2µF no preamble for data; f_{REFOSC} = 3.36MHz. T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; current flow into device pins is positive; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OP}	Operating Current	Continuous 315MHz operation		7	9	mA
		continuous 433.92MHz operation		13	16	mA
		reference oscillator powered down		2	2.5	mA
RF Section, IF Section						
	Receiver Sensitivity	315MHz, SEL0 = 0V; **Notes 5, 6**	–90	–95		dBm
		433.92MHz, SEL0 = 0V; **Notes 5, 6**	–90	–95		dBm
f_{IF}	IF Center Frequency	**Note 7**		2.0		MHz
f_{BW}	IF Bandwidth	315MHz, **Notes 6, 7**		0.8		MHz
		433.92MHz, **Notes 6, 7**		1.1		MHz
	Maximum Receiver Input	R_{SC} = 50Ω		–20		dBm
	Spurious Reverse Isolation	ANT pin, R_{SC} = 50Ω, **Note 8**		30		μV_{RMS}
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$		0.1		
Reference Oscillator						
	Reference Oscillator Source Current			7		µA
Z_{REFOSC}	Reference Oscillator Input Impedance	**Note 9**		200		kΩ
Demodulator						
Z_{CTH}	C_{TH} Source Impedance	V_{SEL0} = V_{DD}, **See Table 1, Note 10**		220		kΩ
ΔZ_{CTH}	Maximum C_{TH} Source Impedance Variation			±15		%
Digital/Control Section						
$Z_{IN(pu)}$	Input Pull-Up Impedance	SEL0		1.0	**0.8**	MΩ
I_{OUT}	Output Current	DO pin, push-pull		10		µA
$V_{OUT(high)}$	Output High Voltage	DO pin, I_{OUT} = 1µA	**$0.8V_{DD}$**			V
$V_{OUT(low)}$	Output Low Voltage	DO pin, I_{OUT} = 1µA			**$0.2V_{DD}$**	V
t_R, t_F	Output Rise and Fall Times	DO pin, C_{LOAD} = 15pF		10		µs

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive, use appropriate ESD precautions. Meets class 1 ESD test requirements, (human body model HBM), in accordance with MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.
4. Specification for packaged product only.
5. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10^{-2} BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle at a data rate of 1kbps (Manchester encoded). The RF input is assumed to be matched into 50Ω.
6. Sensitivity, a commonly specified receiver parameter, provides an indication of the receiver's input referred noise, generally input thermal noise. However, it is possible for a more sensitive receiver to exhibit range performance no better than that of a less sensitive receiver if the background noise is appreciably higher than the thermal noise. Background noise refers to other interfering signals, such as FM radio stations, pagers, etc.

   A better indicator of achievable receiver range performance is usually given by its selectivity, often stated as intermediate frequency (IF) or radio frequency (RF) bandwidth, depending on receiver topology. Selectivity is a measure of the rejection by the receiver of ambient noise. More selective receivers will almost invariably provide better range. Only when the receiver selectivity is so high that most of the noise on the receiver input is actually thermal will the receiver demonstrate sensitivity-limited performance.
7. Parameter scales linearly proportional with reference oscillator frequency f_T. For any reference oscillator frequency other than 3.36MHz, compute new parameter value as the ratio:

$$\frac{f_{REFOSC}\,MHz}{3.36MHz} \times (\text{parameter value at } 3.36MHz)$$

8. Spurious reverse isolation represents the spurious components which appear on the RF input pin (ANT) measured into 50Ω with an input RF matching network
9. Series resistance of the resonator (ceramic resonator or crystal) should be minimized to the extent possible. In cases where the resonator series resistance is too great, the oscillator may oscillate at a diminished peak-to-peak level, or may fail to oscillate entirely. Micrel recommends that series resistances for ceramic resonators and crystals not exceed 50Ω and 100Ω respectively.
10. Parameter scales linearly proportional with reference oscillator frequency f_T. For any reference oscillator frequency other than 3.36MHz, compute new parameter value as the ratio:

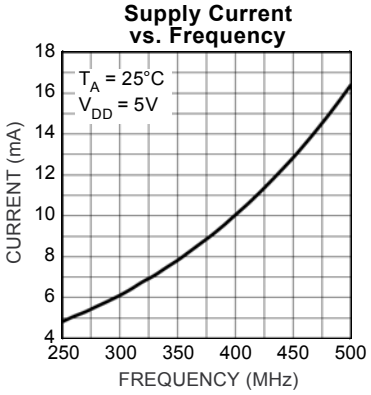
$$\frac{3.36MHz}{f_{REFOSC}\,MHz} \times (\text{parameter value at } 3.36MHz)$$

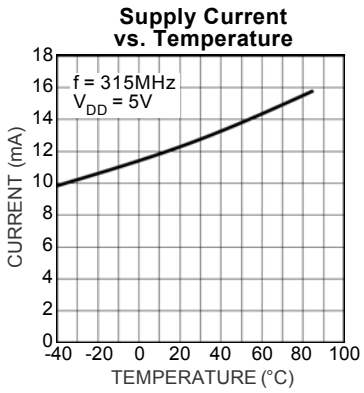
C_{TH} source impedance in Table 1 is represented by (symbolic) resistor RSC in the MICRF008 Simplified Block Diagram. The Programmable LPF (Low Pass Filter) is also illustrated in the MICRF008 Simplified Block Diagram.

SEL0	Programmable LPF Bandwidth (Hz)	C_{TH} Source Impedance (Ω)
1	2400	440k
0	4800	220k

Table 1. Nominal Characteristics Programmable LPF Bandwidth and CTH Source Impedance

Typical Characteristics





Functional Diagram

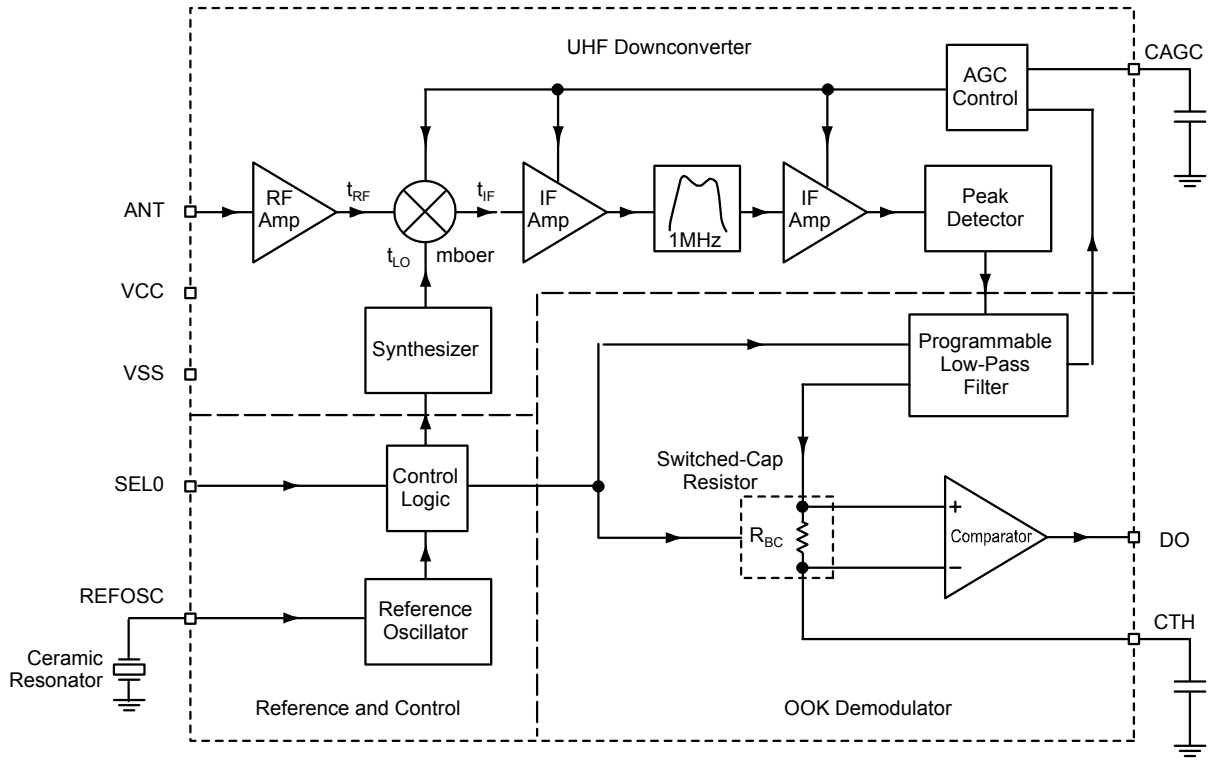


Figure 1. MICRF008 Block Diagram

Functional Description

The entire block diagram illustrates the basic structure of the MICRF008YM. It is made of three sub-blocks, which are the UHF Downconverter, the OOK Demodulator, and the Reference and Control. Also shown in the figure are two capacitors (CTH, and CAGC) and the reference frequency device, usually a ceramic resonator. With the exception of a supply decoupling capacitor and the matching network on the antenna pin, these are all the external components needed with the MICRF008YM to make a complete UHF receiver. There is one control input, the SEL0 pin. The purpose is to set the demodulator filter bandwidth of either 2.4kHz or 4.8kHz, and is set high or low according to the minimum pulse width in the demodulated signal. The input is CMOS compatible, and is pulled-up internally in the IC.

Receiver Operation

The MICRF008YM is a superheterodyne receiver working in sweep mode. It is capable of data rates up to 9.6kbaud NRZ or 4.8kbaud Manchester encoded. The MICRF008YM RF center frequency is controlled by a completely integrated PLL/VCO frequency synthesizer with frequency set by a ceramic resonator. The actual swept bandwidth is approximately 3% of the RF carrier frequency. It makes an ideal part to work with LC-based transmitters or other types of transmitters that are not precise in nature and vary their frequency with time. In sweep mode the LO frequency (local oscillator) is varied in a rate much higher than the data signal, which results in down-conversion of approximately 3% of the carrier frequency present at the antenna pin. The low level RF signal is amplified by the RF amp section and downconverted by the mixer to the IF frequency which is amplified and filtered internally in the device and further amplified for the peak detector. The peak detector will detect the IF and further filtering is accomplished in the programmable low-pass filter. The detected/filtered signal is compared with the DC value of the demodulated signal in the data-slicer and a digital output is provided from the DO pin

Data Slicing Level

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished by an external capacitor CTH and the on-chip switched-capacitor resistor RSC, indicated in the block diagram. The effective resistance of RSC scales inversely

proportional to REFOSC frequency. The nominal value of RSC given in the “Electrical Characteristics ” Table is 220kΩ for a REFOSC frequency of 3.36MHz. Slicing level time constant value vary depending on data pattern, data rate and data duty cycle.

Automatic Gain Control (AGC)

The signal path has automatic gain control (AGC) to increase the overall receiver dynamic range. An external capacitor, CAGC, must be connected to the CAGC pin of the device. Normally the CAGC capacitor is connected to ground. If faster start-up times are required when the receiver is first poweredon, the CAGC capacitor may be connected to VDD. The ratio of decay-to-attack time constant is fixed at 10:1 (that is, the attack time constant is 1/10th of the decay time constant), and the user cannot change this ratio. Nevertheless, the attack time constant is set externally by choosing a value for CAGC.

Another function of the AGC control voltage is to raise the noise floor in order to guarantee a clean signal between the preamble and the data, sometimes called dead time. The AGC control voltage can be further manipulated and amplified to create an RSSI signal, which is useful for several different applications.

Reference Oscillator

All timing and tuning operations on the MICRF008YM are derived from the internal Colpitts reference oscillator. The reference frequency can be implemented in two ways, by using a resonator device (a ceramic resonator or crystal), or by driving an external signal, which should not exceed 0.5VRMS. The reference frequency is obtained by dividing the RF carrier frequency by 129.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF008 is shown in Figures 2 through 6. Specific information regarding each of these circuits is discussed in the following subparagraphs. Not shown are ESD protection diodes which are applied to all input pins.

CTH Pin

Figure 2 illustrates the CTH pin interface circuit. CTH pin is driven from a P-Channel MOSFET source-follower biased with approximately 20µA of bias current. Transmission gates TG1 and TG2 isolate the 3.3pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a “resistance.” The DC potential on the CTH pin is approximately 2.2V, fundamentally determined by the VGS of the two PChannel MOSFET source-followers shown.

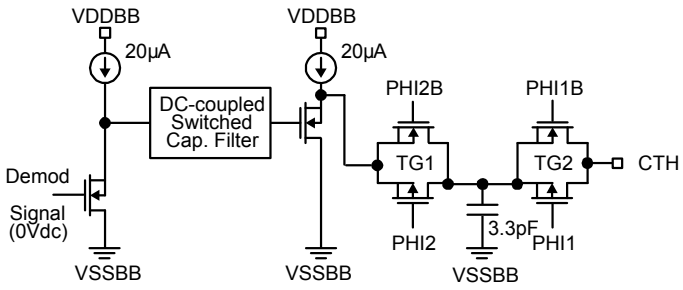


Figure 2. CTH Pin

CAGC Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor CAGC. The attack current is nominally 15µA, while the decay current is a 1/10th scaling of this, approximately 1.5µA. Signal gain of the RF/IF strip inside the IC diminishes as the voltage on CAGC decreases. By simply adding a capacitor to CAGC pin, the attack/decay time constant ratio is fixed at 1:10.

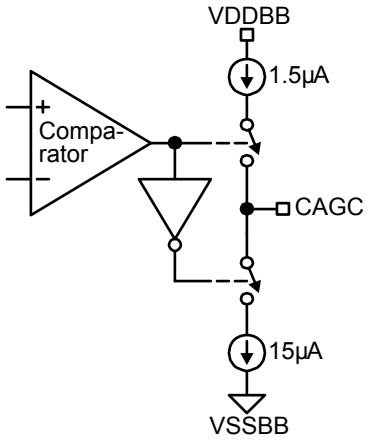


Figure 3. CAGC Pin

DO Pin

The output stage for the Data Comparator (DO pin) is shown in Figure 4. The output is a 10µA push-10µA pull, switched current stage. Such an output stage is capable of driving CMOS-type loads.

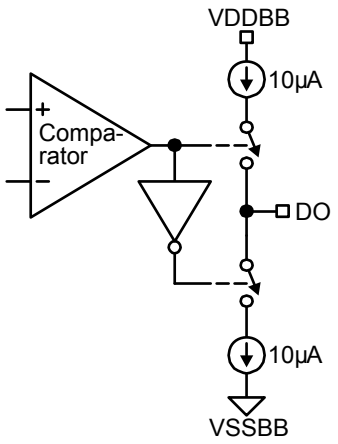


Figure 4. DO Pin

REFOSC Pin

The REFOSC input circuit is shown in Figure 5. Input impedance is quite high (200kΩ). This is a Colpitts oscillator, with internal 30pF capacitors. This input is intended to work with standard ceramic resonators, connected from this pin to VSSBB. The resonators should not contain integral capacitors, since these capacitors are contained inside the IC. Externally applied signals should be AC-coupled, amplitude limited to approximately $0.5V_{PP}$. The nominal DC bias voltage on this pin is 1.4V.

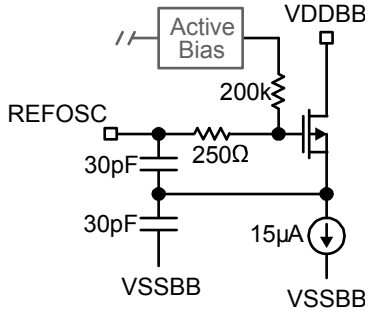


Figure 5. REFOSC Pin

Control Input (SEL0)

Control input circuitry is shown in Figure 6. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-Channel MOSFET Q1 is a large channel length device which functions essentially as a “weak” pullup to VDDBB. Typical pullup current is 5µA, leading to an impedance to the VDDBB supply of typically 1MΩ.

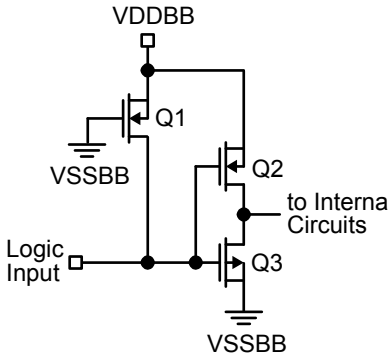
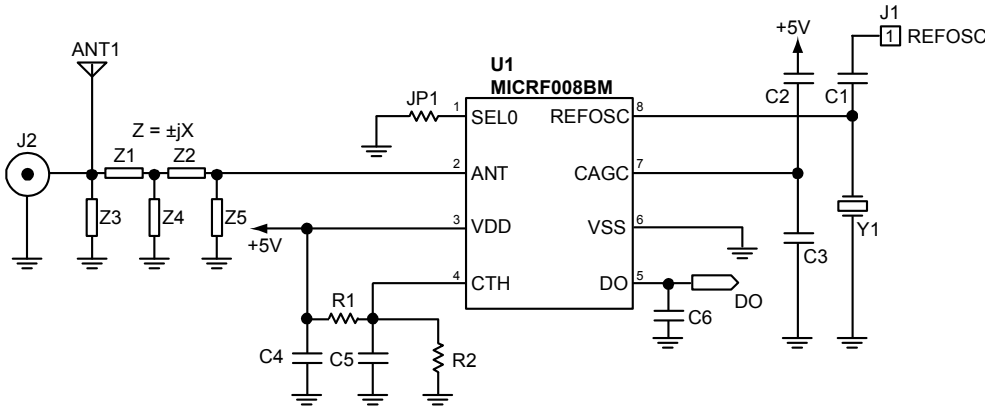


Figure 6. SEL0

Test Circuit



Test Circuit and Application Information

The test circuit is based on the EVAL8 PCB Design. Gerbers, the bill of material and complete schematic are available at Micrel website:

(http://www.micrel.com/product-info/qwikradio.shtml).

EVAL8 provides the means for a complete evaluation of the MICRF008YM. It is not intended as a final receiver design. For final receiver applications, look for the RX8-x series of reference designs. The board is a FR4 material, 0.062 inch thick, in two layers. It is strongly recommended that all RF designs are made in a minimum two-layer board, one side being as solid ground as possible. Blank EVAL8 boards are available for selected customers. To obtain a blank board contact your local Micrel representative/distributor. Four drawings are shown below, the top layer, bottom layer, the top silkscreen layer, and the bottom silkscreen layer. The size of the board is 0.910 x 0.760 inches. It provides the means to test the part thoroughly.

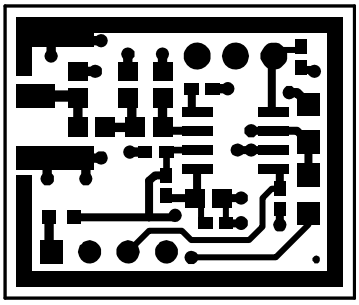


Figure 7a. Top Layer

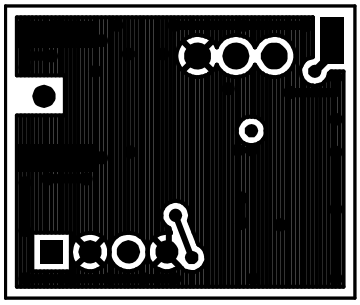


Figure 7b. Bottom Layer

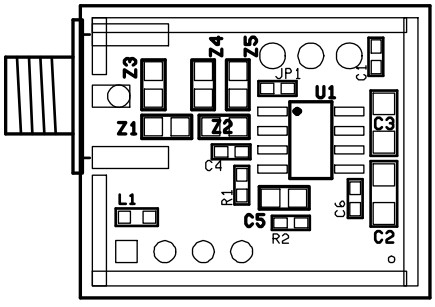


Figure 7c. Top Silkscreen Layer

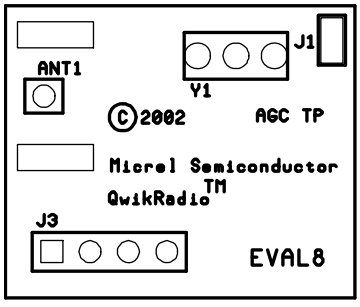


Figure 7d. Bottom Silkscreen Layer

Input Connector/Antenna

Starting at J2, a SMA connector to connect to a RF signal generator. Levels above –20dBm should be avoided. An antenna pad is also provided. Solder a piece of solid wire for the frequency of interest. See Table 2 for 1/4 wavelength antennas. It should be noted that 1/4 wavelength antennas work best ONLY with ground planes of an equivalent size of the antenna. This is not the case here since the board size is very small.

Freq. (MHz)	ANT1 (mm)	ANT1 (inches)
315	231	9.1
390	185	7.3
418	173	6.8
433.92	168	6.6

Table 2. 1/4 Wave Antenna Lengths

The size of the antenna is calculated by the following equation:

$$\frac{1}{4}\lambda\text{Ant} = \frac{3\times10^{8}\times0.97\times1000}{f\times4}[\text{mm}]$$

$$\frac{1}{4}\lambda\text{Ant} = \frac{3\times10^{8}\times0.97\times1000}{f\times101.6}[\text{inches}]$$

where,

- 3 x 10^8 is the speed of light in vacuum in meter per seconds.
- 0.97 is a correction factor for the difference between electrical length and physical length and varies depending on ground plane, and objects next to the antenna.
- f is the frequency of interest in Hertz.

1/4 wavelength antennas are good for initial tests, but should never be used in a final product, unless the PCB area has a large ground plane. Small ground planes makes 1/4 wavelength monopole antennas unstable, and any object close to the antenna changes its impedance. It is completely useless if the antenna is not straight up or if any object touches it. Other antennas, such as half-wave dipole, or 1/8 wavelength monopole are better solutions for small ground planes. A 1/8 wavelength antenna has approximately half the size of a 1/4 wavelength antenna, which makes it very attractive for small designs. The 1/8 wavelength antenna is not as sensitive to proximity effects as the 1/4 wavelength antenna. However, the 1/8 wavelength antenna has a reactive element in its impedance that needs to be taken into account in the matching network. The halfwave dipole has a size approximately double the 1/4 wavelength and does not require a large ground plane. One side of the antenna is connected to the RF input and the other is connected to ground as seen in Figure 8.

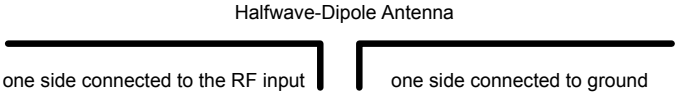


Figure 8. Halfwave-Dipole Antenna

Matching Network

Z1 to Z5 are used for the matching network. Not all parts are used at the same time. Several types of matching network can be implemented: T, π, or a L network. Here a matching network has two purposes. The main purpose is to match the antenna to the antenna pin. By matching it is meant to reduce the loss there is between two circuits; here the antenna being used or signal generator and the antenna pin. The secondary purpose is to filter undesired signals, which will reduce the receiver performance. Since it is a secondary function, more filtering may be required, depending on the amount of noise or adjacent signal interference present in the antenna. A T-Network was chosen assuming that an 1/4 wavelength antenna is being used, which has impedance close to 50Ω in free air or the receiver is being connected to a RF signal generator that has 50Ω output impedance. By using the proper matching elements, almost 9dB better sensitivity can be obtained. There are several techniques used for impedance matching. One frequently used is to plot impedance values in the Smith Chart. However, one needs to know the antenna impedance and the antenna pin impedance in the MICRF008YM to perform the matching. Table 3 below shows the antenna pin input impedance versus frequency and the matching elements needed to match 50Ω to the antenna pin.

Freq. (MHz)	ANT1 (mm)	ANT1 (inches)
315	231	9.1
390	185	7.3
418	173	6.8
433.92	168	6.6

Note 1. All inductors used are Coilcraft 0603 size, and the capacitors are Vishay COG 5%. Z3 and Z5 are not used.

Table 3. Antenna Input, Frequency and Matching Values

C_{TH} Capacitor

In order to calculate the right value for the C_{TH} capacitor, the data format needs to have a preamble that resembles the data pattern, that is it has the same period and duty cycle. (See *"Application Hint 42"*) If the data pattern has no preamble, a large capacitor value should be used, such as 1µF to 2.2µF. However, if the data pattern has a preamble, the C_{TH} capacitor can be calculated and should be used instead of a large capacitor. This will guarantee a stable and reliable performance for the receiver. If the data pattern has variable data rates, the C_{TH} capacitor should be calculated for the lowest data rate and optimized in range tests. To find the C_{TH} capacitor value follow the procedure below:

1. Find the data period or bit period, and the reference oscillator frequency. The reference oscillator frequency is the RF carrier frequency divided by 129. The bit period is the elapsed time from one high and one low of the data pattern.
2. The C_{TH} capacitor is calculated by:

$$C_{TH} = \frac{5 \times \text{bit period} \times \text{REFOSC}}{144.55 \times 10^3} [\text{F}]$$

where:

REFOSC is the reference oscillator frequency in MHz.

Bit period is given in seconds and is the inverse of the baud rate for Manchester encoding.

The result obtained is in farads.

It follows the C_{TH} capacitor value for the common frequencies mentioned above in the Table 4. Again, as mentioned before, the data pattern needs preamble.

	Baud Rate (Hz)		
Frequency (MHz)	**1000 C_{TH}**	**2400 C_{TH}**	**4800 C_{TH}**
315	82nF	39nF	18nF
390	100nF	47nF	22nF
418	120nF	47nF	22nF
433.93	120nF	47nF	22nF

Table 4. Recommended C_{TH} Capacitor Values

C_{AGC} Capacitor

The function of the C_{AGC} capacitor is to minimize the ripple on the AGC control voltage by using a sufficiently large capacitor. It is suggested a value between 1µF to 10µF depending on data dead time, noise, and recovery time from strong to low RF signals. Large capacitor values can be connected to V_{DD} if fast charge time is required (C2). When connected to V_{DD}, it will charge 10 times faster. The drawback is the ripple noise from AGC pin being thrown into the V_{DD} line. The signal on this pin is current-based, with an attack current of 15µA, and a decay current of 1.5µA. It is suggested the following values for the C_{AGC} capacitors in the Table 5. Values can be further optimized during receiver range tests.

Baud Rate (Hz)	C_{AGC} (µF)
1000	4.7 to 10
2400	2.2 to 4.7
4800	1 to 2.2

Table 5. Recommended Values for C_{AGC}

Reference Oscillator Frequency

A Colpitts oscillator inside the chip generates the reference oscillator frequency. It requires a resonator of some kind connected to the REFOSC pin. Either a ceramic resonator or a crystal can be used. A resonator is chosen due to its lower cost and because the MICRF008YM is running in sweep mode, which does not require the precision of a crystal. Resonators found in the market normally have a precision of 0.5%. This precision is sufficient for the MICRF008YM. The reference oscillator frequency can also be generated by an external source through connector J1 and capacitor C1. The maximum level should not exceed $0.5V_{RMS}$. The reference oscillator frequency is calculated by the following equation and Table 6 shows the resonator frequency for the most common used frequencies:

$$\text{REFOSC} = \frac{\text{fc}}{129}$$

where:

- REFOSC is the reference oscillator frequency in MHz.
- fc is the RF received carrier frequency of interest in MHz.

Frequency (MHz)	REFOSC (MHz)
315	2.44
390	3.02
418	3.24
433.92	3.36

Table 6. Reference Oscillator Frequency

For a list of ceramic resonator manufactures, see *"Application Hint 35."*

SEL0 Pin – Setting the Demodulator Bandwidth

The SEL0 pin sets the demodulator bandwidth. When the pin is connected to ground the demodulator bandwidth is set to its minimum. When the pin is left floating (internal pull-up) or connected to VDD, the demodulator bandwidth is set to its maximum. The demodulator bandwidth is a function of the RF frequency used. See Table 7 for the most common frequency used versus the demodulator bandwidth.

	RF Carrier Frequency (MHz)			
SEL0	**315**	**390**	**418**	**433.92**
0	1.6kHz	2.0kHz	2.2kHz	2.4kHz
1	3.6kHz	4.0kHz	4.4kHz	4.8kHz

Table 7. Demodulator Bandwidth

To determine what is the demodulator bandwidth required for the application, the absolute minimum pulse width used in the encoder transmitted signal needs to be found. The data pattern has several different types of pulse width depending what data format is being used (NRZ, Manchester, PWM, etc). The minimum pulsewidth is the shortest pulse in the output of the encoder being sent to the transmitter input measured during one bit time when the signal is high. See Figure 9 below for clarification.

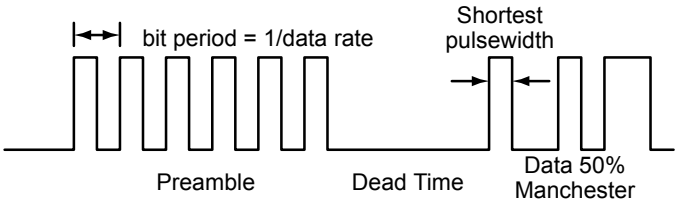


Figure 9. Data Pattern

Then, the demodulator bandwidth required is calculated by:

$$\text{Demod BW} = \frac{0.65}{\text{shortest pulse}}[\text{Hz}]$$

Data Squelching

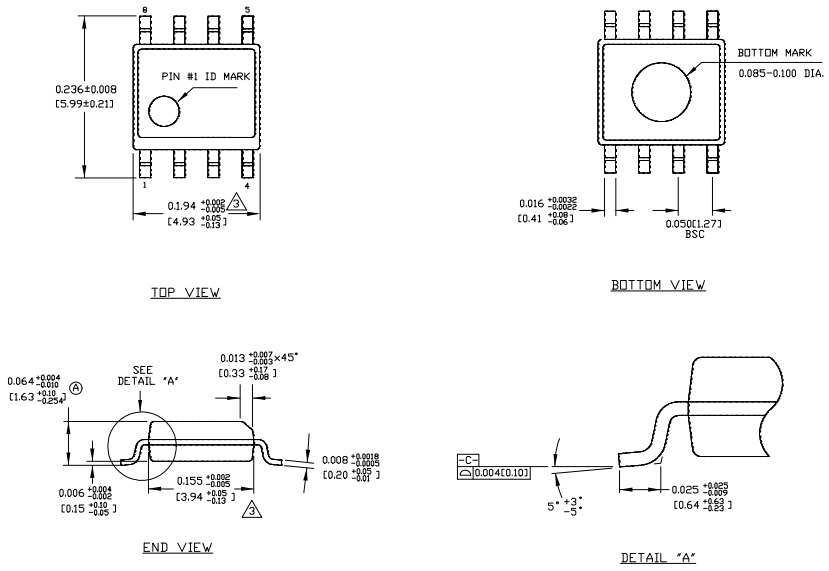
Data squelching can be achieved by software or hardware. The software squelch is preferred over hardware squelch for it is more flexible, reliable, lower cost over manufacturing, etc. However, it takes time and resources to develop any software. If one needs a squelch function, a resistor can be used in the C_{TH} pin. R1 and R2 are in the test circuit for this purpose. Either one of them can be used or both. If only one resistor is used, the value of the resistor should be chosen according to the amount of squelch needed and if the DO pin needs to be sitting high or low without an RF income signal. Values from 10MΩ and below can be used. When both resistors are used, a more accurate control can be achieved for the squelch function.

The drawbacks using these resistors are: loss in receiver sensitivity, reduced demodulator bandwidth, and the C_{TH} capacitor equation will not work. As a result, C_{TH} capacitor will have to be determined empirically. Another way to implement a hardware squelch is to make R1 equal to 10MΩ to 6.8MΩ, and use a low-pass filter after the DO pin and a comparator circuit. The low-pass filter can be a capacitor, which is C6 in the Test Circuit. The reference voltage in the comparator can be set close to VDD/2 and the other input connected to the DO pin.

Power Supply Filter

A decoupling capacitor right at the VDD pin is strongly recommended as it is in the test circuit, which has 0.1µF. Not shown in the Test Circuit Schematic is an EMI Inductor, L1 in the silkscreen layer. It has the purpose to further filter an income noise on the VDD line, generally present in switching power supplies. It is good practice to separate RF ground from digital ground and also VDD RF from other VDD lines

Package Information



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

8-Pin SOIC (M)

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