

## Introduction

Kintex®-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two  $V_{CCINT}$  voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at  $V_{CCINT} = 1.0V$ , the speed specification of a -2L device is the same as the -2 speed grade. When operated at  $V_{CCINT} = 0.9V$ , the -2L performance and static and dynamic power is reduced.

Kintex-7 FPGA DC and AC characteristics are specified in commercial, extended, industrial, and military temperature ranges. Except for the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade military device are the same as for a -1 speed grade commercial

device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in:

- *7 Series FPGAs Overview* ([DS180](#))
- *Defense-Grade 7 Series FPGAs Overview* ([DS185](#))

This Kintex-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at [www.xilinx.com/7](http://www.xilinx.com/7).

## DC Characteristics

Table 1: Absolute Maximum Ratings (1)

| Symbol                 | Description   | Min   | Max              | Units |
|------------------------|---|-------|------------------|-------|
| <b>FPGA Logic</b>      |   |       |                  |       |
| $V_{CCINT}$            | Internal supply voltage   | -0.5  | 1.1              | V     |
| $V_{CCAUX}$            | Auxiliary supply voltage  | -0.5  | 2.0              | V     |
| $V_{CCBRAM}$           | Supply voltage for the block RAM memories   | -0.5  | 1.1              | V     |
| $V_{CCO}$              | Output drivers supply voltage for 3.3V HR I/O banks   | -0.5  | 3.6              | V     |
|                        | Output drivers supply voltage for 1.8V HP I/O banks   | -0.5  | 2.0              | V     |
| $V_{CCAUX\_IO}$        | Auxiliary supply voltage  | -0.5  | 2.06             | V     |
| $V_{REF}$              | Input reference voltage   | -0.5  | 2.0              | V     |
| $V_{IN}^{(2)(3)(4)}$   | I/O input voltage for 3.3V HR I/O banks   | -0.40 | $V_{CCO} + 0.55$ | V     |
|                        | I/O input voltage for 1.8V HP I/O banks   | -0.55 | $V_{CCO} + 0.55$ | V     |
|                        | I/O input voltage (when $V_{CCO} = 3.3V$ ) for $V_{REF}$ and differential I/O standards except TMSD_33 <sup>(5)</sup> | -0.40 | 2.625            | V     |
| $V_{CCBATT}$           | Key memory battery backup supply  | -0.5  | 2.0              | V     |
| <b>GTX Transceiver</b> |   |       |                  |       |
| $V_{MGTAVCC}$          | Analog supply voltage for the GTX transmitter and receiver circuits   | -0.5  | 1.1              | V     |
| $V_{MGTAVTT}$          | Analog supply voltage for the GTX transmitter and receiver termination circuits                                       | -0.5  | 1.32             | V     |
| $V_{MGTVCCAUX}$        | Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers  | -0.5  | 1.935            | V     |
| $V_{MGTREFCLK}$        | GTX transceiver reference clock absolute input voltage  | -0.5  | 1.32             | V     |

**Table 1: Absolute Maximum Ratings (1) (Cont'd)**

| Symbol              | Description  | Min  | Max  | Units |
|---------------------|--|------|------|-------|
| $V_{MGTAVTTRCAL}$   | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column | -0.5 | 1.32 | V     |
| $V_{IN}$            | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage                      | -0.5 | 1.26 | V     |
| $I_{DCIN-FLOAT}$    | DC input current for receiver input pins DC coupled RX termination = floating            | -    | 14   | mA    |
| $I_{DCIN-MGTAVTT}$  | DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$       | -    | 12   | mA    |
| $I_{DCIN-GND}$      | DC input current for receiver input pins DC coupled RX termination = GND                 | -    | 6.5  | mA    |
| $I_{DCOUT-FLOAT}$   | DC output current for transmitter pins DC coupled RX termination = floating              | -    | 14   | mA    |
| $I_{DCOUT-MGTAVTT}$ | DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$         | -    | 12   | mA    |
| <b>XADC</b>         |  |      |      |       |
| $V_{CCADC}$         | XADC supply relative to GNDADC   | -0.5 | 2.0  | V     |
| $V_{REFP}$          | XADC reference input relative to GNDADC  | -0.5 | 2.0  | V     |
| <b>Temperature</b>  |  |      |      |       |
| $T_{STG}$           | Storage temperature (ambient)  | -65  | 150  | °C    |
| $T_{SOL}$           | Maximum soldering temperature for Pb/Sn component bodies (6)                             | -    | +220 | °C    |
|                     | Maximum soldering temperature for Pb-free component bodies (6)                           | -    | +260 | °C    |
| $T_j$               | Maximum junction temperature(6)  | -    | +125 | °C    |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide (UG471)*.
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see [Table 4](#) and [Table 5](#).
- See [Table 10](#) for TMDS\_33 specifications.
- For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification (UG475)*.

**Table 2: Recommended Operating Conditions (1)(2)**

| Symbol                | Description   | Min   | Typ  | Max             | Units |
|-----------------------|---|-------|------|-----------------|-------|
| <b>FPGA Logic</b>     |   |       |      |                 |       |
| $V_{CCINT}^{(3)}$     | Internal supply voltage   | 0.97  | 1.00 | 1.03            | V     |
|                       | For -2L (0.9V) devices: internal supply voltage   | 0.87  | 0.90 | 0.93            | V     |
| $V_{CCBRAM}^{(3)}$    | Block RAM supply voltage  | 0.97  | 1.00 | 1.03            | V     |
|                       | For -2L (0.9V) devices: block RAM supply voltage  | 0.87  | 0.90 | 1.03            | V     |
| $V_{CCAUX}$           | Auxiliary supply voltage  | 1.71  | 1.80 | 1.89            | V     |
| $V_{CCO}^{(4)(5)}$    | Supply voltage for 3.3V HR I/O banks  | 1.14  | -    | 3.465           | V     |
|                       | Supply voltage for 1.8V HP I/O banks  | 1.14  | -    | 1.89            | V     |
| $V_{CCAUX\_IO}^{(6)}$ | Auxiliary supply voltage when set to 1.8V   | 1.71  | 1.80 | 1.89            | V     |
|                       | Auxiliary supply voltage when set to 2.0V   | 1.94  | 2.00 | 2.06            | V     |
| $V_{IN}^{(7)}$        | I/O input voltage   | -0.20 | -    | $V_{CCO} + 0.2$ | V     |
|                       | I/O input voltage (when $V_{CCO} = 3.3V$ ) for $V_{REF}$ and differential I/O standards except TMDS_33(8) | -0.20 | -    | 2.625           | V     |
| $I_{IN}^{(9)}$        | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.      | -     | -    | 10              | mA    |
| $V_{CCBATT}^{(10)}$   | Battery voltage   | 1.0   | -    | 1.89            | V     |

Table 2: Recommended Operating Conditions (1)(2) (Cont'd)

| Symbol                   | Description   | Min  | Typ  | Max  | Units |
|--------------------------|---|------|------|------|-------|
| <b>GTX Transceiver</b>   |   |      |      |      |       |
| $V_{MGTAVCC}^{(11)}$     | Analog supply voltage for the GTX transceiver QPLL frequency range $\leq 10.3125$ GHz <sup>(12)(13)</sup> | 0.97 | 1.0  | 1.08 | V     |
|                          | Analog supply voltage for the GTX transceiver QPLL frequency range $> 10.3125$ GHz                        | 1.02 | 1.05 | 1.08 | V     |
| $V_{MGTAVTT}^{(11)}$     | Analog supply voltage for the GTX transmitter and receiver termination circuits                           | 1.17 | 1.2  | 1.23 | V     |
| $V_{MGTVCCAUX}^{(11)}$   | Auxiliary analog QPLL voltage supply for the transceivers   | 1.75 | 1.80 | 1.85 | V     |
| $V_{MGTAVTTRCAL}^{(11)}$ | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column                  | 1.17 | 1.2  | 1.23 | V     |
| <b>XADC</b>              |   |      |      |      |       |
| $V_{CCADC}$              | XADC supply relative to GNDADC  | 1.71 | 1.80 | 1.89 | V     |
| $V_{REFP}$               | Externally supplied reference voltage   | 1.20 | 1.25 | 1.30 | V     |
| <b>Temperature</b>       |   |      |      |      |       |
| $T_j$                    | Junction temperature operating range for commercial (C) temperature devices                               | 0    | –    | 85   | °C    |
|                          | Junction temperature operating range for extended (E) temperature devices                                 | 0    | –    | 100  | °C    |
|                          | Junction temperature operating range for industrial (I) temperature devices                               | –40  | –    | 100  | °C    |
|                          | Junction temperature operating range for military (M) temperature devices                                 | –55  | –    | 125  | °C    |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system, consult the *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483).
3.  $V_{CCINT}$  and  $V_{CCBRAM}$  should be connected to the same supply.
4. Configuration data is retained even if  $V_{CCO}$  drops to 0V.
5. Includes  $V_{CCO}$  of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at  $\pm 5\%$ .
6. For more information, refer to the  $V_{CCAUX\_IO}$  section of *7 Series FPGAs SelectIO Resources User Guide* (UG471).
7. The lower absolute voltage specification always applies.
8. See Table 10 for TMD5\_33 specifications.
9. A total of 200 mA per bank should not be exceeded.
10.  $V_{CCBATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{CCBATT}$  to either ground or  $V_{CCAUX}$ .
11. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476).
12. For data rates  $\leq 10.3125$  Gb/s,  $V_{MGTAVCC}$  should be  $1.0V \pm 3\%$  for lower power consumption.
13. For lower power consumption,  $V_{MGTAVCC}$  should be  $1.0V \pm 3\%$  over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

| Symbol         | Description   | Min  | Typ <sup>(1)</sup> | Max | Units   |
|----------------|---|------|--------------------|-----|---------|
| $V_{DRINT}$    | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | –                  | –   | V       |
| $V_{DRI}$      | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5  | –                  | –   | V       |
| $I_{REF}$      | $V_{REF}$ leakage current per pin   | –    | –                  | 15  | $\mu A$ |
| $I_L$          | Input or output leakage current per pin (sample-tested)                           | –    | –                  | 15  | $\mu A$ |
| $C_{IN}^{(2)}$ | Die input capacitance at the pad  | –    | –                  | 8   | pF      |
| $I_{RPU}$      | Pad pull-up (when selected) @ $V_{IN} = 0V, V_{CCO} = 3.3V$                       | 90   | –                  | 330 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V, V_{CCO} = 2.5V$                       | 68   | –                  | 250 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V, V_{CCO} = 1.8V$                       | 34   | –                  | 220 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V, V_{CCO} = 1.5V$                       | 23   | –                  | 150 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V, V_{CCO} = 1.2V$                       | 12   | –                  | 120 | $\mu A$ |

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

| Symbol                              | Description  | Min | Typ <sup>(1)</sup> | Max | Units |
|-------------------------------------|--|-----|--------------------|-----|-------|
| I <sub>RPD</sub>                    | Pad pull-down (when selected) @ V <sub>IN</sub> = 3.3V   | 68  | –                  | 330 | μA    |
|                                     | Pad pull-down (when selected) @ V <sub>IN</sub> = 1.8V   | 45  | –                  | 180 | μA    |
| I <sub>CCADC</sub>                  | Analog supply current, analog circuits in powered up state   | –   | –                  | 25  | mA    |
| I <sub>BATT</sub> <sup>(3)</sup>    | Battery supply current   | –   | –                  | 150 | nA    |
| R <sub>IN_TERM</sub> <sup>(4)</sup> | Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 (UNTUNED_SPLIT_40) | 28  | 40                 | 55  | Ω     |
|                                     | Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 (UNTUNED_SPLIT_50) | 35  | 50                 | 65  | Ω     |
|                                     | Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 (UNTUNED_SPLIT_60) | 44  | 60                 | 83  | Ω     |
| n                                   | Temperature diode ideality factor  | –   | 1.010              | –   | –     |
| r                                   | Temperature diode series resistance  | –   | 2                  | –   | Ω     |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V<sub>CCO</sub>/2 level.

Table 4: V<sub>IN</sub> Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks<sup>(1)(2)</sup>

| AC Voltage Overshoot    | % of UI at –55°C to 125°C | AC Voltage Undershoot | % of UI at –55°C to 125°C |
|-------------------------|---------------------------|-----------------------|---------------------------|
| V <sub>CCO</sub> + 0.55 | 100                       | –0.40                 | 100                       |
|                         |                           | –0.45                 | 61.7                      |
|                         |                           | –0.50                 | 25.8                      |
|                         |                           | –0.55                 | 11.0                      |
| V <sub>CCO</sub> + 0.60 | 46.6                      | –0.60                 | 4.77                      |
| V <sub>CCO</sub> + 0.65 | 21.2                      | –0.65                 | 2.10                      |
| V <sub>CCO</sub> + 0.70 | 9.75                      | –0.70                 | 0.94                      |
| V <sub>CCO</sub> + 0.75 | 4.55                      | –0.75                 | 0.43                      |
| V <sub>CCO</sub> + 0.80 | 2.15                      | –0.80                 | 0.20                      |
| V <sub>CCO</sub> + 0.85 | 1.02                      | –0.85                 | 0.09                      |
| V <sub>CCO</sub> + 0.90 | 0.49                      | –0.90                 | 0.04                      |
| V <sub>CCO</sub> + 0.95 | 0.24                      | –0.95                 | 0.02                      |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V<sub>CCO</sub> + 0.20V or below GND – 0.30V, must not exceed the values in this table.

Table 5: V<sub>IN</sub> Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks<sup>(1)(2)</sup>

| AC Voltage Overshoot    | % of UI at –55°C to 125°C | AC Voltage Undershoot | % of UI at –55°C to 125°C |
|-------------------------|---------------------------|-----------------------|---------------------------|
| V <sub>CCO</sub> + 0.55 | 100                       | –0.55                 | 100                       |
| V <sub>CCO</sub> + 0.60 | 50.0 <sup>(3)</sup>       | –0.60                 | 50.0 <sup>(3)</sup>       |
| V <sub>CCO</sub> + 0.65 | 50.0 <sup>(3)</sup>       | –0.65                 | 50.0 <sup>(3)</sup>       |
| V <sub>CCO</sub> + 0.70 | 47.0                      | –0.70                 | 50.0 <sup>(3)</sup>       |
| V <sub>CCO</sub> + 0.75 | 21.2                      | –0.75                 | 50.0 <sup>(3)</sup>       |

Table 5:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks<sup>(1)(2)</sup> (Cont'd)

| AC Voltage Overshoot | % of UI at -55°C to 125°C | AC Voltage Undershoot | % of UI at -55°C to 125°C |
|----------------------|---------------------------|-----------------------|---------------------------|
| $V_{CCO} + 0.80$     | 9.71                      | -0.80                 | 50.0 <sup>(3)</sup>       |
| $V_{CCO} + 0.85$     | 4.51                      | -0.85                 | 28.4                      |
| $V_{CCO} + 0.90$     | 2.12                      | -0.90                 | 12.7                      |
| $V_{CCO} + 0.95$     | 1.01                      | -0.95                 | 5.79                      |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above  $V_{CCO} + 0.20V$  or below  $GND - 0.30V$ , must not exceed the values in this table.
3. For UI lasting less than 20  $\mu s$ .

Table 6: Typical Quiescent Supply Current

| Symbol              | Description                          | Device   | Speed Grade |        |      |      |      | Units |
|---------------------|--------------------------------------|----------|-------------|--------|------|------|------|-------|
|                     |                                      |          | 1.0V        |        |      |      | 0.9V |       |
|                     |                                      |          | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| I <sub>CCINTQ</sub> | Quiescent $V_{CCINT}$ supply current | XC7K70T  | 241         | 241    | 241  | N/A  | 187  | mA    |
|                     |                                      | XC7K160T | 474         | 474    | 474  | N/A  | 368  | mA    |
|                     |                                      | XC7K325T | 810         | 810    | 810  | N/A  | 629  | mA    |
|                     |                                      | XC7K355T | 993         | 993    | 993  | N/A  | 771  | mA    |
|                     |                                      | XC7K410T | 1080        | 1080   | 1080 | N/A  | 838  | mA    |
|                     |                                      | XC7K420T | 1313        | 1313   | 1313 | N/A  | 1019 | mA    |
|                     |                                      | XC7K480T | 1313        | 1313   | 1313 | N/A  | 1019 | mA    |
|                     |                                      | XQ7K325T | N/A         | 810    | 810  | 810  | 629  | mA    |
|                     |                                      | XQ7K410T | N/A         | 1080   | 1080 | 1080 | 838  | mA    |
| I <sub>CCOQ</sub>   | Quiescent $V_{CCO}$ supply current   | XC7K70T  | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XC7K160T | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XC7K325T | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XC7K355T | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XC7K410T | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XC7K420T | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XC7K480T | 1           | 1      | 1    | N/A  | 1    | mA    |
|                     |                                      | XQ7K325T | N/A         | 1      | 1    | 1    | 1    | mA    |
|                     |                                      | XQ7K410T | N/A         | 1      | 1    | 1    | 1    | mA    |
| I <sub>CCAUXQ</sub> | Quiescent $V_{CCAUX}$ supply current | XC7K70T  | 21          | 21     | 21   | N/A  | 21   | mA    |
|                     |                                      | XC7K160T | 40          | 40     | 40   | N/A  | 40   | mA    |
|                     |                                      | XC7K325T | 68          | 68     | 68   | N/A  | 68   | mA    |
|                     |                                      | XC7K355T | 75          | 75     | 75   | N/A  | 75   | mA    |
|                     |                                      | XC7K410T | 85          | 85     | 85   | N/A  | 85   | mA    |
|                     |                                      | XC7K420T | 99          | 99     | 99   | N/A  | 99   | mA    |
|                     |                                      | XC7K480T | 99          | 99     | 99   | N/A  | 99   | mA    |
|                     |                                      | XQ7K325T | N/A         | 68     | 68   | 68   | 68   | mA    |
|                     |                                      | XQ7K410T | N/A         | 85     | 85   | 85   | 85   | mA    |

Table 6: Typical Quiescent Supply Current (Cont'd)

| Symbol                 | Description                                    | Device   | Speed Grade |        |     |     |      | Units |
|------------------------|--|----------|-------------|--------|-----|-----|------|-------|
|                        |  |          | 1.0V        |        |     |     | 0.9V |       |
|                        |  |          | -3          | -2/-2L | -1  | -1M | -2L  |       |
| I <sub>CCAUX_IOQ</sub> | Quiescent V <sub>CCAUX_IO</sub> supply current | XC7K70T  | N/A         | N/A    | N/A | N/A | N/A  | mA    |
|                        |  | XC7K160T | 2           | 2      | 2   | N/A | 2    | mA    |
|                        |  | XC7K325T | 2           | 2      | 2   | N/A | 2    | mA    |
|                        |  | XC7K355T | N/A         | N/A    | N/A | N/A | N/A  | mA    |
|                        |  | XC7K410T | 2           | 2      | 2   | N/A | 2    | mA    |
|                        |  | XC7K420T | N/A         | N/A    | N/A | N/A | N/A  | mA    |
|                        |  | XC7K480T | N/A         | N/A    | N/A | N/A | N/A  | mA    |
|                        |  | XQ7K325T | N/A         | 2      | 2   | 2   | 2    | mA    |
|                        |  | XQ7K410T | N/A         | 2      | 2   | 2   | 2    | mA    |
| I <sub>CCBRAMQ</sub>   | Quiescent V <sub>CCBRAM</sub> supply current   | XC7K70T  | 6           | 6      | 6   | N/A | 6    | mA    |
|                        |  | XC7K160T | 14          | 14     | 14  | N/A | 14   | mA    |
|                        |  | XC7K325T | 19          | 19     | 19  | N/A | 19   | mA    |
|                        |  | XC7K355T | 31          | 31     | 31  | N/A | 31   | mA    |
|                        |  | XC7K410T | 34          | 34     | 34  | N/A | 34   | mA    |
|                        |  | XC7K420T | 41          | 41     | 41  | N/A | 41   | mA    |
|                        |  | XC7K480T | 41          | 41     | 41  | N/A | 41   | mA    |
|                        |  | XQ7K325T | N/A         | 19     | 19  | 19  | 19   | mA    |
|                        |  | XQ7K410T | N/A         | 34     | 34  | 34  | 34   | mA    |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T<sub>j</sub>) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at [www.xilinx.com/power](http://www.xilinx.com/power)) to calculate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V<sub>CCINT</sub>, V<sub>CCBRAM</sub>, V<sub>CCAUX</sub>, V<sub>CCAUX\_IO</sub>, and V<sub>CCO</sub> to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V<sub>CCINT</sub> and V<sub>CCBRAM</sub> have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V<sub>CCAUX</sub>, V<sub>CCAUX\_IO</sub>, and V<sub>CCO</sub> have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V<sub>CCO</sub> voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V<sub>CCO</sub> and V<sub>CCAUX</sub> must not exceed 2.625V for longer than T<sub>VCCO2VCCAUX</sub> for each power-on/off cycle to maintain device reliability levels.
- The T<sub>VCCO2VCCAUX</sub> time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V<sub>CCINT</sub>, V<sub>MGTAVCC</sub>, V<sub>MGTAVTT</sub> OR V<sub>MGTAVCC</sub>, V<sub>CCINT</sub>, V<sub>MGTAVTT</sub>. There is no recommended sequencing for V<sub>MGTVCCAUX</sub>. Both V<sub>MGTAVCC</sub> and V<sub>CCINT</sub> can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V<sub>MGTAVTT</sub> can be higher than specifications during power-up and power-down.

- When  $V_{MGTAVTT}$  is powered before  $V_{MGTAVCC}$  and  $V_{MGTAVTT} - V_{MGTAVCC} > 150$  mV and  $V_{MGTAVCC} < 0.7$ V, the  $V_{MGTAVTT}$  current draw can increase by 460 mA per transceiver during  $V_{MGTAVCC}$  ramp up. The duration of the current draw can be up to  $0.3 \times T_{MGTAVCC}$  (ramp time from GND to 90% of  $V_{MGTAVCC}$ ). The reverse is true for power-down.
- When  $V_{MGTAVTT}$  is powered before  $V_{CCINT}$  and  $V_{MGTAVTT} - V_{CCINT} > 150$  mV and  $V_{CCINT} < 0.7$ V, the  $V_{MGTAVTT}$  current draw can increase by 50 mA per transceiver during  $V_{CCINT}$  ramp up. The duration of the current draw can be up to  $0.3 \times T_{VCCINT}$  (ramp time from GND to 90% of  $V_{CCINT}$ ). The reverse is true for power-down.

Table 7 shows the minimum current, in addition to  $I_{CCQ}$ , that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after  $V_{CCINT}$  is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at [www.xilinx.com/power](http://www.xilinx.com/power)) to estimate current drain on these supplies.

Table 7: Power-On Current for Kintex-7 Devices

| Device   | $I_{CCINTMIN}$      | $I_{CCAUXMIN}$     | $I_{CCOMIN}$                | $I_{CCAUX_IOMIN}$                 | $I_{CCBRAMMIN}$     | Units |
|----------|---------------------|--------------------|-----------------------------|-----------------------------------|---------------------|-------|
| XC7K70T  | $I_{CCINTQ} + 450$  | $I_{CCAUXQ} + 40$  | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 40$  | mA    |
| XC7K160T | $I_{CCINTQ} + 550$  | $I_{CCAUXQ} + 50$  | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 40$  | mA    |
| XC7K325T | $I_{CCINTQ} + 600$  | $I_{CCAUXQ} + 80$  | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 40$  | mA    |
| XC7K355T | $I_{CCINTQ} + 1450$ | $I_{CCAUXQ} + 109$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 81$  | mA    |
| XC7K410T | $I_{CCINTQ} + 1500$ | $I_{CCAUXQ} + 125$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 90$  | mA    |
| XC7K420T | $I_{CCINTQ} + 2200$ | $I_{CCAUXQ} + 180$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 108$ | mA    |
| XC7K480T | $I_{CCINTQ} + 2200$ | $I_{CCAUXQ} + 180$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 108$ | mA    |
| XQ7K325T | $I_{CCINTQ} + 600$  | $I_{CCAUXQ} + 80$  | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 40$  | mA    |
| XQ7K410T | $I_{CCINTQ} + 1500$ | $I_{CCAUXQ} + 125$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUXXIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 90$  | mA    |

Table 8: Power Supply Ramp Time

| Symbol            | Description  | Conditions                      | Min | Max | Units |
|-------------------|--|---------------------------------|-----|-----|-------|
| $T_{VCCINT}$      | Ramp time from GND to 90% of $V_{CCINT}$                         |                                 | 0.2 | 50  | ms    |
| $T_{VCCO}$        | Ramp time from GND to 90% of $V_{CCO}$                           |                                 | 0.2 | 50  | ms    |
| $T_{VCCAUX}$      | Ramp time from GND to 90% of $V_{CCAUX}$                         |                                 | 0.2 | 50  | ms    |
| $T_{VCCAUX_IO}$   | Ramp time from GND to 90% of $V_{CCAUX_IO}$                      |                                 | 0.2 | 50  | ms    |
| $T_{VCCBRAM}$     | Ramp time from GND to 90% of $V_{CCBRAM}$                        |                                 | 0.2 | 50  | ms    |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625$ V | $T_J = 125^\circ\text{C}^{(1)}$ | –   | 300 | ms    |
|                   |  | $T_J = 100^\circ\text{C}^{(1)}$ | –   | 500 |       |
|                   |  | $T_J = 85^\circ\text{C}^{(1)}$  | –   | 800 |       |
| $T_{MGTAVCC}$     | Ramp time from GND to 90% of $V_{MGTAVCC}$                       |                                 | 0.2 | 50  | ms    |
| $T_{MGTAVTT}$     | Ramp time from GND to 90% of $V_{MGTAVTT}$                       |                                 | 0.2 | 50  | ms    |
| $T_{MGTVCCAUX}$   | Ramp time from GND to 90% of $V_{MGTVCCAUX}$                     |                                 | 0.2 | 50  | ms    |

Notes:

1. Based on 240,000 power cycles with nominal  $V_{CCO}$  of 3.3V or 36,500 power cycles with a worst case  $V_{CCO}$  of 3.465V.

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels (1)(2)

| I/O Standard           | $V_{IL}$ |                   | $V_{IH}$          |                   | $V_{OL}$            | $V_{OH}$            | $I_{OL}$ | $I_{OH}$ |
|------------------------|----------|-------------------|-------------------|-------------------|---------------------|---------------------|----------|----------|
|                        | V, Min   | V, Max            | V, Min            | V, Max            | V, Max              | V, Min              | mA       | mA       |
| HSTL_I                 | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 8        | -8       |
| HSTL_I_12              | -0.300   | $V_{REF} - 0.080$ | $V_{REF} + 0.080$ | $V_{CCO} + 0.300$ | 25% $V_{CCO}$       | 75% $V_{CCO}$       | 6.3      | -6.3     |
| HSTL_I_18              | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 8        | -8       |
| HSTL_II                | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 16       | -16      |
| HSTL_II_18             | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 16       | -16      |
| HSUL_12                | -0.300   | $V_{REF} - 0.130$ | $V_{REF} + 0.130$ | $V_{CCO} + 0.300$ | 20% $V_{CCO}$       | 80% $V_{CCO}$       | 0.1      | -0.1     |
| LVC MOS12              | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | Note 3   | Note 3   |
| LVC MOS15,<br>LVDCI_15 | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 25% $V_{CCO}$       | 75% $V_{CCO}$       | Note 4   | Note 4   |
| LVC MOS18,<br>LVDCI_18 | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.450               | $V_{CCO} - 0.450$   | Note 5   | Note 5   |
| LVC MOS25              | -0.300   | 0.700             | 1.700             | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | Note 6   | Note 6   |
| LVC MOS33              | -0.300   | 0.800             | 2.000             | 3.450             | 0.400               | $V_{CCO} - 0.400$   | Note 6   | Note 6   |
| LV TTL                 | -0.300   | 0.800             | 2.000             | 3.450             | 0.400               | 2.400               | Note 7   | Note 7   |
| MOBILE_DDR             | -0.300   | 20% $V_{CCO}$     | 80% $V_{CCO}$     | $V_{CCO} + 0.300$ | 10% $V_{CCO}$       | 90% $V_{CCO}$       | 0.1      | -0.1     |
| PCI33_3                | -0.400   | 30% $V_{CCO}$     | 50% $V_{CCO}$     | $V_{CCO} + 0.500$ | 10% $V_{CCO}$       | 90% $V_{CCO}$       | 1.5      | -0.5     |
| SSTL12                 | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 14.25    | -14.25   |
| SSTL135                | -0.300   | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 13.0     | -13.0    |
| SSTL135_R              | -0.300   | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 8.9      | -8.9     |
| SSTL15                 | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 13.0     | -13.0    |
| SSTL15_R               | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 8.9      | -8.9     |
| SSTL18_I               | -0.300   | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.470$ | $V_{CCO}/2 + 0.470$ | 8        | -8       |
| SSTL18_II              | -0.300   | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.600$ | $V_{CCO}/2 + 0.600$ | 13.4     | -13.4    |

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).



Table 10: Differential SelectIO DC Input and Output Levels

| I/O Standard | V <sub>ICM</sub> <sup>(1)</sup> |        |                    | V <sub>ID</sub> <sup>(2)</sup> |        |        | V <sub>OCM</sub> <sup>(3)</sup> |                         |                         | V <sub>OD</sub> <sup>(4)</sup> |        |        |
|--------------|---------------------------------|--------|--------------------|--------------------------------|--------|--------|---------------------------------|-------------------------|-------------------------|--------------------------------|--------|--------|
|              | V, Min                          | V, Typ | V, Max             | V, Min                         | V, Typ | V, Max | V, Min                          | V, Typ                  | V, Max                  | V, Min                         | V, Typ | V, Max |
| BLVDS_25     | 0.300                           | 1.200  | 1.425              | 0.100                          | –      | –      | –                               | 1.250                   | –                       | Note 5                         |        |        |
| MINI_LVDS_25 | 0.300                           | 1.200  | V <sub>CCAUX</sub> | 0.200                          | 0.400  | 0.600  | 1.000                           | 1.200                   | 1.400                   | 0.300                          | 0.450  | 0.600  |
| PPDS_25      | 0.200                           | 0.900  | V <sub>CCAUX</sub> | 0.100                          | 0.250  | 0.400  | 0.500                           | 0.950                   | 1.400                   | 0.100                          | 0.250  | 0.400  |
| RSDS_25      | 0.300                           | 0.900  | 1.500              | 0.100                          | 0.350  | 0.600  | 1.000                           | 1.200                   | 1.400                   | 0.100                          | 0.350  | 0.600  |
| TMDS_33      | 2.700                           | 2.965  | 3.230              | 0.150                          | 0.675  | 1.200  | V <sub>CCO</sub> –0.405         | V <sub>CCO</sub> –0.300 | V <sub>CCO</sub> –0.190 | 0.400                          | 0.600  | 0.800  |

**Notes:**

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage (Q –  $\bar{Q}$ ).
3. V<sub>OCM</sub> is the output common mode voltage.
4. V<sub>OD</sub> is the output differential voltage (Q –  $\bar{Q}$ ).
5. V<sub>OD</sub> for BLVDS will vary significantly depending on topology and loading.
6. LVDS\_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

| I/O Standard    | V <sub>ICM</sub> <sup>(1)</sup> |        |        | V <sub>ID</sub> <sup>(2)</sup> |        | V <sub>OL</sub> <sup>(3)</sup> | V <sub>OH</sub> <sup>(4)</sup> | I <sub>OL</sub> | I <sub>OH</sub> |
|-----------------|---------------------------------|--------|--------|--------------------------------|--------|--------------------------------|--------------------------------|-----------------|-----------------|
|                 | V, Min                          | V, Typ | V, Max | V, Min                         | V, Max | V, Max                         | V, Min                         | mA, Max         | mA, Min         |
| DIFF_HSTL_I     | 0.300                           | 0.750  | 1.125  | 0.100                          | –      | 0.400                          | V <sub>CCO</sub> –0.400        | 8.00            | –8.00           |
| DIFF_HSTL_I_18  | 0.300                           | 0.900  | 1.425  | 0.100                          | –      | 0.400                          | V <sub>CCO</sub> –0.400        | 8.00            | –8.00           |
| DIFF_HSTL_II    | 0.300                           | 0.750  | 1.125  | 0.100                          | –      | 0.400                          | V <sub>CCO</sub> –0.400        | 16.00           | –16.00          |
| DIFF_HSTL_II_18 | 0.300                           | 0.900  | 1.425  | 0.100                          | –      | 0.400                          | V <sub>CCO</sub> –0.400        | 16.00           | –16.00          |
| DIFF_HSUL_12    | 0.300                           | 0.600  | 0.850  | 0.100                          | –      | 20% V <sub>CCO</sub>           | 80% V <sub>CCO</sub>           | 0.100           | –0.100          |
| DIFF_MOBILE_DDR | 0.300                           | 0.900  | 1.425  | 0.100                          | –      | 10% V <sub>CCO</sub>           | 90% V <sub>CCO</sub>           | 0.100           | –0.100          |
| DIFF_SSTL12     | 0.300                           | 0.600  | 0.850  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.150  | (V <sub>CCO</sub> /2) + 0.150  | 14.25           | –14.25          |
| DIFF_SSTL135    | 0.300                           | 0.675  | 1.000  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.150  | (V <sub>CCO</sub> /2) + 0.150  | 13.0            | –13.0           |
| DIFF_SSTL135_R  | 0.300                           | 0.675  | 1.000  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.150  | (V <sub>CCO</sub> /2) + 0.150  | 8.9             | –8.9            |
| DIFF_SSTL15     | 0.300                           | 0.750  | 1.125  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.175  | (V <sub>CCO</sub> /2) + 0.175  | 13.0            | –13.0           |
| DIFF_SSTL15_R   | 0.300                           | 0.750  | 1.125  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.175  | (V <sub>CCO</sub> /2) + 0.175  | 8.9             | –8.9            |
| DIFF_SSTL18_I   | 0.300                           | 0.900  | 1.425  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.470  | (V <sub>CCO</sub> /2) + 0.470  | 8.00            | –8.00           |
| DIFF_SSTL18_II  | 0.300                           | 0.900  | 1.425  | 0.100                          | –      | (V <sub>CCO</sub> /2) – 0.600  | (V <sub>CCO</sub> /2) + 0.600  | 13.4            | –13.4           |

**Notes:**

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage (Q –  $\bar{Q}$ ).
3. V<sub>OL</sub> is the single-ended low-output voltage.
4. V<sub>OH</sub> is the single-ended high-output voltage.

## LVDS DC Specifications (LVDS\_25)

The LVDS\_25 standard is available in the HR I/O banks. See the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

Table 12: LVDS\_25 DC Specifications

| Symbol      | DC Parameter   | Conditions  | Min   | Typ   | Max   | Units |
|-------------|--|---|-------|-------|-------|-------|
| $V_{CCO}$   | Supply Voltage   |   | 2.375 | 2.500 | 2.625 | V     |
| $V_{OH}$    | Output High Voltage for Q and $\bar{Q}$  | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | –     | –     | 1.675 | V     |
| $V_{OL}$    | Output Low Voltage for Q and $\bar{Q}$   | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | 0.700 | –     | –     | V     |
| $V_{ODIFF}$ | Differential Output Voltage:<br>(Q – $\bar{Q}$ ), Q = High<br>( $\bar{Q}$ – Q), $\bar{Q}$ = High | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | 247   | 350   | 600   | mV    |
| $V_{OCM}$   | Output Common-Mode Voltage   | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | 1.000 | 1.250 | 1.425 | V     |
| $V_{IDIFF}$ | Differential Input Voltage:<br>(Q – $\bar{Q}$ ), Q = High<br>( $\bar{Q}$ – Q), $\bar{Q}$ = High  |   | 100   | 350   | 600   | mV    |
| $V_{ICM}$   | Input Common-Mode Voltage  |   | 0.300 | 1.200 | 1.425 | V     |

**Notes:**

1. Differential inputs for LVDS\_25 can be placed in banks with  $V_{CCO}$  levels that are different from the required level for outputs. Refer to the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

## LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

Table 13: LVDS DC Specifications

| Symbol      | DC Parameter   | Conditions  | Min   | Typ   | Max   | Units |
|-------------|--|---|-------|-------|-------|-------|
| $V_{CCO}$   | Supply Voltage   |   | 1.710 | 1.800 | 1.890 | V     |
| $V_{OH}$    | Output High Voltage for Q and $\bar{Q}$  | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | –     | –     | 1.675 | V     |
| $V_{OL}$    | Output Low Voltage for Q and $\bar{Q}$   | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | 0.825 | –     | –     | V     |
| $V_{ODIFF}$ | Differential Output Voltage:<br>(Q – $\bar{Q}$ ), Q = High<br>( $\bar{Q}$ – Q), $\bar{Q}$ = High | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | 247   | 350   | 600   | mV    |
| $V_{OCM}$   | Output Common-Mode Voltage   | $R_T = 100 \Omega$ across Q and $\bar{Q}$ signals | 1.000 | 1.250 | 1.425 | V     |
| $V_{IDIFF}$ | Differential Input Voltage:<br>(Q – $\bar{Q}$ ), Q = High<br>( $\bar{Q}$ – Q), $\bar{Q}$ = High  | Common-mode input voltage = 1.25V                 | 100   | 350   | 600   | mV    |
| $V_{ICM}$   | Input Common-Mode Voltage  | Differential input voltage = $\pm 350$ mV         | 0.300 | 1.200 | 1.425 | V     |

**Notes:**

1. Differential inputs for LVDS can be placed in banks with  $V_{CCO}$  levels that are different from the required level for outputs. Refer to the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite 2013.4 and ISE® software 14.7 as outlined in [Table 14](#).

Table 14: Kintex-7 FPGA Speed Specification Version By Device

| Version In: |               | Typical $V_{CCINT}$<br>(Table 2) | Device  |
|-------------|---------------|----------------------------------|---|
| ISE 14.7    | Vivado 2013.4 |                                  |   |
| 1.10        | 1.11          | 1.0V                             | XC7K70T, XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T |
| 1.09        | 1.09          | 0.9V                             | XC7K70T, XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T |
| 1.05        | 1.06          | 1.0V                             | XQ7K325T, XQ7K410T  |
| 1.05        | 1.05          | 0.9V                             | XQ7K325T, XQ7K410T  |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 15](#) correlates the current status of each Kintex-7 device on a per speed grade basis.

Table 15: Kintex-7 Device Speed Grade Designations

| Device   | Speed Grade Designations |   |   |
|----------|--------------------------|---|---|
|          | Advance                  | Preliminary                             | Production                              |
| XC7K70T  |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XC7K160T |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XC7K325T |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XC7K355T |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XC7K410T |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XC7K420T |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XC7K480T |                          |   | -3, -2, -2L(1.0V), -1, and -2L (0.9V)   |
| XQ7K325T |                          |   | -2I, -2L(1.0V), -1I, -2L(0.9V), and -1M |
| XQ7K410T |                          | -2I, -2L(1.0V), -1I, -2L(0.9V), and -1M |   |

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 16](#) lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: Kintex-7 Device Production Software and Speed Specification Release

| Device   | Speed Grade Designations                          |   |     |   |
|----------|---|---|-----|---|
|          | 1.0V  |   |     | 0.9V <sup>(1)</sup>                               |
|          | -3  | -2/-2L  | -1  | -1M   |
| XC7K70T  | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XC7K160T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XC7K325T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XC7K355T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XC7K410T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XC7K420T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XC7K480T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 |   | N/A | Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06 |
| XQ7K325T | N/A   | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 |     | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 |
| XQ7K410T | N/A   |   |     |   |

### Notes:

- In the software, -2L (0.9V) designs are distinguished from -2L (1.0V) designs via an additional "L" following the device name, e.g., XC7K325TL is the device name for a -2L (0.9V) design and XC7K325T is the part name for a -2L (1.0V) design. For the -2L (0.9V) speed specification, select the Kintex-7 Low Voltage family in the software.
- Blank entries indicate a device and/or speed grade in advance or preliminary status.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 11](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

*Table 17: Networking Applications Interface Performances*

| Description  | I/O Bank Type | Speed Grade |        |      |      | Units |
|--|---------------|-------------|--------|------|------|-------|
|  |               | 1.0V        |        |      | 0.9V |       |
|  |               | -3          | -2/-2L | -1   | -2L  |       |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)  | HR            | 710         | 710    | 625  | 625  | Mb/s  |
|  | HP            | 710         | 710    | 625  | 625  | Mb/s  |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | HR            | 1250        | 1250   | 950  | 950  | Mb/s  |
|  | HP            | 1600        | 1400   | 1250 | 1250 | Mb/s  |
| SDR LVDS receiver (SFI-4.1) <sup>(1)</sup>                 | HR            | 710         | 710    | 625  | 625  | Mb/s  |
|  | HP            | 710         | 710    | 625  | 625  | Mb/s  |
| DDR LVDS receiver (SPI-4.2) <sup>(1)</sup>                 | HR            | 1250        | 1250   | 950  | 950  | Mb/s  |
|  | HP            | 1600        | 1400   | 1250 | 1250 | Mb/s  |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FFG and RF Packages)<sup>(1)(2)</sup>

| Memory Standard               | I/O Bank Type | V <sub>CCAUX_IO</sub> | Speed Grade |        |      |      |      | Units |
|-------------------------------|---------------|-----------------------|-------------|--------|------|------|------|-------|
|                               |               |                       | 1.0V        |        |      |      | 0.9V |       |
|                               |               |                       | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| <b>4:1 Memory Controllers</b> |               |                       |             |        |      |      |      |       |
| DDR3                          | HP            | 2.0V                  | 1866        | 1866   | 1600 | 1066 | 1333 | Mb/s  |
|                               | HP            | 1.8V                  | 1600        | 1333   | 1066 | 800  | 1066 | Mb/s  |
|                               | HR            | N/A                   | 1066        | 1066   | 800  | 800  | 800  | Mb/s  |
| DDR3L                         | HP            | 2.0V                  | 1600        | 1600   | 1333 | 1066 | 1066 | Mb/s  |
|                               | HP            | 1.8V                  | 1333        | 1066   | 800  | 800  | 800  | Mb/s  |
|                               | HR            | N/A                   | 800         | 800    | 667  | N/A  | 667  | Mb/s  |
| DDR2                          | HP            | 2.0V                  | 800         | 800    | 800  | 667  | 800  | Mb/s  |
|                               | HP            | 1.8V                  | 800         | 800    | 800  | 667  | 800  | Mb/s  |
|                               | HR            | N/A                   | 800         | 800    | 800  | 533  | 800  | Mb/s  |
| RLDRAM III                    | HP            | 2.0V                  | 800         | 667    | 667  | 550  | 533  | MHz   |
|                               | HP            | 1.8V                  | 550         | 500    | 450  | 400  | 450  | MHz   |
|                               | HR            | N/A                   | N/A         |        |      |      |      |       |
| <b>2:1 Memory Controllers</b> |               |                       |             |        |      |      |      |       |
| DDR3                          | HP            | 2.0V                  | 1066        | 1066   | 800  | 667  | 800  | Mb/s  |
|                               | HP            | 1.8V                  | 1066        | 1066   | 800  | 667  | 800  | Mb/s  |
|                               | HR            | N/A                   | 1066        | 1066   | 800  | 667  | 800  | Mb/s  |
| DDR3L                         | HP            | 2.0V                  | 1066        | 1066   | 800  | 667  | 800  | Mb/s  |
|                               | HP            | 1.8V                  | 1066        | 1066   | 800  | 667  | 800  | Mb/s  |
|                               | HR            | N/A                   | 800         | 800    | 667  | N/A  | 667  | Mb/s  |
| DDR2                          | HP            | 2.0V                  | 800         | 800    | 800  | 667  | 800  | Mb/s  |
|                               | HP            | 1.8V                  |             |        |      | 667  |      |       |
|                               | HR            | N/A                   |             |        |      | 533  |      |       |
| QDR II+ <sup>(3)</sup>        | HP            | 2.0V                  | 550         | 500    | 450  | 300  | 450  | MHz   |
|                               | HP            | 1.8V                  | 500         | 450    | 400  | 300  | 400  | MHz   |
|                               | HR            | N/A                   |             |        |      |      |      |       |
| RLDRAM II                     | HP            | 2.0V                  | 533         | 500    | 450  | 400  | 450  | MHz   |
|                               | HP            | 1.8V                  |             |        |      |      |      |       |
|                               | HR            | N/A                   |             |        |      |      |      |       |
| LPDDR2                        | HP            | 2.0V                  | 667         | 667    | 667  | 533  | 667  | Mb/s  |
|                               | HP            | 1.8V                  | 667         | 667    | 667  | 533  | 667  | Mb/s  |
|                               | HR            | N/A                   | 667         | 667    | 667  | 533  | 667  | Mb/s  |

**Notes:**

1. V<sub>REF</sub> tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V<sub>REF</sub> the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 19: Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FBG Packages)<sup>(1)(2)</sup>

| Memory Standard               | I/O Bank Type | V <sub>CCAUX_IO</sub> <sup>(3)</sup> | Speed Grade |        |     |     |      | Units |
|-------------------------------|---------------|--------------------------------------|-------------|--------|-----|-----|------|-------|
|                               |               |                                      | 1.0V        |        |     |     | 0.9V |       |
|                               |               |                                      | -3          | -2/-2L | -1  | -1M | -2L  |       |
| <b>4:1 Memory Controllers</b> |               |                                      |             |        |     |     |      |       |
| DDR3                          | HP            | N/A                                  | 1333        | 1066   | 800 | 800 | 800  | Mb/s  |
|                               | HR            | N/A                                  | 1066        | 800    | 800 | 800 | 800  | Mb/s  |
| DDR3L                         | HP            | N/A                                  | 1066        | 800    | 667 | 667 | 667  | Mb/s  |
|                               | HR            | N/A                                  | 800         | 800    | 667 | N/A | 667  | Mb/s  |
| DDR2                          | HP            | N/A                                  | 800         | 800    | 800 | 667 | 800  | Mb/s  |
|                               | HR            | N/A                                  | 800         | 667    | 667 | 533 | 667  | Mb/s  |
| RLDRAM III                    | HP            | N/A                                  | 550         | 500    | 450 | 350 | 450  | MHz   |
|                               | HR            | N/A                                  | N/A         |        |     |     |      |       |
| <b>2:1 Memory Controllers</b> |               |                                      |             |        |     |     |      |       |
| DDR3                          | HP            | N/A                                  | 1066        | 1066   | 800 | 667 | 800  | Mb/s  |
|                               | HR            | N/A                                  | 1066        | 800    | 800 | 667 | 800  | Mb/s  |
| DDR3L                         | HP            | N/A                                  | 1066        | 800    | 667 | 667 | 667  | Mb/s  |
|                               | HR            | N/A                                  | 800         | 800    | 667 | N/A | 667  | Mb/s  |
| DDR2                          | HP            | N/A                                  | 800         | 800    | 800 | 667 | 800  | Mb/s  |
|                               | HR            | N/A                                  | 800         | 667    | 667 | 533 | 667  | Mb/s  |
| QDR II+ <sup>(4)</sup>        | HP            | N/A                                  | 550         | 500    | 450 | 300 | 450  | MHz   |
|                               | HR            | N/A                                  | 450         | 400    | 350 | 300 | 350  | MHz   |
| RLDRAM II                     | HP            | N/A                                  | 533         | 500    | 450 | 400 | 450  | MHz   |
|                               | HR            | N/A                                  |             |        |     |     |      |       |
| LPDDR2                        | HP            | N/A                                  | 667         | 667    | 667 | 400 | 667  | Mb/s  |
|                               | HR            | N/A                                  | 667         | 667    | 533 | 400 | 533  | Mb/s  |

**Notes:**

1. V<sub>REF</sub> tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* ([UG586](#)).
2. When using the internal V<sub>REF</sub> the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V<sub>CCAUX\_IO</sub> supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

### IOB Pad Input/Output/3-State

Table 20 (3.3V high-range IOB (HR)) and Table 21 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than  $T_{IOTP}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the IN\_TERM termination turn-on time is always faster than  $T_{IOTP}$  when the INTERMDISABLE pin is used.

Table 20: 3.3V IOB High Range (HR) Switching Characteristics

| I/O Standard             | $T_{IOPI}$  |        |      |      |      | $T_{IOOP}$  |        |      |      |      | $T_{IOTP}$  |        |      |      |      | Units |
|--------------------------|-------------|--------|------|------|------|-------------|--------|------|------|------|-------------|--------|------|------|------|-------|
|                          | Speed Grade |        |      |      |      | Speed Grade |        |      |      |      | Speed Grade |        |      |      |      |       |
|                          | 1.0V        |        |      |      | 0.9V | 1.0V        |        |      |      | 0.9V | 1.0V        |        |      |      | 0.9V |       |
|                          | -3          | -2/-2L | -1   | -1M  | -2L  | -3          | -2/-2L | -1   | -1M  | -2L  | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| LVTTL_S4                 | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 3.77        | 3.90   | 4.00 | 4.00 | 4.13 | 3.52        | 3.67   | 3.86 | 3.86 | 3.85 | ns    |
| LVTTL_S8                 | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 3.50        | 3.64   | 3.73 | 3.73 | 3.86 | 3.26        | 3.40   | 3.60 | 3.60 | 3.58 | ns    |
| LVTTL_S12                | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 3.49        | 3.62   | 3.72 | 3.72 | 3.84 | 3.24        | 3.39   | 3.58 | 3.58 | 3.56 | ns    |
| LVTTL_S16                | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 3.03        | 3.17   | 3.26 | 3.26 | 3.39 | 2.79        | 2.93   | 3.13 | 3.13 | 3.11 | ns    |
| LVTTL_S24                | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 3.25        | 3.39   | 3.48 | 3.48 | 3.61 | 3.01        | 3.15   | 3.35 | 3.35 | 3.33 | ns    |
| LVTTL_F4                 | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 3.22        | 3.36   | 3.45 | 3.45 | 3.58 | 2.98        | 3.12   | 3.32 | 3.32 | 3.30 | ns    |
| LVTTL_F8                 | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 2.71        | 2.84   | 2.93 | 2.93 | 3.06 | 2.46        | 2.61   | 2.80 | 2.80 | 2.78 | ns    |
| LVTTL_F12                | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 2.69        | 2.82   | 2.92 | 2.92 | 3.05 | 2.44        | 2.59   | 2.79 | 2.79 | 2.77 | ns    |
| LVTTL_F16                | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 2.57        | 2.85   | 3.15 | 3.15 | 2.88 | 2.33        | 2.61   | 3.02 | 3.02 | 2.60 | ns    |
| LVTTL_F24                | 1.31        | 1.42   | 1.64 | 1.64 | 1.51 | 2.41        | 2.64   | 2.89 | 3.04 | 2.94 | 2.16        | 2.41   | 2.76 | 2.91 | 2.66 | ns    |
| LVDS_25                  | 0.64        | 0.68   | 0.80 | 0.87 | 0.83 | 1.36        | 1.47   | 1.55 | 1.55 | 1.58 | 1.11        | 1.24   | 1.41 | 1.41 | 1.30 | ns    |
| MINI_LVDS_25             | 0.68        | 0.70   | 0.79 | 0.87 | 0.83 | 1.36        | 1.47   | 1.55 | 1.55 | 1.59 | 1.11        | 1.24   | 1.41 | 1.41 | 1.31 | ns    |
| BLVDS_25                 | 0.65        | 0.69   | 0.80 | 0.85 | 0.83 | 1.83        | 2.02   | 2.20 | 2.57 | 2.16 | 1.59        | 1.79   | 2.07 | 2.44 | 1.88 | ns    |
| RSDS_25 (point to point) | 0.63        | 0.68   | 0.79 | 0.87 | 0.83 | 1.36        | 1.48   | 1.55 | 1.55 | 1.59 | 1.11        | 1.24   | 1.41 | 1.41 | 1.31 | ns    |
| PPDS_25                  | 0.65        | 0.69   | 0.80 | 0.87 | 0.83 | 1.36        | 1.49   | 1.58 | 1.58 | 1.59 | 1.11        | 1.25   | 1.45 | 1.45 | 1.31 | ns    |
| TMDS_33                  | 0.72        | 0.76   | 0.86 | 0.90 | 0.83 | 1.43        | 1.54   | 1.60 | 1.60 | 1.70 | 1.18        | 1.31   | 1.47 | 1.47 | 1.42 | ns    |
| PCI33_3                  | 1.28        | 1.41   | 1.65 | 1.65 | 1.50 | 2.71        | 3.08   | 3.52 | 3.52 | 3.42 | 2.46        | 2.84   | 3.39 | 3.39 | 3.14 | ns    |
| HSUL_12_S                | 0.63        | 0.64   | 0.71 | 0.85 | 0.79 | 1.77        | 1.90   | 2.00 | 2.00 | 2.13 | 1.52        | 1.67   | 1.86 | 1.86 | 1.85 | ns    |
| HSUL_12_F                | 0.63        | 0.64   | 0.71 | 0.85 | 0.79 | 1.26        | 1.40   | 1.50 | 1.50 | 1.61 | 1.01        | 1.16   | 1.37 | 1.37 | 1.33 | ns    |
| DIFF_HSUL_12_S           | 0.58        | 0.61   | 0.70 | 0.84 | 0.81 | 1.55        | 1.68   | 1.78 | 1.78 | 1.92 | 1.30        | 1.45   | 1.65 | 1.65 | 1.64 | ns    |
| DIFF_HSUL_12_F           | 0.58        | 0.61   | 0.70 | 0.84 | 0.81 | 1.16        | 1.28   | 1.35 | 1.35 | 1.50 | 0.92        | 1.04   | 1.21 | 1.21 | 1.22 | ns    |
| MOBILE_DDR_S             | 0.64        | 0.66   | 0.74 | 0.74 | 0.89 | 2.58        | 2.91   | 3.31 | 3.31 | 1.95 | 2.33        | 2.68   | 3.17 | 3.17 | 1.67 | ns    |
| MOBILE_DDR_F             | 0.64        | 0.66   | 0.74 | 0.74 | 0.89 | 1.91        | 2.13   | 2.36 | 2.36 | 1.69 | 1.66        | 1.89   | 2.23 | 2.23 | 1.41 | ns    |
| DIFF_MOBILE_DDR_S        | 0.63        | 0.66   | 0.75 | 0.75 | 0.79 | 2.51        | 2.84   | 3.24 | 3.24 | 1.95 | 2.26        | 2.61   | 3.10 | 3.10 | 1.67 | ns    |
| DIFF_MOBILE_DDR_F        | 0.63        | 0.66   | 0.75 | 0.75 | 0.79 | 1.89        | 2.11   | 2.34 | 2.34 | 1.72 | 1.64        | 1.88   | 2.21 | 2.21 | 1.44 | ns    |
| HSTL_I_S                 | 0.61        | 0.64   | 0.73 | 0.84 | 0.79 | 1.55        | 1.69   | 1.80 | 1.80 | 1.91 | 1.30        | 1.46   | 1.67 | 1.67 | 1.63 | ns    |
| HSTL_II_S                | 0.61        | 0.64   | 0.73 | 0.84 | 0.78 | 1.21        | 1.34   | 1.43 | 1.61 | 1.70 | 0.96        | 1.11   | 1.30 | 1.47 | 1.42 | ns    |
| HSTL_I_18_S              | 0.64        | 0.67   | 0.76 | 0.85 | 0.79 | 1.28        | 1.39   | 1.45 | 1.45 | 1.58 | 1.04        | 1.16   | 1.31 | 1.32 | 1.30 | ns    |



Table 20: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

| I/O Standard      | T <sub>IOPI</sub> |        |      |      |      | T <sub>IOOP</sub> |        |      |      |      | T <sub>IOTP</sub> |        |      |      |      | Units |
|-------------------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------|
|                   | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      |       |
|                   | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V |       |
|                   | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  |       |
| HSTL_II_18_S      | 0.64              | 0.67   | 0.76 | 0.85 | 0.79 | 1.18              | 1.31   | 1.40 | 1.57 | 1.69 | 0.93              | 1.08   | 1.27 | 1.44 | 1.41 | ns    |
| DIFF_HSTL_I_S     | 0.63              | 0.67   | 0.77 | 0.84 | 0.78 | 1.42              | 1.54   | 1.61 | 1.78 | 1.84 | 1.17              | 1.31   | 1.48 | 1.65 | 1.56 | ns    |
| DIFF_HSTL_II_S    | 0.63              | 0.67   | 0.77 | 0.84 | 0.79 | 1.15              | 1.24   | 1.27 | 1.61 | 1.78 | 0.91              | 1.01   | 1.14 | 1.47 | 1.50 | ns    |
| DIFF_HSTL_I_18_S  | 0.65              | 0.69   | 0.78 | 0.84 | 0.79 | 1.27              | 1.38   | 1.43 | 1.45 | 1.67 | 1.03              | 1.14   | 1.30 | 1.32 | 1.39 | ns    |
| DIFF_HSTL_II_18_S | 0.65              | 0.69   | 0.78 | 0.85 | 0.81 | 1.14              | 1.23   | 1.26 | 1.57 | 1.72 | 0.90              | 1.00   | 1.13 | 1.44 | 1.44 | ns    |
| HSTL_I_F          | 0.61              | 0.64   | 0.73 | 0.84 | 0.79 | 1.10              | 1.19   | 1.23 | 1.31 | 1.41 | 0.85              | 0.96   | 1.10 | 1.18 | 1.13 | ns    |
| HSTL_II_F         | 0.61              | 0.64   | 0.73 | 0.84 | 0.78 | 1.05              | 1.18   | 1.28 | 1.31 | 1.42 | 0.80              | 0.95   | 1.15 | 1.18 | 1.14 | ns    |
| HSTL_I_18_F       | 0.64              | 0.67   | 0.76 | 0.85 | 0.79 | 1.05              | 1.18   | 1.28 | 1.36 | 1.44 | 0.80              | 0.95   | 1.15 | 1.22 | 1.16 | ns    |
| HSTL_II_18_F      | 0.64              | 0.67   | 0.76 | 0.85 | 0.79 | 1.03              | 1.14   | 1.23 | 1.32 | 1.42 | 0.78              | 0.90   | 1.10 | 1.19 | 1.14 | ns    |
| DIFF_HSTL_I_F     | 0.63              | 0.67   | 0.77 | 0.84 | 0.78 | 1.09              | 1.18   | 1.22 | 1.31 | 1.48 | 0.84              | 0.95   | 1.09 | 1.18 | 1.20 | ns    |
| DIFF_HSTL_II_F    | 0.63              | 0.67   | 0.77 | 0.84 | 0.79 | 1.02              | 1.11   | 1.14 | 1.31 | 1.48 | 0.77              | 0.88   | 1.01 | 1.18 | 1.20 | ns    |
| DIFF_HSTL_I_18_F  | 0.65              | 0.69   | 0.78 | 0.84 | 0.79 | 1.08              | 1.17   | 1.21 | 1.36 | 1.48 | 0.83              | 0.94   | 1.07 | 1.22 | 1.20 | ns    |
| DIFF_HSTL_II_18_F | 0.65              | 0.69   | 0.78 | 0.85 | 0.81 | 1.01              | 1.10   | 1.13 | 1.32 | 1.48 | 0.76              | 0.87   | 1.00 | 1.19 | 1.20 | ns    |
| LVC MOS33_S4      | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 3.77              | 3.90   | 4.00 | 4.00 | 4.13 | 3.52              | 3.67   | 3.86 | 3.86 | 3.85 | ns    |
| LVC MOS33_S8      | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 3.49              | 3.62   | 3.72 | 3.72 | 3.84 | 3.24              | 3.39   | 3.58 | 3.58 | 3.56 | ns    |
| LVC MOS33_S12     | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 3.05              | 3.18   | 3.28 | 3.28 | 3.41 | 2.80              | 2.95   | 3.15 | 3.15 | 3.13 | ns    |
| LVC MOS33_S16     | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 3.06              | 3.43   | 3.88 | 3.88 | 3.72 | 2.81              | 3.20   | 3.75 | 3.75 | 3.44 | ns    |
| LVC MOS33_F4      | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 3.22              | 3.36   | 3.45 | 3.45 | 3.58 | 2.98              | 3.12   | 3.32 | 3.32 | 3.30 | ns    |
| LVC MOS33_F8      | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 2.71              | 2.84   | 2.93 | 2.93 | 3.06 | 2.46              | 2.61   | 2.80 | 2.80 | 2.78 | ns    |
| LVC MOS33_F12     | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 2.57              | 2.85   | 3.15 | 3.15 | 2.88 | 2.33              | 2.61   | 3.02 | 3.02 | 2.60 | ns    |
| LVC MOS33_F16     | 1.31              | 1.40   | 1.60 | 1.60 | 1.54 | 2.44              | 2.69   | 2.96 | 2.96 | 2.88 | 2.19              | 2.45   | 2.82 | 2.82 | 2.60 | ns    |
| LVC MOS25_S4      | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 3.08              | 3.22   | 3.31 | 3.31 | 3.44 | 2.84              | 2.98   | 3.18 | 3.18 | 3.16 | ns    |
| LVC MOS25_S8      | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 2.85              | 2.98   | 3.07 | 3.08 | 3.20 | 2.60              | 2.75   | 2.94 | 2.94 | 2.92 | ns    |
| LVC MOS25_S12     | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 2.44              | 2.57   | 2.67 | 2.67 | 2.80 | 2.19              | 2.34   | 2.54 | 2.54 | 2.52 | ns    |
| LVC MOS25_S16     | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 2.79              | 2.92   | 3.01 | 3.01 | 3.14 | 2.54              | 2.68   | 2.88 | 2.88 | 2.86 | ns    |
| LVC MOS25_F4      | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 2.71              | 2.84   | 2.93 | 2.93 | 3.06 | 2.46              | 2.61   | 2.80 | 2.80 | 2.78 | ns    |
| LVC MOS25_F8      | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 2.14              | 2.28   | 2.37 | 2.37 | 2.50 | 1.90              | 2.04   | 2.24 | 2.24 | 2.22 | ns    |
| LVC MOS25_F12     | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 2.15              | 2.29   | 2.52 | 2.52 | 2.48 | 1.91              | 2.05   | 2.38 | 2.38 | 2.20 | ns    |
| LVC MOS25_F16     | 1.08              | 1.16   | 1.32 | 1.35 | 1.36 | 1.92              | 2.17   | 2.45 | 2.45 | 2.33 | 1.67              | 1.94   | 2.32 | 2.32 | 2.05 | ns    |
| LVC MOS18_S4      | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.55              | 1.68   | 1.78 | 1.78 | 1.91 | 1.30              | 1.45   | 1.65 | 1.65 | 1.63 | ns    |
| LVC MOS18_S8      | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 2.14              | 2.28   | 2.37 | 2.37 | 2.50 | 1.90              | 2.04   | 2.24 | 2.24 | 2.22 | ns    |
| LVC MOS18_S12     | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 2.14              | 2.28   | 2.37 | 2.37 | 2.50 | 1.90              | 2.04   | 2.24 | 2.24 | 2.22 | ns    |
| LVC MOS18_S16     | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.49              | 1.62   | 1.72 | 1.72 | 1.84 | 1.24              | 1.39   | 1.58 | 1.58 | 1.56 | ns    |
| LVC MOS18_S24     | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.74              | 1.92   | 2.08 | 2.22 | 1.92 | 1.50              | 1.69   | 1.95 | 2.08 | 1.64 | ns    |
| LVC MOS18_F4      | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.38              | 1.51   | 1.61 | 1.64 | 1.77 | 1.13              | 1.28   | 1.47 | 1.50 | 1.49 | ns    |
| LVC MOS18_F8      | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.64              | 1.78   | 1.87 | 1.87 | 2.00 | 1.40              | 1.54   | 1.74 | 1.74 | 1.72 | ns    |
| LVC MOS18_F12     | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.64              | 1.78   | 1.87 | 1.87 | 2.00 | 1.40              | 1.54   | 1.74 | 1.74 | 1.72 | ns    |
| LVC MOS18_F16     | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.52              | 1.68   | 1.81 | 1.81 | 1.72 | 1.28              | 1.45   | 1.68 | 1.68 | 1.44 | ns    |
| LVC MOS18_F24     | 0.64              | 0.66   | 0.74 | 0.95 | 0.87 | 1.34              | 1.46   | 1.55 | 2.09 | 1.66 | 1.09              | 1.23   | 1.42 | 1.96 | 1.38 | ns    |

**Table 20: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)**

| I/O Standard     | T <sub>IOP1</sub> |        |      |      |      | T <sub>IOP</sub> |        |      |      |      | T <sub>IOTP</sub> |        |      |      |      | Units |
|------------------|-------------------|--------|------|------|------|------------------|--------|------|------|------|-------------------|--------|------|------|------|-------|
|                  | Speed Grade       |        |      |      |      | Speed Grade      |        |      |      |      | Speed Grade       |        |      |      |      |       |
|                  | 1.0V              |        |      |      | 0.9V | 1.0V             |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V |       |
|                  | -3                | -2/-2L | -1   | -1M  | -2L  | -3               | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  |       |
| LVC MOS15_S4     | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.86             | 2.00   | 2.09 | 2.09 | 2.22 | 1.62              | 1.76   | 1.96 | 1.96 | 1.94 | ns    |
| LVC MOS15_S8     | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 2.05             | 2.18   | 2.28 | 2.28 | 2.41 | 1.80              | 1.95   | 2.14 | 2.15 | 2.13 | ns    |
| LVC MOS15_S12    | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.83             | 2.03   | 2.23 | 2.23 | 1.91 | 1.59              | 1.80   | 2.10 | 2.10 | 1.63 | ns    |
| LVC MOS15_S16    | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.76             | 1.95   | 2.13 | 2.13 | 1.91 | 1.52              | 1.72   | 1.99 | 1.99 | 1.63 | ns    |
| LVC MOS15_F4     | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.63             | 1.76   | 1.86 | 1.86 | 1.98 | 1.38              | 1.53   | 1.72 | 1.72 | 1.70 | ns    |
| LVC MOS15_F8     | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.79             | 1.99   | 2.18 | 2.18 | 1.92 | 1.55              | 1.76   | 2.05 | 2.05 | 1.64 | ns    |
| LVC MOS15_F12    | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.40             | 1.54   | 1.65 | 1.65 | 1.67 | 1.15              | 1.31   | 1.52 | 1.52 | 1.39 | ns    |
| LVC MOS15_F16    | 0.66              | 0.69   | 0.81 | 0.93 | 0.90 | 1.37             | 1.51   | 1.61 | 1.89 | 1.66 | 1.13              | 1.27   | 1.48 | 1.75 | 1.38 | ns    |
| LVC MOS12_S4     | 0.88              | 0.91   | 1.00 | 1.17 | 1.01 | 2.53             | 2.67   | 2.76 | 2.76 | 2.89 | 2.29              | 2.43   | 2.63 | 2.63 | 2.61 | ns    |
| LVC MOS12_S8     | 0.88              | 0.91   | 1.00 | 1.17 | 1.01 | 2.05             | 2.18   | 2.28 | 2.28 | 2.41 | 1.80              | 1.95   | 2.14 | 2.15 | 2.13 | ns    |
| LVC MOS12_S12    | 0.88              | 0.91   | 1.00 | 1.17 | 1.01 | 1.75             | 1.89   | 1.98 | 1.98 | 2.11 | 1.51              | 1.65   | 1.85 | 1.85 | 1.83 | ns    |
| LVC MOS12_F4     | 0.88              | 0.91   | 1.00 | 1.17 | 1.01 | 1.94             | 2.07   | 2.17 | 2.17 | 2.30 | 1.69              | 1.84   | 2.04 | 2.04 | 2.02 | ns    |
| LVC MOS12_F8     | 0.88              | 0.91   | 1.00 | 1.17 | 1.01 | 1.50             | 1.64   | 1.73 | 1.73 | 1.86 | 1.26              | 1.40   | 1.60 | 1.60 | 1.58 | ns    |
| LVC MOS12_F12    | 0.88              | 0.91   | 1.00 | 1.17 | 1.01 | 1.54             | 1.71   | 1.87 | 1.87 | 1.69 | 1.29              | 1.48   | 1.74 | 1.74 | 1.41 | ns    |
| SSTL135_S        | 0.61              | 0.64   | 0.73 | 0.85 | 0.79 | 1.27             | 1.40   | 1.50 | 1.53 | 1.64 | 1.02              | 1.17   | 1.36 | 1.40 | 1.36 | ns    |
| SSTL15_S         | 0.61              | 0.64   | 0.73 | 0.73 | 0.73 | 1.24             | 1.37   | 1.47 | 1.53 | 1.59 | 0.99              | 1.14   | 1.33 | 1.40 | 1.31 | ns    |
| SSTL18_I_S       | 0.64              | 0.67   | 0.76 | 0.84 | 0.79 | 1.59             | 1.74   | 1.85 | 1.85 | 1.95 | 1.34              | 1.50   | 1.72 | 1.72 | 1.67 | ns    |
| SSTL18_II_S      | 0.64              | 0.67   | 0.76 | 0.85 | 0.78 | 1.27             | 1.40   | 1.50 | 1.50 | 1.63 | 1.02              | 1.17   | 1.36 | 1.36 | 1.35 | ns    |
| DIFF_SSTL135_S   | 0.59              | 0.61   | 0.73 | 0.85 | 0.79 | 1.27             | 1.40   | 1.50 | 1.53 | 1.64 | 1.02              | 1.17   | 1.36 | 1.40 | 1.36 | ns    |
| DIFF_SSTL15_S    | 0.63              | 0.67   | 0.77 | 0.85 | 0.79 | 1.24             | 1.37   | 1.47 | 1.53 | 1.59 | 0.99              | 1.14   | 1.33 | 1.40 | 1.31 | ns    |
| DIFF_SSTL18_I_S  | 0.65              | 0.69   | 0.78 | 0.85 | 0.79 | 1.50             | 1.63   | 1.72 | 1.82 | 1.95 | 1.26              | 1.40   | 1.59 | 1.69 | 1.67 | ns    |
| DIFF_SSTL18_II_S | 0.65              | 0.69   | 0.78 | 0.85 | 0.79 | 1.13             | 1.22   | 1.25 | 1.50 | 1.66 | 0.88              | 0.99   | 1.12 | 1.36 | 1.38 | ns    |
| SSTL135_F        | 0.61              | 0.64   | 0.73 | 0.85 | 0.79 | 1.04             | 1.17   | 1.26 | 1.31 | 1.42 | 0.79              | 0.93   | 1.13 | 1.18 | 1.14 | ns    |
| SSTL15_F         | 0.61              | 0.64   | 0.73 | 0.73 | 0.73 | 1.04             | 1.17   | 1.26 | 1.26 | 1.39 | 0.79              | 0.93   | 1.13 | 1.13 | 1.11 | ns    |
| SSTL18_I_F       | 0.64              | 0.67   | 0.76 | 0.84 | 0.79 | 1.12             | 1.22   | 1.26 | 1.34 | 1.44 | 0.88              | 0.99   | 1.13 | 1.21 | 1.16 | ns    |
| SSTL18_II_F      | 0.64              | 0.67   | 0.76 | 0.85 | 0.78 | 1.05             | 1.18   | 1.28 | 1.32 | 1.42 | 0.80              | 0.95   | 1.15 | 1.19 | 1.14 | ns    |
| DIFF_SSTL135_F   | 0.59              | 0.61   | 0.73 | 0.85 | 0.79 | 1.04             | 1.17   | 1.26 | 1.31 | 1.42 | 0.79              | 0.93   | 1.13 | 1.18 | 1.14 | ns    |
| DIFF_SSTL15_F    | 0.63              | 0.67   | 0.77 | 0.85 | 0.79 | 1.04             | 1.17   | 1.26 | 1.26 | 1.39 | 0.79              | 0.93   | 1.13 | 1.13 | 1.11 | ns    |
| DIFF_SSTL18_I_F  | 0.65              | 0.69   | 0.78 | 0.85 | 0.79 | 1.10             | 1.19   | 1.23 | 1.34 | 1.52 | 0.85              | 0.96   | 1.10 | 1.21 | 1.24 | ns    |
| DIFF_SSTL18_II_F | 0.65              | 0.69   | 0.78 | 0.85 | 0.79 | 1.02             | 1.10   | 1.14 | 1.32 | 1.50 | 0.77              | 0.87   | 1.00 | 1.19 | 1.22 | ns    |

**Table 21: 1.8V IOB High Performance (HP) Switching Characteristics**

| I/O Standard            | T <sub>IOPI</sub> |        |      |      |      | T <sub>IOOP</sub> |        |      |      |      | T <sub>IOTP</sub> |        |      |      |      | Units |
|-------------------------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------|
|                         | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      |       |
|                         | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V |       |
|                         | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  |       |
| LVDS                    | 0.75              | 0.79   | 0.92 | 0.96 | 0.89 | 1.05              | 1.17   | 1.24 | 1.26 | 1.43 | 0.88              | 1.01   | 1.08 | 1.10 | 1.32 | ns    |
| HSUL_12_S               | 0.69              | 0.72   | 0.82 | 0.98 | 0.95 | 1.65              | 1.84   | 2.05 | 2.05 | 1.80 | 1.48              | 1.68   | 1.89 | 1.89 | 1.70 | ns    |
| HSUL_12_F               | 0.69              | 0.72   | 0.82 | 0.98 | 0.95 | 1.39              | 1.54   | 1.68 | 1.68 | 1.49 | 1.22              | 1.38   | 1.52 | 1.52 | 1.39 | ns    |
| DIFF_HSUL_12_S          | 0.69              | 0.72   | 0.82 | 0.98 | 0.92 | 1.65              | 1.84   | 2.05 | 2.05 | 1.47 | 1.48              | 1.68   | 1.89 | 1.89 | 1.37 | ns    |
| DIFF_HSUL_12_F          | 0.69              | 0.72   | 0.82 | 0.98 | 0.92 | 1.39              | 1.54   | 1.68 | 1.68 | 1.35 | 1.22              | 1.38   | 1.52 | 1.52 | 1.24 | ns    |
| DIFF_HSUL_12_DCI_S      | 0.69              | 0.72   | 0.82 | 0.82 | 0.92 | 1.78              | 1.91   | 2.05 | 2.05 | 1.46 | 1.61              | 1.76   | 1.89 | 1.89 | 1.35 | ns    |
| DIFF_HSUL_12_DCI_F      | 0.69              | 0.72   | 0.82 | 0.82 | 0.92 | 1.56              | 1.67   | 1.76 | 1.76 | 1.35 | 1.39              | 1.51   | 1.60 | 1.60 | 1.24 | ns    |
| HSTL_I_S                | 0.68              | 0.72   | 0.82 | 0.90 | 0.84 | 1.15              | 1.28   | 1.38 | 1.38 | 1.46 | 0.98              | 1.12   | 1.22 | 1.22 | 1.35 | ns    |
| HSTL_II_S               | 0.68              | 0.72   | 0.82 | 0.90 | 0.84 | 1.05              | 1.17   | 1.26 | 1.27 | 1.44 | 0.88              | 1.01   | 1.10 | 1.11 | 1.34 | ns    |
| HSTL_I_18_S             | 0.70              | 0.72   | 0.82 | 0.95 | 0.86 | 1.12              | 1.24   | 1.34 | 1.34 | 1.41 | 0.95              | 1.08   | 1.18 | 1.18 | 1.31 | ns    |
| HSTL_II_18_S            | 0.70              | 0.72   | 0.82 | 0.90 | 0.86 | 1.06              | 1.18   | 1.26 | 1.27 | 1.44 | 0.89              | 1.02   | 1.10 | 1.11 | 1.34 | ns    |
| HSTL_I_12_S             | 0.68              | 0.72   | 0.82 | 0.96 | 0.94 | 1.14              | 1.27   | 1.37 | 1.37 | 1.43 | 0.97              | 1.11   | 1.21 | 1.21 | 1.32 | ns    |
| HSTL_I_DCI_S            | 0.68              | 0.72   | 0.82 | 0.90 | 0.78 | 1.11              | 1.23   | 1.33 | 1.33 | 1.36 | 0.94              | 1.07   | 1.17 | 1.17 | 1.26 | ns    |
| HSTL_II_DCI_S           | 0.68              | 0.72   | 0.82 | 0.85 | 0.78 | 1.05              | 1.17   | 1.26 | 1.26 | 1.33 | 0.88              | 1.01   | 1.10 | 1.10 | 1.23 | ns    |
| HSTL_II_T_DCI_S         | 0.70              | 0.72   | 0.82 | 0.82 | 0.76 | 1.15              | 1.28   | 1.38 | 1.38 | 1.40 | 0.98              | 1.12   | 1.22 | 1.22 | 1.29 | ns    |
| HSTL_I_DCI_18_S         | 0.70              | 0.72   | 0.82 | 0.90 | 0.76 | 1.11              | 1.23   | 1.33 | 1.33 | 1.36 | 0.94              | 1.07   | 1.17 | 1.17 | 1.26 | ns    |
| HSTL_II_DCI_18_S        | 0.70              | 0.72   | 0.82 | 0.82 | 0.76 | 1.05              | 1.16   | 1.24 | 1.24 | 1.32 | 0.88              | 1.00   | 1.08 | 1.08 | 1.21 | ns    |
| HSTL_II_T_DCI_18_S      | 0.70              | 0.72   | 0.82 | 0.84 | 0.76 | 1.11              | 1.23   | 1.33 | 1.34 | 1.36 | 0.94              | 1.07   | 1.17 | 1.18 | 1.26 | ns    |
| DIFF_HSTL_I_S           | 0.75              | 0.79   | 0.92 | 1.02 | 0.89 | 1.15              | 1.28   | 1.38 | 1.38 | 1.47 | 0.98              | 1.12   | 1.22 | 1.22 | 1.37 | ns    |
| DIFF_HSTL_II_S          | 0.75              | 0.79   | 0.92 | 1.02 | 0.89 | 1.05              | 1.17   | 1.26 | 1.32 | 1.47 | 0.88              | 1.01   | 1.10 | 1.16 | 1.37 | ns    |
| DIFF_HSTL_I_DCI_S       | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 1.15              | 1.28   | 1.38 | 1.38 | 1.47 | 0.98              | 1.12   | 1.22 | 1.22 | 1.37 | ns    |
| DIFF_HSTL_II_DCI_S      | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 1.05              | 1.17   | 1.26 | 1.26 | 1.40 | 0.88              | 1.01   | 1.10 | 1.10 | 1.29 | ns    |
| DIFF_HSTL_I_18_S        | 0.75              | 0.79   | 0.92 | 0.98 | 0.89 | 1.12              | 1.24   | 1.34 | 1.34 | 1.46 | 0.95              | 1.08   | 1.18 | 1.18 | 1.35 | ns    |
| DIFF_HSTL_II_18_S       | 0.75              | 0.79   | 0.92 | 0.99 | 0.89 | 1.06              | 1.18   | 1.26 | 1.32 | 1.47 | 0.89              | 1.02   | 1.10 | 1.16 | 1.37 | ns    |
| DIFF_HSTL_I_DCI_18_S    | 0.75              | 0.79   | 0.92 | 0.92 | 0.75 | 1.11              | 1.23   | 1.33 | 1.33 | 1.46 | 0.94              | 1.07   | 1.17 | 1.17 | 1.35 | ns    |
| DIFF_HSTL_II_DCI_18_S   | 0.75              | 0.79   | 0.92 | 0.93 | 0.75 | 1.05              | 1.16   | 1.24 | 1.26 | 1.41 | 0.88              | 1.00   | 1.08 | 1.10 | 1.31 | ns    |
| DIFF_HSTL_II_T_DCI_18_S | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 1.11              | 1.23   | 1.33 | 1.33 | 1.46 | 0.94              | 1.07   | 1.17 | 1.17 | 1.35 | ns    |
| HSTL_I_F                | 0.68              | 0.72   | 0.82 | 0.90 | 0.84 | 1.02              | 1.14   | 1.22 | 1.22 | 1.26 | 0.85              | 0.98   | 1.06 | 1.06 | 1.15 | ns    |
| HSTL_II_F               | 0.68              | 0.72   | 0.82 | 0.90 | 0.84 | 0.97              | 1.08   | 1.15 | 1.15 | 1.29 | 0.80              | 0.92   | 0.99 | 0.99 | 1.18 | ns    |
| HSTL_I_18_F             | 0.70              | 0.72   | 0.82 | 0.95 | 0.86 | 1.04              | 1.16   | 1.24 | 1.24 | 1.32 | 0.87              | 1.00   | 1.08 | 1.08 | 1.21 | ns    |
| HSTL_II_18_F            | 0.70              | 0.72   | 0.82 | 0.90 | 0.86 | 0.98              | 1.09   | 1.16 | 1.20 | 1.35 | 0.81              | 0.94   | 1.00 | 1.03 | 1.24 | ns    |
| HSTL_I_12_F             | 0.68              | 0.72   | 0.82 | 0.96 | 0.94 | 1.02              | 1.13   | 1.21 | 1.21 | 1.26 | 0.85              | 0.97   | 1.05 | 1.05 | 1.15 | ns    |
| HSTL_I_DCI_F            | 0.68              | 0.72   | 0.82 | 0.90 | 0.78 | 1.04              | 1.16   | 1.24 | 1.24 | 1.30 | 0.87              | 1.00   | 1.08 | 1.08 | 1.20 | ns    |
| HSTL_II_DCI_F           | 0.68              | 0.72   | 0.82 | 0.85 | 0.78 | 0.97              | 1.08   | 1.15 | 1.15 | 1.22 | 0.80              | 0.92   | 0.99 | 0.99 | 1.12 | ns    |
| HSTL_II_T_DCI_F         | 0.70              | 0.72   | 0.82 | 0.82 | 0.76 | 1.02              | 1.14   | 1.22 | 1.22 | 1.26 | 0.85              | 0.98   | 1.06 | 1.06 | 1.15 | ns    |
| HSTL_I_DCI_18_F         | 0.70              | 0.72   | 0.82 | 0.90 | 0.76 | 1.04              | 1.16   | 1.24 | 1.24 | 1.30 | 0.87              | 1.00   | 1.08 | 1.08 | 1.20 | ns    |
| HSTL_II_DCI_18_F        | 0.70              | 0.72   | 0.82 | 0.82 | 0.76 | 0.98              | 1.09   | 1.16 | 1.16 | 1.27 | 0.81              | 0.93   | 1.00 | 1.00 | 1.17 | ns    |

Table 21: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standard            | T <sub>IOPI</sub> |        |      |      |      | T <sub>IOOP</sub> |        |      |      |      | T <sub>IOTP</sub> |        |      |      |      | Units |
|-------------------------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------|
|                         | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      |       |
|                         | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V |       |
|                         | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  |       |
| HSTL_II_T_DCI_18_F      | 0.70              | 0.72   | 0.82 | 0.84 | 0.76 | 1.04              | 1.16   | 1.24 | 1.24 | 1.30 | 0.87              | 1.00   | 1.08 | 1.08 | 1.20 | ns    |
| DIFF_HSTL_I_F           | 0.75              | 0.79   | 0.92 | 1.02 | 0.89 | 1.02              | 1.14   | 1.22 | 1.22 | 1.35 | 0.85              | 0.98   | 1.06 | 1.06 | 1.24 | ns    |
| DIFF_HSTL_II_F          | 0.75              | 0.79   | 0.92 | 1.02 | 0.89 | 0.97              | 1.08   | 1.15 | 1.20 | 1.35 | 0.80              | 0.92   | 0.99 | 1.03 | 1.24 | ns    |
| DIFF_HSTL_I_DCI_F       | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 1.02              | 1.14   | 1.22 | 1.22 | 1.35 | 0.85              | 0.98   | 1.06 | 1.06 | 1.24 | ns    |
| DIFF_HSTL_II_DCI_F      | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 0.97              | 1.08   | 1.15 | 1.15 | 1.30 | 0.80              | 0.92   | 0.99 | 0.99 | 1.20 | ns    |
| DIFF_HSTL_I_18_F        | 0.75              | 0.79   | 0.92 | 0.98 | 0.89 | 1.04              | 1.16   | 1.24 | 1.24 | 1.38 | 0.87              | 1.00   | 1.08 | 1.08 | 1.28 | ns    |
| DIFF_HSTL_II_18_F       | 0.75              | 0.79   | 0.92 | 0.99 | 0.89 | 0.98              | 1.09   | 1.16 | 1.24 | 1.40 | 0.81              | 0.94   | 1.00 | 1.08 | 1.29 | ns    |
| DIFF_HSTL_I_DCI_18_F    | 0.75              | 0.79   | 0.92 | 0.92 | 0.75 | 1.04              | 1.16   | 1.24 | 1.24 | 1.38 | 0.87              | 1.00   | 1.08 | 1.08 | 1.28 | ns    |
| DIFF_HSTL_II_DCI_18_F   | 0.75              | 0.79   | 0.92 | 0.93 | 0.75 | 0.98              | 1.09   | 1.16 | 1.18 | 1.33 | 0.81              | 0.93   | 1.00 | 1.02 | 1.23 | ns    |
| DIFF_HSTL_II_T_DCI_18_F | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 1.04              | 1.16   | 1.24 | 1.24 | 1.38 | 0.87              | 1.00   | 1.08 | 1.08 | 1.28 | ns    |
| LVC MOS18_S2            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 3.95              | 4.28   | 4.85 | 4.85 | 3.40 | 3.78              | 4.13   | 4.69 | 4.69 | 3.29 | ns    |
| LVC MOS18_S4            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 2.67              | 2.98   | 3.43 | 3.43 | 2.69 | 2.50              | 2.82   | 3.27 | 3.27 | 2.59 | ns    |
| LVC MOS18_S6            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 2.14              | 2.38   | 2.72 | 2.72 | 2.18 | 1.97              | 2.22   | 2.56 | 2.56 | 2.07 | ns    |
| LVC MOS18_S8            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.98              | 2.21   | 2.52 | 2.52 | 2.02 | 1.81              | 2.05   | 2.36 | 2.36 | 1.92 | ns    |
| LVC MOS18_S12           | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.70              | 1.91   | 2.17 | 2.17 | 1.85 | 1.53              | 1.75   | 2.01 | 2.01 | 1.74 | ns    |
| LVC MOS18_S16           | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.57              | 1.75   | 1.97 | 1.97 | 1.76 | 1.40              | 1.59   | 1.81 | 1.81 | 1.65 | ns    |
| LVC MOS18_F2            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 3.50              | 3.87   | 4.48 | 4.48 | 2.85 | 3.33              | 3.71   | 4.32 | 4.32 | 2.74 | ns    |
| LVC MOS18_F4            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 2.23              | 2.50   | 2.87 | 2.87 | 2.26 | 2.06              | 2.34   | 2.71 | 2.71 | 2.15 | ns    |
| LVC MOS18_F6            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.80              | 2.00   | 2.26 | 2.26 | 1.52 | 1.63              | 1.84   | 2.09 | 2.09 | 1.42 | ns    |
| LVC MOS18_F8            | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.46              | 1.72   | 2.04 | 2.04 | 1.51 | 1.29              | 1.56   | 1.88 | 1.88 | 1.40 | ns    |
| LVC MOS18_F12           | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.26              | 1.40   | 1.53 | 1.53 | 1.46 | 1.09              | 1.24   | 1.37 | 1.37 | 1.35 | ns    |
| LVC MOS18_F16           | 0.47              | 0.50   | 0.60 | 0.90 | 0.87 | 1.19              | 1.33   | 1.44 | 1.66 | 1.46 | 1.02              | 1.17   | 1.28 | 1.50 | 1.35 | ns    |
| LVC MOS15_S2            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 3.55              | 3.89   | 4.45 | 4.45 | 3.11 | 3.38              | 3.73   | 4.29 | 4.29 | 3.01 | ns    |
| LVC MOS15_S4            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 2.45              | 2.70   | 3.06 | 3.06 | 2.46 | 2.28              | 2.54   | 2.90 | 2.90 | 2.35 | ns    |
| LVC MOS15_S6            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 2.24              | 2.51   | 2.88 | 2.88 | 2.33 | 2.07              | 2.35   | 2.72 | 2.72 | 2.23 | ns    |
| LVC MOS15_S8            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.91              | 2.16   | 2.49 | 2.49 | 2.05 | 1.74              | 2.00   | 2.32 | 2.32 | 1.95 | ns    |
| LVC MOS15_S12           | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.77              | 1.98   | 2.23 | 2.23 | 1.97 | 1.60              | 1.82   | 2.07 | 2.07 | 1.87 | ns    |
| LVC MOS15_S16           | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.62              | 1.81   | 2.02 | 2.02 | 1.85 | 1.45              | 1.65   | 1.86 | 1.86 | 1.74 | ns    |
| LVC MOS15_F2            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 3.38              | 3.69   | 4.18 | 4.18 | 2.74 | 3.21              | 3.53   | 4.02 | 4.02 | 2.64 | ns    |
| LVC MOS15_F4            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 2.04              | 2.21   | 2.44 | 2.44 | 1.72 | 1.87              | 2.06   | 2.27 | 2.27 | 1.62 | ns    |
| LVC MOS15_F6            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.47              | 1.74   | 2.09 | 2.09 | 1.49 | 1.30              | 1.58   | 1.93 | 1.93 | 1.39 | ns    |
| LVC MOS15_F8            | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.31              | 1.46   | 1.61 | 1.61 | 1.47 | 1.14              | 1.30   | 1.45 | 1.45 | 1.37 | ns    |
| LVC MOS15_F12           | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.21              | 1.34   | 1.45 | 1.45 | 1.44 | 1.04              | 1.18   | 1.29 | 1.29 | 1.34 | ns    |
| LVC MOS15_F16           | 0.59              | 0.62   | 0.73 | 0.88 | 0.86 | 1.18              | 1.31   | 1.41 | 1.68 | 1.41 | 1.01              | 1.15   | 1.25 | 1.52 | 1.31 | ns    |
| LVC MOS12_S2            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 3.38              | 3.80   | 4.48 | 4.48 | 3.27 | 3.21              | 3.64   | 4.31 | 4.31 | 3.17 | ns    |
| LVC MOS12_S4            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 2.62              | 2.94   | 3.43 | 3.43 | 2.76 | 2.45              | 2.78   | 3.27 | 3.27 | 2.65 | ns    |
| LVC MOS12_S6            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 2.05              | 2.33   | 2.72 | 2.72 | 2.24 | 1.88              | 2.17   | 2.56 | 2.56 | 2.14 | ns    |

**Table 21: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)**

| I/O Standard           | T <sub>IOPI</sub> |        |      |      |      | T <sub>IOOP</sub> |        |      |      |      | T <sub>IOTP</sub> |        |      |      |      | Units |
|------------------------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------|
|                        | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      |       |
|                        | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V |       |
|                        | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  |       |
| LVCN0512_S8            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 1.94              | 2.18   | 2.51 | 2.51 | 2.16 | 1.77              | 2.02   | 2.34 | 2.34 | 2.06 | ns    |
| LVCN0512_F2            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 2.84              | 3.15   | 3.62 | 3.62 | 2.47 | 2.67              | 2.99   | 3.46 | 3.46 | 2.37 | ns    |
| LVCN0512_F4            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 1.97              | 2.18   | 2.44 | 2.44 | 1.69 | 1.80              | 2.02   | 2.28 | 2.28 | 1.59 | ns    |
| LVCN0512_F6            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 1.33              | 1.51   | 1.70 | 1.70 | 1.43 | 1.16              | 1.35   | 1.54 | 1.54 | 1.32 | ns    |
| LVCN0512_F8            | 0.64              | 0.67   | 0.78 | 1.04 | 0.95 | 1.27              | 1.42   | 1.55 | 1.55 | 1.41 | 1.10              | 1.26   | 1.39 | 1.39 | 1.31 | ns    |
| LVDCI_18               | 0.47              | 0.50   | 0.60 | 0.87 | 0.86 | 1.99              | 2.15   | 2.35 | 2.35 | 2.44 | 1.82              | 1.99   | 2.19 | 2.19 | 2.34 | ns    |
| LVDCI_15               | 0.59              | 0.62   | 0.73 | 0.92 | 0.87 | 1.98              | 2.23   | 2.58 | 2.58 | 2.40 | 1.81              | 2.07   | 2.41 | 2.41 | 2.29 | ns    |
| LVDCI_DV2_18           | 0.47              | 0.50   | 0.60 | 0.88 | 0.87 | 1.99              | 2.15   | 2.34 | 2.34 | 1.86 | 1.82              | 1.99   | 2.18 | 2.18 | 1.76 | ns    |
| LVDCI_DV2_15           | 0.59              | 0.62   | 0.73 | 0.88 | 0.87 | 1.98              | 2.23   | 2.58 | 2.58 | 1.83 | 1.81              | 2.07   | 2.41 | 2.41 | 1.73 | ns    |
| HSLVDCI_18             | 0.68              | 0.72   | 0.82 | 0.90 | 0.86 | 1.99              | 2.15   | 2.35 | 2.35 | 2.43 | 1.82              | 1.99   | 2.19 | 2.19 | 2.32 | ns    |
| HSLVDCI_15             | 0.68              | 0.72   | 0.82 | 0.93 | 0.84 | 1.98              | 2.23   | 2.58 | 2.58 | 2.27 | 1.81              | 2.07   | 2.41 | 2.41 | 2.17 | ns    |
| SSTL18_I_S             | 0.68              | 0.72   | 0.82 | 0.95 | 0.86 | 1.02              | 1.15   | 1.24 | 1.24 | 1.41 | 0.85              | 0.99   | 1.08 | 1.08 | 1.31 | ns    |
| SSTL18_IL_S            | 0.68              | 0.72   | 0.82 | 1.01 | 0.87 | 1.17              | 1.29   | 1.37 | 1.38 | 1.55 | 1.00              | 1.13   | 1.21 | 1.22 | 1.45 | ns    |
| SSTL18_I_DCI_S         | 0.68              | 0.72   | 0.82 | 0.87 | 0.76 | 0.92              | 1.06   | 1.17 | 1.18 | 1.32 | 0.75              | 0.90   | 1.01 | 1.02 | 1.21 | ns    |
| SSTL18_IL_DCI_S        | 0.68              | 0.72   | 0.82 | 0.82 | 0.78 | 0.88              | 0.98   | 1.08 | 1.12 | 1.26 | 0.71              | 0.83   | 0.92 | 0.96 | 1.15 | ns    |
| SSTL18_IL_T_DCI_S      | 0.68              | 0.72   | 0.82 | 0.98 | 0.78 | 0.92              | 1.06   | 1.17 | 1.18 | 1.32 | 0.75              | 0.90   | 1.01 | 1.02 | 1.21 | ns    |
| SSTL15_S               | 0.68              | 0.72   | 0.82 | 0.82 | 0.81 | 0.94              | 1.06   | 1.15 | 1.16 | 1.32 | 0.77              | 0.91   | 0.99 | 1.00 | 1.21 | ns    |
| SSTL15_DCI_S           | 0.68              | 0.72   | 0.82 | 0.90 | 0.78 | 0.94              | 1.06   | 1.15 | 1.16 | 1.30 | 0.77              | 0.90   | 0.99 | 1.00 | 1.20 | ns    |
| SSTL15_T_DCI_S         | 0.68              | 0.72   | 0.82 | 0.87 | 0.80 | 0.94              | 1.06   | 1.15 | 1.15 | 1.30 | 0.77              | 0.90   | 0.99 | 0.99 | 1.20 | ns    |
| SSTL135_S              | 0.69              | 0.72   | 0.82 | 0.93 | 0.89 | 0.97              | 1.10   | 1.19 | 1.20 | 1.35 | 0.80              | 0.94   | 1.03 | 1.03 | 1.24 | ns    |
| SSTL135_DCI_S          | 0.69              | 0.72   | 0.82 | 0.85 | 0.84 | 0.97              | 1.09   | 1.19 | 1.20 | 1.33 | 0.80              | 0.93   | 1.03 | 1.03 | 1.23 | ns    |
| SSTL135_T_DCI_S        | 0.69              | 0.72   | 0.82 | 0.93 | 0.84 | 0.97              | 1.09   | 1.19 | 1.20 | 1.33 | 0.80              | 0.93   | 1.03 | 1.03 | 1.23 | ns    |
| SSTL12_S               | 0.69              | 0.72   | 0.82 | 1.02 | 0.95 | 0.96              | 1.09   | 1.18 | 1.18 | 1.33 | 0.79              | 0.93   | 1.02 | 1.02 | 1.23 | ns    |
| SSTL12_DCI_S           | 0.69              | 0.72   | 0.82 | 0.90 | 0.91 | 1.03              | 1.17   | 1.27 | 1.27 | 1.33 | 0.86              | 1.01   | 1.11 | 1.11 | 1.23 | ns    |
| SSTL12_T_DCI_S         | 0.69              | 0.72   | 0.82 | 0.88 | 0.91 | 1.03              | 1.17   | 1.27 | 1.27 | 1.33 | 0.86              | 1.01   | 1.11 | 1.11 | 1.23 | ns    |
| DIFF_SSTL18_I_S        | 0.75              | 0.79   | 0.92 | 0.99 | 0.89 | 1.02              | 1.15   | 1.24 | 1.29 | 1.43 | 0.85              | 0.99   | 1.08 | 1.13 | 1.32 | ns    |
| DIFF_SSTL18_IL_S       | 0.75              | 0.79   | 0.92 | 0.93 | 0.89 | 1.17              | 1.29   | 1.37 | 1.40 | 1.55 | 1.00              | 1.13   | 1.21 | 1.24 | 1.45 | ns    |
| DIFF_SSTL18_I_DCI_S    | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 0.92              | 1.06   | 1.17 | 1.24 | 1.40 | 0.75              | 0.90   | 1.01 | 1.08 | 1.29 | ns    |
| DIFF_SSTL18_IL_DCI_S   | 0.75              | 0.79   | 0.92 | 0.96 | 0.75 | 0.88              | 0.98   | 1.08 | 1.18 | 1.33 | 0.71              | 0.83   | 0.92 | 1.02 | 1.23 | ns    |
| DIFF_SSTL18_IL_T_DCI_S | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 0.92              | 1.06   | 1.17 | 1.24 | 1.40 | 0.75              | 0.90   | 1.01 | 1.08 | 1.29 | ns    |
| DIFF_SSTL15_S          | 0.68              | 0.72   | 0.82 | 0.99 | 0.89 | 0.94              | 1.06   | 1.15 | 1.16 | 1.32 | 0.77              | 0.91   | 0.99 | 1.00 | 1.21 | ns    |
| DIFF_SSTL15_DCI_S      | 0.68              | 0.72   | 0.82 | 0.96 | 0.75 | 0.94              | 1.06   | 1.15 | 1.16 | 1.30 | 0.77              | 0.90   | 0.99 | 1.00 | 1.20 | ns    |
| DIFF_SSTL15_T_DCI_S    | 0.68              | 0.72   | 0.82 | 0.88 | 0.76 | 0.94              | 1.06   | 1.15 | 1.23 | 1.38 | 0.77              | 0.90   | 0.99 | 1.07 | 1.28 | ns    |
| DIFF_SSTL135_S         | 0.69              | 0.72   | 0.82 | 1.09 | 0.91 | 0.97              | 1.10   | 1.19 | 1.20 | 1.35 | 0.80              | 0.94   | 1.03 | 1.03 | 1.24 | ns    |
| DIFF_SSTL135_DCI_S     | 0.69              | 0.72   | 0.82 | 0.90 | 0.76 | 0.97              | 1.09   | 1.19 | 1.20 | 1.33 | 0.80              | 0.93   | 1.03 | 1.03 | 1.23 | ns    |
| DIFF_SSTL135_T_DCI_S   | 0.69              | 0.72   | 0.82 | 0.84 | 0.76 | 0.97              | 1.09   | 1.19 | 1.27 | 1.43 | 0.80              | 0.93   | 1.03 | 1.11 | 1.32 | ns    |
| DIFF_SSTL12_S          | 0.69              | 0.72   | 0.82 | 0.96 | 0.91 | 0.96              | 1.09   | 1.18 | 1.18 | 1.33 | 0.79              | 0.93   | 1.02 | 1.02 | 1.23 | ns    |

**Table 21: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)**

| I/O Standard           | T <sub>IOPI</sub> |        |      |      |      | T <sub>IOOP</sub> |        |      |      |      | T <sub>IOTP</sub> |        |      |      |      | Units |
|------------------------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------------------|--------|------|------|------|-------|
|                        | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      | Speed Grade       |        |      |      |      |       |
|                        | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V | 1.0V              |        |      |      | 0.9V |       |
|                        | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  | -3                | -2/-2L | -1   | -1M  | -2L  |       |
| DIFF_SSTL12_DCI_S      | 0.69              | 0.72   | 0.82 | 0.87 | 0.78 | 1.03              | 1.17   | 1.27 | 1.27 | 1.33 | 0.86              | 1.01   | 1.11 | 1.11 | 1.23 | ns    |
| DIFF_SSTL12_T_DCI_S    | 0.69              | 0.72   | 0.82 | 0.96 | 0.80 | 1.03              | 1.17   | 1.27 | 1.27 | 1.41 | 0.86              | 1.01   | 1.11 | 1.11 | 1.31 | ns    |
| SSTL18_I_F             | 0.68              | 0.72   | 0.82 | 0.95 | 0.86 | 0.94              | 1.06   | 1.15 | 1.15 | 1.32 | 0.77              | 0.91   | 0.99 | 0.99 | 1.21 | ns    |
| SSTL18_IL_F            | 0.68              | 0.72   | 0.82 | 1.01 | 0.87 | 0.97              | 1.09   | 1.16 | 1.21 | 1.36 | 0.80              | 0.93   | 1.00 | 1.05 | 1.26 | ns    |
| SSTL18_I_DCI_F         | 0.68              | 0.72   | 0.82 | 0.87 | 0.76 | 0.89              | 1.02   | 1.10 | 1.15 | 1.30 | 0.72              | 0.86   | 0.94 | 0.99 | 1.20 | ns    |
| SSTL18_IL_DCI_F        | 0.68              | 0.72   | 0.82 | 0.82 | 0.78 | 0.89              | 1.02   | 1.10 | 1.10 | 1.24 | 0.72              | 0.86   | 0.94 | 0.94 | 1.14 | ns    |
| SSTL18_IL_T_DCI_F      | 0.68              | 0.72   | 0.82 | 0.98 | 0.78 | 0.89              | 1.02   | 1.10 | 1.15 | 1.27 | 0.72              | 0.86   | 0.94 | 0.99 | 1.17 | ns    |
| SSTL15_F               | 0.68              | 0.72   | 0.82 | 0.82 | 0.81 | 0.89              | 1.01   | 1.09 | 1.09 | 1.24 | 0.72              | 0.85   | 0.93 | 0.93 | 1.14 | ns    |
| SSTL15_DCI_F           | 0.68              | 0.72   | 0.82 | 0.90 | 0.78 | 0.89              | 1.01   | 1.09 | 1.12 | 1.27 | 0.72              | 0.85   | 0.93 | 0.96 | 1.17 | ns    |
| SSTL15_T_DCI_F         | 0.68              | 0.72   | 0.82 | 0.87 | 0.80 | 0.89              | 1.01   | 1.09 | 1.12 | 1.27 | 0.72              | 0.85   | 0.93 | 0.96 | 1.17 | ns    |
| SSTL135_F              | 0.69              | 0.72   | 0.82 | 0.93 | 0.89 | 0.88              | 1.00   | 1.08 | 1.12 | 1.27 | 0.71              | 0.85   | 0.92 | 0.96 | 1.17 | ns    |
| SSTL135_DCI_F          | 0.69              | 0.72   | 0.82 | 0.85 | 0.84 | 0.89              | 1.00   | 1.08 | 1.12 | 1.27 | 0.72              | 0.85   | 0.92 | 0.96 | 1.17 | ns    |
| SSTL135_T_DCI_F        | 0.69              | 0.72   | 0.82 | 0.93 | 0.84 | 0.89              | 1.00   | 1.08 | 1.12 | 1.27 | 0.72              | 0.85   | 0.92 | 0.96 | 1.17 | ns    |
| SSTL12_F               | 0.69              | 0.72   | 0.82 | 1.02 | 0.95 | 0.88              | 1.00   | 1.08 | 1.12 | 1.26 | 0.71              | 0.84   | 0.92 | 0.96 | 1.15 | ns    |
| SSTL12_DCI_F           | 0.69              | 0.72   | 0.82 | 0.90 | 0.91 | 0.91              | 1.03   | 1.11 | 1.11 | 1.24 | 0.74              | 0.88   | 0.95 | 0.95 | 1.14 | ns    |
| SSTL12_T_DCI_F         | 0.69              | 0.72   | 0.82 | 0.88 | 0.91 | 0.91              | 1.03   | 1.11 | 1.12 | 1.26 | 0.74              | 0.88   | 0.95 | 0.96 | 1.15 | ns    |
| DIFF_SSTL18_I_F        | 0.75              | 0.79   | 0.92 | 0.99 | 0.89 | 0.94              | 1.06   | 1.15 | 1.23 | 1.38 | 0.77              | 0.91   | 0.99 | 1.07 | 1.28 | ns    |
| DIFF_SSTL18_IL_F       | 0.75              | 0.79   | 0.92 | 0.93 | 0.89 | 0.97              | 1.09   | 1.16 | 1.24 | 1.40 | 0.80              | 0.93   | 1.00 | 1.08 | 1.29 | ns    |
| DIFF_SSTL18_I_DCI_F    | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 0.89              | 1.02   | 1.10 | 1.23 | 1.36 | 0.72              | 0.86   | 0.94 | 1.07 | 1.26 | ns    |
| DIFF_SSTL18_IL_DCI_F   | 0.75              | 0.79   | 0.92 | 0.96 | 0.75 | 0.89              | 1.02   | 1.10 | 1.16 | 1.32 | 0.72              | 0.86   | 0.94 | 1.00 | 1.21 | ns    |
| DIFF_SSTL18_IL_T_DCI_F | 0.75              | 0.79   | 0.92 | 0.92 | 0.76 | 0.89              | 1.02   | 1.10 | 1.24 | 1.38 | 0.72              | 0.86   | 0.94 | 1.08 | 1.28 | ns    |
| DIFF_SSTL15_F          | 0.68              | 0.72   | 0.82 | 0.99 | 0.89 | 0.89              | 1.01   | 1.09 | 1.09 | 1.24 | 0.72              | 0.85   | 0.93 | 0.93 | 1.14 | ns    |
| DIFF_SSTL15_DCI_F      | 0.68              | 0.72   | 0.82 | 0.96 | 0.75 | 0.89              | 1.01   | 1.09 | 1.12 | 1.27 | 0.72              | 0.85   | 0.93 | 0.96 | 1.17 | ns    |
| DIFF_SSTL15_T_DCI_F    | 0.68              | 0.72   | 0.82 | 0.88 | 0.76 | 0.89              | 1.01   | 1.09 | 1.20 | 1.35 | 0.72              | 0.85   | 0.93 | 1.03 | 1.24 | ns    |
| DIFF_SSTL135_F         | 0.69              | 0.72   | 0.82 | 1.09 | 0.91 | 0.88              | 1.00   | 1.08 | 1.12 | 1.27 | 0.71              | 0.85   | 0.92 | 0.96 | 1.17 | ns    |
| DIFF_SSTL135_DCI_F     | 0.69              | 0.72   | 0.82 | 0.90 | 0.76 | 0.89              | 1.00   | 1.08 | 1.12 | 1.27 | 0.72              | 0.85   | 0.92 | 0.96 | 1.17 | ns    |
| DIFF_SSTL135_T_DCI_F   | 0.69              | 0.72   | 0.82 | 0.84 | 0.76 | 0.89              | 1.00   | 1.08 | 1.20 | 1.35 | 0.72              | 0.85   | 0.92 | 1.03 | 1.24 | ns    |
| DIFF_SSTL12_F          | 0.69              | 0.72   | 0.82 | 0.96 | 0.91 | 0.88              | 1.00   | 1.08 | 1.12 | 1.26 | 0.71              | 0.84   | 0.92 | 0.96 | 1.15 | ns    |
| DIFF_SSTL12_DCI_F      | 0.69              | 0.72   | 0.82 | 0.87 | 0.78 | 0.91              | 1.03   | 1.11 | 1.11 | 1.24 | 0.74              | 0.88   | 0.95 | 0.95 | 1.14 | ns    |
| DIFF_SSTL12_T_DCI_F    | 0.69              | 0.72   | 0.82 | 0.96 | 0.80 | 0.91              | 1.03   | 1.11 | 1.18 | 1.33 | 0.74              | 0.88   | 0.95 | 1.02 | 1.23 | ns    |

Table 22 specifies the values of  $T_{IOTPHZ}$  and  $T_{IOIBUFDISABLE}$ .  $T_{IOTPHZ}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).  $T_{IOIBUFDISABLE}$  is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than  $T_{IOTPHZ}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN\_TERM termination turn-off time is always faster than  $T_{IOTPHZ}$  when the INTERMDISABLE pin is used.

**Table 22: IOB 3-state Output Switching Characteristics**

| Symbol                  | Description   | Speed Grade |        |      |      |      | Units |
|-------------------------|---|-------------|--------|------|------|------|-------|
|                         |   | 1.0V        |        |      |      | 0.9V |       |
|                         |   | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| $T_{IOTPHZ}$            | T input to pad high-impedance                                   | 0.76        | 0.86   | 0.99 | 0.99 | 0.62 | ns    |
| $T_{IOIBUFDISABLE\_HR}$ | IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks | 1.72        | 1.89   | 2.14 | 2.14 | 2.17 | ns    |
| $T_{IOIBUFDISABLE\_HP}$ | IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks | 1.31        | 1.46   | 1.76 | 1.76 | 1.86 | ns    |

## Input/Output Logic Switching Characteristics

Table 23: ILOGIC Switching Characteristics

| Symbol                      | Description   | Speed Grade |           |           |           |            | Units   |
|-----------------------------|---|-------------|-----------|-----------|-----------|------------|---------|
|                             |   | 1.0V        |           |           |           | 0.9V       |         |
|                             |   | -3          | -2/-2L    | -1        | -1M       | -2L        |         |
| <b>Setup/Hold</b>           |   |             |           |           |           |            |         |
| $T_{ICE1CK}/T_{ICKCE1}$     | CE1 pin Setup/Hold with respect to CLK  | 0.42/0.00   | 0.48/0.00 | 0.67/0.00 | 0.67/0.00 | 0.56/-0.16 | ns      |
| $T_{ISRCK}/T_{ICKSR}$       | SR pin Setup/Hold with respect to CLK   | 0.53/0.01   | 0.61/0.01 | 0.99/0.01 | 0.99/0.01 | 0.88/-0.30 | ns      |
| $T_{IDOCKE2}/T_{IOCKDE2}$   | D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)          | 0.01/0.27   | 0.01/0.29 | 0.01/0.34 | 0.01/0.34 | 0.01/0.41  | ns      |
| $T_{IDOCKDE2}/T_{IOCKDDE2}$ | DDL pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)       | 0.01/0.27   | 0.02/0.29 | 0.02/0.34 | 0.02/0.34 | 0.01/0.41  | ns      |
| $T_{IDOCKE3}/T_{IOCKDE3}$   | D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)          | 0.01/0.27   | 0.01/0.29 | 0.01/0.34 | 0.01/0.34 | 0.01/0.41  | ns      |
| $T_{IDOCKDE3}/T_{IOCKDDE3}$ | DDL pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)       | 0.01/0.27   | 0.02/0.29 | 0.02/0.34 | 0.02/0.34 | 0.01/0.41  | ns      |
| <b>Combinatorial</b>        |   |             |           |           |           |            |         |
| $T_{IDIE2}$                 | D pin to O pin propagation delay, no Delay (HP I/O banks only)                  | 0.09        | 0.10      | 0.12      | 0.12      | 0.14       | ns      |
| $T_{IDIDE2}$                | DDL pin to O pin propagation delay (using IDELAY) (HP I/O banks only)           | 0.10        | 0.11      | 0.13      | 0.13      | 0.15       | ns      |
| $T_{IDIE3}$                 | D pin to O pin propagation delay, no Delay (HR I/O banks only)                  | 0.09        | 0.10      | 0.12      | 0.12      | 0.14       | ns      |
| $T_{IDIDE3}$                | DDL pin to O pin propagation delay (using IDELAY) (HR I/O banks only)           | 0.10        | 0.11      | 0.13      | 0.13      | 0.15       | ns      |
| <b>Sequential Delays</b>    |   |             |           |           |           |            |         |
| $T_{IDLOE2}$                | D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)    | 0.36        | 0.39      | 0.45      | 0.45      | 0.54       | ns      |
| $T_{IDLDE2}$                | DDL pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only) | 0.36        | 0.39      | 0.45      | 0.45      | 0.55       | ns      |
| $T_{IDLOE3}$                | D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)    | 0.36        | 0.39      | 0.45      | 0.45      | 0.54       | ns      |
| $T_{IDLDE3}$                | DDL pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only) | 0.36        | 0.39      | 0.45      | 0.45      | 0.55       | ns      |
| $T_{ICKQ}$                  | CLK to Q outputs  | 0.47        | 0.50      | 0.58      | 0.58      | 0.71       | ns      |
| $T_{RQ\_ILOGICE2}$          | SR pin to OQ/TQ out (HP I/O banks only)   | 0.84        | 0.94      | 1.16      | 1.16      | 1.32       | ns      |
| $T_{GSRQ\_ILOGICE2}$        | Global Set/Reset to Q outputs (HP I/O banks only)                               | 7.60        | 7.60      | 10.51     | 10.51     | 11.39      | ns      |
| $T_{RQ\_ILOGICE3}$          | SR pin to OQ/TQ out (HR I/O banks only)   | 0.84        | 0.94      | 1.16      | 1.16      | 1.32       | ns      |
| $T_{GSRQ\_ILOGICE3}$        | Global Set/Reset to Q outputs (HR I/O banks only)                               | 7.60        | 7.60      | 10.51     | 10.51     | 11.39      | ns      |
| <b>Set/Reset</b>            |   |             |           |           |           |            |         |
| $T_{RPW\_ILOGICE2}$         | Minimum Pulse Width, SR inputs (HP I/O banks only)                              | 0.54        | 0.63      | 0.63      | 0.63      | 0.68       | ns, Min |
| $T_{RPW\_ILOGICE3}$         | Minimum Pulse Width, SR inputs (HR I/O banks only)                              | 0.54        | 0.63      | 0.63      | 0.63      | 0.68       | ns, Min |



Table 24: OLOGIC Switching Characteristics

| Symbol                   | Description  | Speed Grade |            |            |            |            | Units   |
|--------------------------|--|-------------|------------|------------|------------|------------|---------|
|                          |  | 1.0V        |            |            |            | 0.9V       |         |
|                          |  | -3          | -2/-2L     | -1         | -1M        | -2L        |         |
| <b>Setup/Hold</b>        |  |             |            |            |            |            |         |
| $T_{ODCK}/T_{OCKD}$      | D1/D2 pins Setup/Hold with respect to CLK          | 0.45/-0.13  | 0.50/-0.13 | 0.58/-0.13 | 0.58/-0.13 | 0.79/-0.18 | ns      |
| $T_{OOCECK}/T_{OCKOCE}$  | OCE pin Setup/Hold with respect to CLK             | 0.28/0.03   | 0.29/0.03  | 0.45/0.03  | 0.45/0.03  | 0.35/-0.10 | ns      |
| $T_{OSRCK}/T_{OCKSR}$    | SR pin Setup/Hold with respect to CLK              | 0.32/0.18   | 0.38/0.18  | 0.70/0.18  | 0.70/0.18  | 0.62/-0.04 | ns      |
| $T_{OTCK}/T_{OCKT}$      | T1/T2 pins Setup/Hold with respect to CLK          | 0.49/-0.16  | 0.56/-0.16 | 0.68/-0.16 | 0.68/-0.13 | 0.67/-0.18 | ns      |
| $T_{OTCECK}/T_{OCKTCE}$  | TCE pin Setup/Hold with respect to CLK             | 0.28/0.01   | 0.30/0.01  | 0.45/0.01  | 0.45/0.06  | 0.31/-0.10 | ns      |
| <b>Combinatorial</b>     |  |             |            |            |            |            |         |
| $T_{ODQ}$                | D1 to OQ out or T1 to TQ out                       | 0.73        | 0.81       | 0.97       | 0.97       | 1.18       | ns      |
| <b>Sequential Delays</b> |  |             |            |            |            |            |         |
| $T_{OCKQ}$               | CLK to OQ/TQ out                                   | 0.41        | 0.43       | 0.49       | 0.49       | 0.63       | ns      |
| $T_{RQ\_OLOGICE2}$       | SR pin to OQ/TQ out (HP I/O banks only)            | 0.63        | 0.70       | 0.83       | 0.83       | 1.12       | ns      |
| $T_{GSRQ\_OLOGICE2}$     | Global Set/Reset to Q outputs (HP I/O banks only)  | 7.60        | 7.60       | 10.51      | 10.51      | 11.39      | ns      |
| $T_{RQ\_OLOGICE3}$       | SR pin to OQ/TQ out (HR I/O banks only)            | 0.63        | 0.70       | 0.83       | 0.83       | 1.12       | ns      |
| $T_{GSRQ\_OLOGICE3}$     | Global Set/Reset to Q outputs (HR I/O banks only)  | 7.60        | 7.60       | 10.51      | 10.51      | 11.39      | ns      |
| <b>Set/Reset</b>         |  |             |            |            |            |            |         |
| $T_{RPW\_OLOGICE2}$      | Minimum Pulse Width, SR inputs (HP I/O banks only) | 0.54        | 0.54       | 0.63       | 0.63       | 0.68       | ns, Min |
| $T_{RPW\_OLOGICE3}$      | Minimum Pulse Width, SR inputs (HR I/O banks only) | 0.54        | 0.54       | 0.63       | 0.63       | 0.68       | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

Table 25: ISERDES Switching Characteristics

| Symbol  | Description  | Speed Grade |            |            |            |            | Units |
|---|--|-------------|------------|------------|------------|------------|-------|
|   |  | 1.0V        |            |            |            | 0.9V       |       |
|   |  | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| <b>Setup/Hold for Control Lines</b>               |  |             |            |            |            |            |       |
| $T_{ISCK\_BITSLIP}/$<br>$T_{ISCK\_BITSLIP}$       | BITSLIP pin Setup/Hold with respect to CLKDIV                                  | 0.01/0.12   | 0.02/0.13  | 0.02/0.15  | 0.02/0.15  | 0.02/0.21  | ns    |
| $T_{ISCK\_CE}/$<br>$T_{ISCK\_CE}^{(2)}$           | CE pin Setup/Hold with respect to CLK (for CE1)                                | 0.39/-0.02  | 0.44/-0.02 | 0.63/-0.02 | 0.63/-0.02 | 0.51/-0.22 | ns    |
| $T_{ISCK\_CE2}/$<br>$T_{ISCK\_CE2}^{(2)}$         | CE pin Setup/Hold with respect to CLKDIV (for CE2)                             | -0.12/0.29  | -0.12/0.31 | -0.12/0.35 | -0.12/0.35 | -0.17/0.40 | ns    |
| <b>Setup/Hold for Data Lines</b>                  |  |             |            |            |            |            |       |
| $T_{ISDCK\_D}/$<br>$T_{ISCKD\_D}$                 | D pin Setup/Hold with respect to CLK   | -0.02/0.11  | -0.02/0.12 | -0.02/0.15 | -0.02/0.15 | -0.04/0.19 | ns    |
| $T_{ISDCK\_DDLY}/$<br>$T_{ISCKD\_DDLY}$           | DDLY pin Setup/Hold with respect to CLK (using IDELAY) <sup>(1)</sup>          | -0.02/0.11  | -0.02/0.12 | -0.02/0.15 | -0.02/0.15 | -0.03/0.19 | ns    |
| $T_{ISDCK\_D\_DDR}/$<br>$T_{ISCKD\_D\_DDR}$       | D pin Setup/Hold with respect to CLK at DDR mode                               | -0.02/0.11  | -0.02/0.12 | -0.02/0.15 | -0.02/0.15 | -0.04/0.19 | ns    |
| $T_{ISDCK\_DDLY\_DDR}/$<br>$T_{ISCKD\_DDLY\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) <sup>(1)</sup> | 0.11/0.11   | 0.12/0.12  | 0.15/0.15  | 0.15/0.15  | 0.19/0.19  | ns    |
| <b>Sequential Delays</b>                          |  |             |            |            |            |            |       |
| $T_{ISCKO\_Q}$                                    | CLKDIV to out at Q pin   | 0.46        | 0.47       | 0.58       | 0.58       | 0.67       | ns    |
| <b>Propagation Delays</b>                         |  |             |            |            |            |            |       |
| $T_{ISDO\_DO}$                                    | D input to DO output pin   | 0.09        | 0.10       | 0.12       | 0.12       | 0.14       | ns    |

**Notes:**

- Recorded at 0 tap value.
- $T_{ISCK\_CE2}$  and  $T_{ISCK\_CE2}$  are reported as  $T_{ISCK\_CE}/T_{ISCK\_CE}$  in the timing report.

## Output Serializer/Deserializer Switching Characteristics

Table 26: OSERDES Switching Characteristics

| Symbol                              | Description                                   | Speed Grade |            |            |            |            | Units |
|-------------------------------------|---|-------------|------------|------------|------------|------------|-------|
|                                     |   | 1.0V        |            |            |            | 0.9V       |       |
|                                     |   | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| <b>Setup/Hold</b>                   |   |             |            |            |            |            |       |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$         | D input Setup/Hold with respect to CLKDIV     | 0.37/0.02   | 0.40/0.02  | 0.55/0.02  | 0.55/0.02  | 0.44/-0.24 | ns    |
| $T_{OSDCK\_T}/T_{OSCKD\_T}^{(1)}$   | T input Setup/Hold with respect to CLK        | 0.49/-0.15  | 0.56/-0.15 | 0.68/-0.15 | 0.68/-0.15 | 0.67/-0.25 | ns    |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}^{(1)}$ | T input Setup/Hold with respect to CLKDIV     | 0.27/-0.15  | 0.30/-0.15 | 0.34/-0.15 | 0.34/-0.15 | 0.46/-0.25 | ns    |
| $T_{OSCKC\_OCE}/T_{OSCKC\_OCE}$     | OCE input Setup/Hold with respect to CLK      | 0.28/0.03   | 0.29/0.03  | 0.45/0.03  | 0.45/0.03  | 0.35/-0.15 | ns    |
| $T_{OSCKC\_S}$                      | SR (Reset) input Setup with respect to CLKDIV | 0.41        | 0.46       | 0.75       | 0.75       | 0.70       | ns    |
| $T_{OSCKC\_TCE}/T_{OSCKC\_TCE}$     | TCE input Setup/Hold with respect to CLK      | 0.28/0.01   | 0.30/0.01  | 0.45/0.01  | 0.45/0.01  | 0.31/-0.15 | ns    |
| <b>Sequential Delays</b>            |   |             |            |            |            |            |       |
| $T_{OSCKO\_OQ}$                     | Clock to out from CLK to OQ                   | 0.35        | 0.37       | 0.42       | 0.42       | 0.54       | ns    |
| $T_{OSCKO\_TQ}$                     | Clock to out from CLK to TQ                   | 0.41        | 0.43       | 0.49       | 0.49       | 0.63       | ns    |
| <b>Combinatorial</b>                |   |             |            |            |            |            |       |
| $T_{OSDO\_TTQ}$                     | T input to TQ Out                             | 0.73        | 0.81       | 0.97       | 0.97       | 1.18       | ns    |

**Notes:**

- $T_{OSDCK\_T2}$  and  $T_{OSCKD\_T2}$  are reported as  $T_{OSDCK\_T}/T_{OSCKD\_T}$  in the timing report.

## Input/Output Delay Switching Characteristics

Table 27: Input/Output Delay Switching Characteristics

| Symbol   | Description   | Speed Grade                    |           |           |           |           | Units      |
|--|---|--------------------------------|-----------|-----------|-----------|-----------|------------|
|  |   | 1.0V                           |           |           |           | 0.9V      |            |
|  |   | -3                             | -2/-2L    | -1        | -1M       | -2L       |            |
| <b>IDELAYCTRL</b>  |   |                                |           |           |           |           |            |
| T <sub>DLYCCO_RDY</sub>                                      | Reset to Ready for IDELAYCTRL   | 3.22                           | 3.22      | 3.22      | 3.22      | 3.22      | µs         |
| F <sub>IDELAYCTRL_REF</sub>                                  | Attribute REFCLK frequency = 200.00 <sup>(1)</sup>  | 200.00                         | 200.00    | 200.00    | 200.00    | 200.00    | MHz        |
|  | Attribute REFCLK frequency = 300.00 <sup>(1)</sup>  | 300.00                         | 300.00    | N/A       | N/A       | N/A       | MHz        |
| IDELAYCTRL_REF_PRECISION                                     | REFCLK precision  | ±10                            | ±10       | ±10       | ±10       | ±10       | MHz        |
| T <sub>IDELAYCTRL_RPW</sub>                                  | Minimum Reset pulse width   | 52.00                          | 52.00     | 52.00     | 52.00     | 52.00     | ns         |
| <b>IDELAY/ODELAY</b>   |   |                                |           |           |           |           |            |
| T <sub>IDELAYRESOLUTION</sub>                                | IDELAY/ODELAY chain delay resolution  | 1/(32 x 2 x F <sub>REF</sub> ) |           |           |           |           | ps         |
| T <sub>IDELAYPAT_JIT</sub> and<br>T <sub>ODELAYPAT_JIT</sub> | Pattern dependent period jitter in delay chain for clock pattern. <sup>(2)</sup>                | 0                              | 0         | 0         | 0         | 0         | ps per tap |
|  | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) <sup>(3)</sup> | ±5                             | ±5        | ±5        | ±5        | ±5        | ps per tap |
|  | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) <sup>(4)</sup> | ±9                             | ±9        | ±9        | ±9        | ±9        | ps per tap |
| T <sub>IDELAY_CLK_MAX</sub> /<br>T <sub>ODELAY_CLK_MAX</sub> | Maximum frequency of CLK input to IDELAY/ODELAY   | 800.00                         | 800.00    | 710.00    | 710.00    | 710.00    | MHz        |
| T <sub>IDCCK_CE</sub> /<br>T <sub>IDCKC_CE</sub>             | CE pin Setup/Hold with respect to C for IDELAY  | 0.11/0.10                      | 0.14/0.12 | 0.18/0.14 | 0.18/0.14 | 0.14/0.16 | ns         |
| T <sub>ODCCK_CE</sub> /<br>T <sub>ODCKC_CE</sub>             | CE pin Setup/Hold with respect to C for ODELAY  | 0.14/0.03                      | 0.16/0.04 | 0.19/0.05 | 0.19/0.05 | 0.28/0.06 | ns         |
| T <sub>IDCCK_INC</sub> /<br>T <sub>IDCKC_INC</sub>           | INC pin Setup/Hold with respect to C for IDELAY   | 0.10/0.14                      | 0.12/0.16 | 0.14/0.20 | 0.14/0.20 | 0.10/0.23 | ns         |
| T <sub>ODCCK_INC</sub> /<br>T <sub>ODCKC_INC</sub>           | INC pin Setup/Hold with respect to C for ODELAY   | 0.10/0.07                      | 0.12/0.08 | 0.13/0.09 | 0.13/0.09 | 0.19/0.16 | ns         |
| T <sub>IDCCK_RST</sub> /<br>T <sub>IDCKC_RST</sub>           | RST pin Setup/Hold with respect to C for IDELAY   | 0.13/0.08                      | 0.14/0.10 | 0.16/0.12 | 0.16/0.12 | 0.22/0.19 | ns         |
| T <sub>ODCCK_RST</sub> /<br>T <sub>ODCKC_RST</sub>           | RST pin Setup/Hold with respect to C for ODELAY   | 0.16/0.04                      | 0.19/0.06 | 0.24/0.08 | 0.24/0.08 | 0.32/0.11 | ns         |
| T <sub>IDDO_IDATAIN</sub>                                    | Propagation delay through IDELAY  | Note 5                         | Note 5    | Note 5    | Note 5    | Note 5    | ps         |
| T <sub>ODDO_ODATAIN</sub>                                    | Propagation delay through ODELAY  | Note 5                         | Note 5    | Note 5    | Note 5    | Note 5    | ps         |

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH\_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH\_PERFORMANCE mode is set to TRUE.
4. When HIGH\_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 28: IO\_FIFO Switching Characteristics

| Symbol                             | Description            | Speed Grade |            |            |            |            | Units |
|------------------------------------|------------------------|-------------|------------|------------|------------|------------|-------|
|                                    |                        | 1.0V        |            |            |            | 0.9V       |       |
|                                    |                        | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| <b>IO_FIFO Clock to Out Delays</b> |                        |             |            |            |            |            |       |
| $T_{OFFCKO\_DO}$                   | RDCLK to Q outputs     | 0.51        | 0.56       | 0.63       | 0.63       | 0.81       | ns    |
| $T_{CKO\_FLAGS}$                   | Clock to IO_FIFO Flags | 0.59        | 0.62       | 0.81       | 0.81       | 0.77       | ns    |
| <b>Setup/Hold</b>                  |                        |             |            |            |            |            |       |
| $T_{CCK\_D}/T_{CKC\_D}$            | D inputs to WRCLK      | 0.43/-0.01  | 0.47/-0.01 | 0.53/-0.01 | 0.53/0.09  | 0.76/-0.05 | ns    |
| $T_{IFFCK\_WREN}/T_{IFFCKC\_WREN}$ | WREN to WRCLK          | 0.39/-0.01  | 0.43/-0.01 | 0.50/-0.01 | 0.50/-0.01 | 0.70/-0.05 | ns    |
| $T_{OFFCK\_RDEN}/T_{OFFCKC\_RDEN}$ | RDEN to RDCLK          | 0.49/0.01   | 0.53/0.02  | 0.61/0.02  | 0.61/0.02  | 0.79/-0.02 | ns    |
| <b>Minimum Pulse Width</b>         |                        |             |            |            |            |            |       |
| $T_{PWH\_IO\_FIFO}$                | RESET, RDCLK, WRCLK    | 0.81        | 0.92       | 1.08       | 1.08       | 1.29       | ns    |
| $T_{PWL\_IO\_FIFO}$                | RESET, RDCLK, WRCLK    | 0.81        | 0.92       | 1.08       | 1.08       | 1.29       | ns    |
| <b>Maximum Frequency</b>           |                        |             |            |            |            |            |       |
| $F_{MAX}$                          | RDCLK and WRCLK        | 533.05      | 470.37     | 400.00     | 400.00     | 333.33     | MHz   |

## CLB Switching Characteristics

Table 29: CLB Switching Characteristics

| Symbol   | Description  | Speed Grade |           |           |           |           | Units   |
|--|--|-------------|-----------|-----------|-----------|-----------|---------|
|  |  | 1.0V        |           |           |           | 0.9V      |         |
|  |  | -3          | -2/-2L    | -1        | -1M       | -2L       |         |
| <b>Combinatorial Delays</b>  |  |             |           |           |           |           |         |
| $T_{ILO}$  | An – Dn LUT address to A   | 0.05        | 0.05      | 0.06      | 0.06      | 0.07      | ns, Max |
| $T_{ILO\_2}$   | An – Dn LUT address to AMUX/CMUX   | 0.15        | 0.16      | 0.19      | 0.19      | 0.22      | ns, Max |
| $T_{ILO\_3}$   | An – Dn LUT address to BMUX_A  | 0.24        | 0.25      | 0.30      | 0.30      | 0.37      | ns, Max |
| $T_{ITO}$  | An – Dn inputs to A – D Q outputs  | 0.58        | 0.61      | 0.74      | 0.74      | 0.91      | ns, Max |
| $T_{AXA}$  | AX inputs to AMUX output   | 0.38        | 0.40      | 0.49      | 0.49      | 0.62      | ns, Max |
| $T_{AXB}$  | AX inputs to BMUX output   | 0.40        | 0.42      | 0.52      | 0.52      | 0.66      | ns, Max |
| $T_{AXC}$  | AX inputs to CMUX output   | 0.39        | 0.41      | 0.50      | 0.50      | 0.62      | ns, Max |
| $T_{AXD}$  | AX inputs to DMUX output   | 0.43        | 0.44      | 0.52      | 0.52      | 0.67      | ns, Max |
| $T_{BXB}$  | BX inputs to BMUX output   | 0.31        | 0.33      | 0.40      | 0.40      | 0.51      | ns, Max |
| $T_{BXD}$  | BX inputs to DMUX output   | 0.38        | 0.39      | 0.47      | 0.47      | 0.62      | ns, Max |
| $T_{CXC}$  | CX inputs to CMUX output   | 0.27        | 0.28      | 0.34      | 0.34      | 0.43      | ns, Max |
| $T_{CXD}$  | CX inputs to DMUX output   | 0.33        | 0.34      | 0.41      | 0.41      | 0.54      | ns, Max |
| $T_{DXD}$  | DX inputs to DMUX output   | 0.32        | 0.33      | 0.40      | 0.40      | 0.52      | ns, Max |
| <b>Sequential Delays</b>   |  |             |           |           |           |           |         |
| $T_{CKO}$  | Clock to AQ – DQ outputs   | 0.26        | 0.27      | 0.32      | 0.32      | 0.40      | ns, Max |
| $T_{SHCKO}$  | Clock to AMUX – DMUX outputs   | 0.32        | 0.32      | 0.39      | 0.39      | 0.46      | ns, Max |
| <b>Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK</b> |  |             |           |           |           |           |         |
| $T_{AS}/T_{AH}$  | $A_N – D_N$ input to CLK on A – D Flip Flops                                 | 0.01/0.12   | 0.02/0.13 | 0.03/0.18 | 0.03/0.24 | 0.02/0.18 | ns, Min |
| $T_{DICK}/T_{CKDI}$  | $A_X – D_X$ input to CLK on A – D Flip Flops                                 | 0.04/0.14   | 0.04/0.14 | 0.05/0.20 | 0.05/0.26 | 0.05/0.21 | ns, Min |
|  | $A_X – D_X$ input through MUXs and/or carry logic to CLK on A – D Flip Flops | 0.36/0.10   | 0.37/0.11 | 0.46/0.16 | 0.46/0.22 | 0.56/0.15 | ns, Min |
| $T_{CECK\_CLB}/T_{CKCE\_CLB}$  | CE input to CLK on A – D Flip Flops  | 0.19/0.05   | 0.20/0.05 | 0.25/0.05 | 0.25/0.11 | 0.24/0.04 | ns, Min |
| $T_{SRCK}/T_{CKSR}$  | SR input to CLK on A – D Flip Flops  | 0.30/0.05   | 0.31/0.07 | 0.37/0.09 | 0.37/0.22 | 0.48/0.05 | ns, Min |
| <b>Set/Reset</b>   |  |             |           |           |           |           |         |
| $T_{SRMIN}$  | SR input minimum pulse width   | 0.52        | 0.78      | 1.04      | 1.04      | 0.95      | ns, Min |
| $T_{RQ}$   | Delay from SR input to AQ – DQ flip-flops                                    | 0.38        | 0.38      | 0.46      | 0.46      | 0.59      | ns, Max |
| $T_{CEO}$  | Delay from CE input to AQ – DQ flip-flops                                    | 0.34        | 0.35      | 0.43      | 0.43      | 0.54      | ns, Max |
| $F_{TOG}$  | Toggle frequency (for export control)  | 1818        | 1818      | 1818      | 1818      | 1286      | MHz     |

**CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Table 30: CLB Distributed RAM Switching Characteristics

| Symbol   | Description  | Speed Grade |           |           |           |           | Units   |
|--|--|-------------|-----------|-----------|-----------|-----------|---------|
|  |  | 1.0V        |           |           |           | 0.9V      |         |
|  |  | -3          | -2/-2L    | -1        | -1M       | -2L       |         |
| <b>Sequential Delays</b>                           |  |             |           |           |           |           |         |
| T <sub>SHCKO</sub>                                 | Clock to A – B outputs                                     | 0.68        | 0.70      | 0.85      | 0.85      | 1.08      | ns, Max |
| T <sub>SHCKO_1</sub>                               | Clock to AMUX – BMUX outputs                               | 0.91        | 0.95      | 1.15      | 1.15      | 1.44      | ns, Max |
| <b>Setup and Hold Times Before/After Clock CLK</b> |  |             |           |           |           |           |         |
| T <sub>DS_LRAM</sub> /T <sub>DH_LRAM</sub>         | A – D inputs to CLK  | 0.45/0.23   | 0.45/0.24 | 0.54/0.27 | 0.54/0.28 | 0.69/0.33 | ns, Min |
| T <sub>AS_LRAM</sub> /T <sub>AH_LRAM</sub>         | Address An inputs to clock                                 | 0.13/0.50   | 0.14/0.50 | 0.17/0.58 | 0.17/0.61 | 0.21/0.63 | ns, Min |
|  | Address An inputs through MUXs and/or carry logic to clock | 0.40/0.16   | 0.42/0.17 | 0.52/0.23 | 0.52/0.29 | 0.63/0.23 | ns, Min |
| T <sub>WS_LRAM</sub> /T <sub>WH_LRAM</sub>         | WE input to clock  | 0.29/0.09   | 0.30/0.09 | 0.36/0.09 | 0.36/0.11 | 0.46/0.10 | ns, Min |
| T <sub>CECK_LRAM</sub> /<br>T <sub>CKCE_LRAM</sub> | CE input to CLK  | 0.29/0.09   | 0.30/0.09 | 0.37/0.09 | 0.37/0.11 | 0.47/0.10 | ns, Min |
| <b>Clock CLK</b>                                   |  |             |           |           |           |           |         |
| T <sub>MPW</sub>                                   | Minimum pulse width  | 0.68        | 0.77      | 0.91      | 0.91      | 1.11      | ns, Min |
| T <sub>MCP</sub>                                   | Minimum clock period                                       | 1.35        | 1.54      | 1.82      | 1.82      | 2.22      | ns, Min |

**Notes:**

1. T<sub>SHCKO</sub> also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

**CLB Shift Register Switching Characteristics (SLICEM Only)**

Table 31: CLB Shift Register Switching Characteristics

| Symbol   | Description                         | Speed Grade |           |           |           |           | Units   |
|--|-------------------------------------|-------------|-----------|-----------|-----------|-----------|---------|
|  |                                     | 1.0V        |           |           |           | 0.9V      |         |
|  |                                     | -3          | -2/-2L    | -1        | -1M       | -2L       |         |
| <b>Sequential Delays</b>                               |                                     |             |           |           |           |           |         |
| T <sub>REG</sub>                                       | Clock to A – D outputs              | 0.96        | 0.98      | 1.20      | 1.20      | 1.35      | ns, Max |
| T <sub>REG_MUX</sub>                                   | Clock to AMUX – DMUX output         | 1.19        | 1.23      | 1.50      | 1.50      | 1.72      | ns, Max |
| T <sub>REG_M31</sub>                                   | Clock to DMUX output via M31 output | 0.89        | 0.91      | 1.10      | 1.10      | 1.25      | ns, Max |
| <b>Setup and Hold Times Before/After Clock CLK</b>     |                                     |             |           |           |           |           |         |
| T <sub>WS_SHFREG</sub> /<br>T <sub>WH_SHFREG</sub>     | WE input                            | 0.26/0.09   | 0.27/0.09 | 0.33/0.09 | 0.33/0.11 | 0.41/0.10 | ns, Min |
| T <sub>CECK_SHFREG</sub> /<br>T <sub>CKCE_SHFREG</sub> | CE input to CLK                     | 0.27/0.09   | 0.28/0.09 | 0.33/0.09 | 0.33/0.11 | 0.42/0.10 | ns, Min |
| T <sub>DS_SHFREG</sub> /<br>T <sub>DH_SHFREG</sub>     | A – D inputs to CLK                 | 0.28/0.26   | 0.28/0.26 | 0.33/0.30 | 0.33/0.36 | 0.41/0.36 | ns, Min |
| <b>Clock CLK</b>                                       |                                     |             |           |           |           |           |         |
| T <sub>MPW_SHFREG</sub>                                | Minimum pulse width                 | 0.55        | 0.65      | 0.78      | 0.78      | 0.91      | ns, Min |

## Block RAM and FIFO Switching Characteristics

Table 32: Block RAM and FIFO Switching Characteristics

| Symbol   | Description   | Speed Grade |           |           |           |           | Units   |
|--|---|-------------|-----------|-----------|-----------|-----------|---------|
|  |   | 1.0V        |           |           |           | 0.9V      |         |
|  |   | -3          | -2/-2L    | -1        | -1M       | -2L       |         |
| <b>Block RAM and FIFO Clock-to-Out Delays</b>                        |   |             |           |           |           |           |         |
| T <sub>RCKO_DO</sub> and<br>T <sub>RCKO_DO_REG</sub> <sup>(1)</sup>  | Clock CLK to DOUT output (without output register) <sup>(2)(3)</sup>                                    | 1.57        | 1.80      | 2.08      | 2.08      | 2.44      | ns, Max |
|  | Clock CLK to DOUT output (with output register) <sup>(4)(5)</sup>                                       | 0.54        | 0.63      | 0.75      | 0.75      | 0.86      | ns, Max |
| T <sub>RCKO_DO_ECC</sub> and<br>T <sub>RCKO_DO_ECC_REG</sub>         | Clock CLK to DOUT output with ECC (without output register) <sup>(2)(3)</sup>                           | 2.35        | 2.58      | 3.26      | 3.26      | 4.49      | ns, Max |
|  | Clock CLK to DOUT output with ECC (with output register) <sup>(4)(5)</sup>                              | 0.62        | 0.69      | 0.80      | 0.80      | 0.94      | ns, Max |
| T <sub>RCKO_DO_CASCADE</sub> and<br>T <sub>RCKO_DO_CASCADE_REG</sub> | Clock CLK to DOUT output with Cascade (without output register) <sup>(2)</sup>                          | 2.21        | 2.45      | 2.80      | 2.80      | 3.19      | ns, Max |
|  | Clock CLK to DOUT output with Cascade (with output register) <sup>(4)</sup>                             | 0.98        | 1.08      | 1.24      | 1.24      | 1.32      | ns, Max |
| T <sub>RCKO_FLAGS</sub>  | Clock CLK to FIFO flags outputs <sup>(6)</sup>  | 0.65        | 0.74      | 0.89      | 0.89      | 0.97      | ns, Max |
| T <sub>RCKO_POINTERS</sub>   | Clock CLK to FIFO pointers outputs <sup>(7)</sup>   | 0.79        | 0.87      | 0.98      | 0.98      | 1.10      | ns, Max |
| T <sub>RCKO_PARITY_ECC</sub>   | Clock CLK to ECCPARITY in ECC encode only mode  | 0.66        | 0.72      | 0.80      | 0.80      | 0.93      | ns, Max |
| T <sub>RCKO_SDBIT_ECC</sub> and<br>T <sub>RCKO_SDBIT_ECC_REG</sub>   | Clock CLK to BITERR (without output register)   | 2.17        | 2.38      | 3.01      | 3.01      | 4.15      | ns, Max |
|  | Clock CLK to BITERR (with output register)  | 0.57        | 0.65      | 0.76      | 0.76      | 0.89      | ns, Max |
| T <sub>RCKO_RDADDR_ECC</sub> and<br>T <sub>RCKO_RDADDR_ECC_REG</sub> | Clock CLK to RDADDR output with ECC (without output register)   | 0.64        | 0.74      | 0.90      | 0.90      | 0.98      | ns, Max |
|  | Clock CLK to RDADDR output with ECC (with output register)  | 0.71        | 0.79      | 0.92      | 0.92      | 1.10      | ns, Max |
| <b>Setup and Hold Times Before/After Clock CLK</b>                   |   |             |           |           |           |           |         |
| T <sub>RCKC_ADDRA</sub> /T <sub>RCKC_ADDRA</sub>                     | ADDR inputs <sup>(8)</sup>  | 0.38/0.27   | 0.42/0.28 | 0.48/0.31 | 0.48/0.38 | 0.65/0.38 | ns, Min |
| T <sub>RDCK_DI_WF_NC</sub> /<br>T <sub>RCKD_DI_WF_NC</sub>           | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode <sup>(9)</sup> | 0.49/0.51   | 0.55/0.53 | 0.63/0.57 | 0.63/0.57 | 0.78/0.64 | ns, Min |
| T <sub>RDCK_DI_RF</sub> /T <sub>RCKD_DI_RF</sub>                     | Data input setup/hold time when block RAM is configured in READ_FIRST mode <sup>(9)</sup>               | 0.17/0.25   | 0.19/0.29 | 0.21/0.35 | 0.21/0.35 | 0.25/0.32 | ns, Min |
| T <sub>RDCK_DI_ECC</sub> /<br>T <sub>RCKD_DI_ECC</sub>               | DIN inputs with block RAM ECC in standard mode <sup>(9)</sup>   | 0.42/0.37   | 0.47/0.39 | 0.53/0.43 | 0.53/0.58 | 0.66/0.46 | ns, Min |
| T <sub>RDCK_DI_ECCW</sub> /<br>T <sub>RCKD_DI_ECCW</sub>             | DIN inputs with block RAM ECC encode only <sup>(9)</sup>  | 0.79/0.37   | 0.87/0.39 | 0.99/0.43 | 0.99/0.58 | 1.17/0.41 | ns, Min |
| T <sub>RDCK_DI_ECC_FIFO</sub> /<br>T <sub>RCKD_DI_ECC_FIFO</sub>     | DIN inputs with FIFO ECC in standard mode <sup>(9)</sup>  | 0.89/0.47   | 0.98/0.50 | 1.12/0.54 | 1.12/0.69 | 1.32/0.65 | ns, Min |



Table 32: Block RAM and FIFO Switching Characteristics (Cont'd)

| Symbol  | Description   | Speed Grade |            |            |            |            | Units   |
|---|---|-------------|------------|------------|------------|------------|---------|
|   |   | 1.0V        |            |            |            | 0.9V       |         |
|   |   | -3          | -2/-2L     | -1         | -1M        | -2L        |         |
| $T_{RCKK\_INJECTBITERR}/T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode  | 0.49/0.30   | 0.55/0.31  | 0.63/0.34  | 0.63/0.43  | 0.78/0.41  | ns, Min |
| $T_{RCKK\_EN}/T_{RCKC\_EN}$                     | Block RAM Enable (EN) input   | 0.30/0.17   | 0.33/0.18  | 0.38/0.20  | 0.38/0.32  | 0.48/0.22  | ns, Min |
| $T_{RCKK\_REGCE}/T_{RCKC\_REGCE}$               | CE input of output register   | 0.21/0.13   | 0.25/0.13  | 0.31/0.14  | 0.31/0.19  | 0.34/0.16  | ns, Min |
| $T_{RCKK\_RSTREG}/T_{RCKC\_RSTREG}$             | Synchronous RSTREG input  | 0.25/0.06   | 0.27/0.06  | 0.29/0.06  | 0.29/0.14  | 0.35/0.06  | ns, Min |
| $T_{RCKK\_RSTRAM}/T_{RCKC\_RSTRAM}$             | Synchronous RSTRAM input  | 0.27/0.35   | 0.29/0.37  | 0.31/0.39  | 0.31/0.39  | 0.34/0.40  | ns, Min |
| $T_{RCKK\_WEA}/T_{RCKC\_WEA}$                   | Write Enable (WE) input (Block RAM only)  | 0.38/0.15   | 0.41/0.16  | 0.46/0.17  | 0.46/0.29  | 0.54/0.19  | ns, Min |
| $T_{RCKK\_WREN}/T_{RCKC\_WREN}$                 | WREN FIFO inputs  | 0.39/0.25   | 0.39/0.30  | 0.40/0.37  | 0.40/0.49  | 0.65/0.37  | ns, Min |
| $T_{RCKK\_RDEN}/T_{RCKC\_RDEN}$                 | RDEN FIFO inputs  | 0.36/0.26   | 0.36/0.30  | 0.37/0.37  | 0.37/0.49  | 0.60/0.38  | ns, Min |
| <b>Reset Delays</b>                             |   |             |            |            |            |            |         |
| $T_{RCO\_FLAGS}$                                | Reset RST to FIFO flags/pointers <sup>(10)</sup>  | 0.76        | 0.83       | 0.93       | 0.93       | 1.06       | ns, Max |
| $T_{RREC\_RST}/T_{RREM\_RST}$                   | FIFO reset recovery and removal timing <sup>(11)</sup>  | 1.59/-0.68  | 1.76/-0.68 | 2.01/-0.68 | 2.01/-0.68 | 2.07/-0.60 | ns, Max |
| <b>Maximum Frequency</b>                        |   |             |            |            |            |            |         |
| $F_{MAX\_BRAM\_WF\_NC}$                         | Block RAM (Write first and No change modes)<br>When not in SDP RF mode  | 601.32      | 543.77     | 458.09     | 458.09     | 372.44     | MHz     |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$                | Block RAM (Read first, Performance mode)<br>When in SDP RF mode but no address overlap between port A and port B                            | 601.32      | 543.77     | 458.09     | 458.09     | 372.44     | MHz     |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$             | Block RAM (Read first, Delayed_write mode)<br>When in SDP RF mode and there is possibility of overlap between port A and port B addresses   | 528.26      | 477.33     | 400.80     | 400.80     | 317.36     | MHz     |
| $F_{MAX\_CAS\_WF\_NC}$                          | Block RAM Cascade (Write first, No change mode)<br>When cascade but not in RF mode  | 551.27      | 493.83     | 408.00     | 408.00     | 322.48     | MHz     |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$                 | Block RAM Cascade (Read first, Performance mode)<br>When in cascade with RF mode and no possibility of address overlap/one port is disabled | 551.27      | 493.83     | 408.00     | 408.00     | 322.48     | MHz     |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$              | When in cascade RF mode and there is a possibility of address overlap between port A and port B   | 478.24      | 427.35     | 350.88     | 350.88     | 267.38     | MHz     |

**Table 32: Block RAM and FIFO Switching Characteristics (Cont'd)**

| Symbol          | Description                             | Speed Grade |        |        |        |        | Units |
|-----------------|---|-------------|--------|--------|--------|--------|-------|
|                 |   | 1.0V        |        |        |        | 0.9V   |       |
|                 |   | -3          | -2/-2L | -1     | -1M    | -2L    |       |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC           | 601.32      | 543.77 | 458.09 | 458.09 | 372.44 | MHz   |
| $F_{MAX\_ECC}$  | Block RAM and FIFO in ECC configuration | 484.26      | 430.85 | 351.12 | 351.12 | 254.13 | MHz   |

**Notes:**

1. The timing report shows all of these parameters as  $T_{RCKO\_DO}$ .
2.  $T_{RCKO\_DOR}$  includes  $T_{RCKO\_DOW}$ ,  $T_{RCKO\_DOPR}$ , and  $T_{RCKO\_DOPW}$  as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with  $DO\_REG = 0$ .
4.  $T_{RCKO\_DO}$  includes  $T_{RCKO\_DOP}$  as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with  $DO\_REG = 1$ .
6.  $T_{RCKO\_FLAGS}$  includes the following parameters:  $T_{RCKO\_AEMPTY}$ ,  $T_{RCKO\_AFULL}$ ,  $T_{RCKO\_EMPTY}$ ,  $T_{RCKO\_FULL}$ ,  $T_{RCKO\_RDERR}$ ,  $T_{RCKO\_WRERR}$ .
7.  $T_{RCKO\_POINTERS}$  includes both  $T_{RCKO\_RDCOUNT}$  and  $T_{RCKO\_WRCOUNT}$ .
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10.  $T_{RCKO\_FLAGS}$  includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

Table 33: DSP48E1 Switching Characteristics

| Symbol  | Description   | Speed Grade    |                |                |                |                | Units |
|---|---|----------------|----------------|----------------|----------------|----------------|-------|
|   |   | 1.0V           |                |                |                | 0.9V           |       |
|   |   | -3             | -2/-2L         | -1             | -1M            | -2L            |       |
| <b>Setup and Hold Times of Data/Control Pins to the Input Register Clock</b>          |   |                |                |                |                |                |       |
| $T_{DSPDCK\_A\_AREG}/T_{DSPCKD\_A\_AREG}$   | A input to A register CLK                           | 0.24/<br>0.12  | 0.27/<br>0.14  | 0.31/<br>0.16  | 0.33/<br>0.18  | 0.38/<br>0.12  | ns    |
| $T_{DSPDCK\_B\_BREG}/T_{DSPCKD\_B\_BREG}$   | B input to B register CLK                           | 0.28/<br>0.13  | 0.32/<br>0.14  | 0.39/<br>0.15  | 0.41/<br>0.18  | 0.51/<br>0.16  | ns    |
| $T_{DSPDCK\_C\_CREG}/T_{DSPCKD\_C\_CREG}$   | C input to C register CLK                           | 0.15/<br>0.15  | 0.17/<br>0.17  | 0.20/<br>0.20  | 0.20/<br>0.22  | 0.31/<br>0.21  | ns    |
| $T_{DSPDCK\_D\_DREG}/T_{DSPCKD\_D\_DREG}$   | D input to D register CLK                           | 0.21/<br>0.19  | 0.27/<br>0.22  | 0.35/<br>0.26  | 0.35/<br>0.27  | 0.46/<br>0.20  | ns    |
| $T_{DSPDCK\_ACIN\_AREG}/T_{DSPCKD\_ACIN\_AREG}$                                       | ACIN input to A register CLK                        | 0.21/<br>0.12  | 0.24/<br>0.14  | 0.27/<br>0.16  | 0.30/<br>0.16  | 0.31/<br>0.12  | ns    |
| $T_{DSPDCK\_BCIN\_BREG}/T_{DSPCKD\_BCIN\_BREG}$                                       | BCIN input to B register CLK                        | 0.22/<br>0.13  | 0.25/<br>0.14  | 0.30/<br>0.15  | 0.32/<br>0.15  | 0.34/<br>0.16  | ns    |
| <b>Setup and Hold Times of Data Pins to the Pipeline Register Clock</b>               |   |                |                |                |                |                |       |
| $T_{DSPDCK\_ \{A, B\} \_MREG\_MULT}/T_{DSPCKD\_ \{A, B\} \_MREG\_MULT}$               | {A, B} input to M register CLK using multiplier     | 2.04/<br>-0.01 | 2.34/<br>-0.01 | 2.79/<br>-0.01 | 2.79/<br>-0.01 | 3.66/<br>-0.06 | ns    |
| $T_{DSPDCK\_ \{A, D\} \_ADREG}/T_{DSPCKD\_ \{A, D\} \_ADREG}$                         | {A, D} input to AD register CLK                     | 1.09/<br>-0.02 | 1.25/<br>-0.02 | 1.49/<br>-0.02 | 1.49/<br>-0.02 | 1.94/<br>-0.23 | ns    |
| <b>Setup and Hold Times of Data/Control Pins to the Output Register Clock</b>         |   |                |                |                |                |                |       |
| $T_{DSPDCK\_ \{A, B\} \_PREG\_MULT}/T_{DSPCKD\_ \{A, B\} \_PREG\_MULT}$               | {A, B,} input to P register CLK using multiplier    | 3.41/<br>-0.24 | 3.90/<br>-0.24 | 4.64/<br>-0.24 | 4.64/<br>-0.24 | 5.89/<br>-0.41 | ns    |
| $T_{DSPDCK\_D\_PREG\_MULT}/T_{DSPCKD\_D\_PREG\_MULT}$                                 | D input to P register CLK using multiplier          | 3.33/<br>-0.62 | 3.81/<br>-0.62 | 4.53/<br>-0.62 | 4.53/<br>-0.62 | 5.70/<br>-1.42 | ns    |
| $T_{DSPDCK\_ \{A, B\} \_PREG}/T_{DSPCKD\_ \{A, B\} \_PREG}$                           | A or B input to P register CLK not using multiplier | 1.47/<br>-0.24 | 1.68/<br>-0.24 | 2.00/<br>-0.24 | 2.00/<br>-0.24 | 2.37/<br>-0.41 | ns    |
| $T_{DSPDCK\_C\_PREG}/T_{DSPCKD\_C\_PREG}$   | C input to P register CLK not using multiplier      | 1.30/<br>-0.22 | 1.49/<br>-0.22 | 1.78/<br>-0.22 | 1.78/<br>-0.22 | 2.11/<br>-0.36 | ns    |
| $T_{DSPDCK\_PCIN\_PREG}/T_{DSPCKD\_PCIN\_PREG}$                                       | PCIN input to P register CLK                        | 1.12/<br>-0.13 | 1.28/<br>-0.13 | 1.52/<br>-0.13 | 1.52/<br>-0.13 | 1.81/<br>-0.21 | ns    |
| <b>Setup and Hold Times of the CE Pins</b>  |   |                |                |                |                |                |       |
| $T_{DSPDCK\_ \{CEA;CEB\} \_ \{AREG;BREG\}}/T_{DSPCKD\_ \{CEA;CEB\} \_ \{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK             | 0.30/<br>0.05  | 0.36/<br>0.06  | 0.44/<br>0.09  | 0.44/<br>0.09  | 0.55/<br>0.09  | ns    |
| $T_{DSPDCK\_CEC\_CREG}/T_{DSPCKD\_CEC\_CREG}$   | CEC input to C register CLK                         | 0.24/<br>0.08  | 0.29/<br>0.09  | 0.36/<br>0.11  | 0.36/<br>0.11  | 0.43/<br>0.11  | ns    |
| $T_{DSPDCK\_CED\_DREG}/T_{DSPCKD\_CED\_DREG}$   | CED input to D register CLK                         | 0.31/<br>-0.02 | 0.36/<br>-0.02 | 0.44/<br>-0.02 | 0.44/<br>0.02  | 0.58/<br>0.12  | ns    |
| $T_{DSPDCK\_CEM\_MREG}/T_{DSPCKD\_CEM\_MREG}$   | CEM input to M register CLK                         | 0.26/<br>0.15  | 0.29/<br>0.17  | 0.33/<br>0.20  | 0.33/<br>0.20  | 0.39/<br>0.25  | ns    |
| $T_{DSPDCK\_CEP\_PREG}/T_{DSPCKD\_CEP\_PREG}$   | CEP input to P register CLK                         | 0.31/<br>0.01  | 0.36/<br>0.01  | 0.45/<br>0.01  | 0.45/<br>0.01  | 0.54/<br>0.00  | ns    |

Table 33: DSP48E1 Switching Characteristics (Cont'd)

| Symbol  | Description   | Speed Grade   |               |               |               |               | Units |
|---|---|---------------|---------------|---------------|---------------|---------------|-------|
|   |   | 1.0V          |               |               |               | 0.9V          |       |
|   |   | -3            | -2/-2L        | -1            | -1M           | -2L           |       |
| <b>Setup and Hold Times of the RST Pins</b>   |   |               |               |               |               |               |       |
| $T_{\text{DSPDCK\_RSTA; RSTB\_AREG; BREG}} / T_{\text{DSPCKD\_RSTA; RSTB\_AREG; BREG}}$ | {RSTA, RSTB} input to {A, B} register CLK                 | 0.34/<br>0.10 | 0.39/<br>0.11 | 0.47/<br>0.13 | 0.47/<br>0.14 | 0.53/<br>0.34 | ns    |
| $T_{\text{DSPDCK\_RSTC\_CREG}} / T_{\text{DSPCKD\_RSTC\_CREG}}$                         | RSTC input to C register CLK                              | 0.06/<br>0.22 | 0.07/<br>0.24 | 0.08/<br>0.26 | 0.08/<br>0.26 | 0.08/<br>0.31 | ns    |
| $T_{\text{DSPDCK\_RSTD\_DREG}} / T_{\text{DSPCKD\_RSTD\_DREG}}$                         | RSTD input to D register CLK                              | 0.37/<br>0.06 | 0.42/<br>0.06 | 0.50/<br>0.07 | 0.50/<br>0.07 | 0.57/<br>0.07 | ns    |
| $T_{\text{DSPDCK\_RSTM\_MREG}} / T_{\text{DSPCKD\_RSTM\_MREG}}$                         | RSTM input to M register CLK                              | 0.18/<br>0.18 | 0.20/<br>0.21 | 0.23/<br>0.24 | 0.23/<br>0.24 | 0.24/<br>0.29 | ns    |
| $T_{\text{DSPDCK\_RSTP\_PREG}} / T_{\text{DSPCKD\_RSTP\_PREG}}$                         | RSTP input to P register CLK                              | 0.24/<br>0.01 | 0.26/<br>0.01 | 0.30/<br>0.01 | 0.30/<br>0.11 | 0.37/<br>0.00 | ns    |
| <b>Combinatorial Delays from Input Pins to Output Pins</b>                              |   |               |               |               |               |               |       |
| $T_{\text{DSPDO\_A\_CARRYOUT\_MULT}}$   | A input to CARRYOUT output using multiplier               | 3.21          | 3.69          | 4.39          | 4.39          | 5.60          | ns    |
| $T_{\text{DSPDO\_D\_P\_MULT}}$  | D input to P output using multiplier                      | 3.15          | 3.61          | 4.30          | 4.30          | 5.44          | ns    |
| $T_{\text{DSPDO\_A\_P}}$  | A input to P output not using multiplier                  | 1.30          | 1.48          | 1.76          | 1.76          | 2.10          | ns    |
| $T_{\text{DSPDO\_C\_P}}$  | C input to P output                                       | 1.13          | 1.30          | 1.55          | 1.55          | 1.84          | ns    |
| <b>Combinatorial Delays from Input Pins to Cascading Output Pins</b>                    |   |               |               |               |               |               |       |
| $T_{\text{DSPDO\_A; B\_ACOUT; BCOUT}}$  | {A, B} input to {ACOUT, BCOUT} output                     | 0.47          | 0.53          | 0.63          | 0.63          | 0.75          | ns    |
| $T_{\text{DSPDO\_A; B\_CARRYCASCOULT}}$   | {A, B} input to CARRYCASCOULT output using multiplier     | 3.44          | 3.94          | 4.69          | 4.69          | 5.96          | ns    |
| $T_{\text{DSPDO\_D\_CARRYCASCOULT}}$  | D input to CARRYCASCOULT output using multiplier          | 3.36          | 3.85          | 4.58          | 4.58          | 5.77          | ns    |
| $T_{\text{DSPDO\_A; B\_CARRYCASCOULT}}$   | {A, B} input to CARRYCASCOULT output not using multiplier | 1.50          | 1.72          | 2.04          | 2.04          | 2.44          | ns    |
| $T_{\text{DSPDO\_C\_CARRYCASCOULT}}$  | C input to CARRYCASCOULT output                           | 1.34          | 1.53          | 1.83          | 1.83          | 2.18          | ns    |
| <b>Combinatorial Delays from Cascading Input Pins to All Output Pins</b>                |   |               |               |               |               |               |       |
| $T_{\text{DSPDO\_ACIN\_P\_MULT}}$   | ACIN input to P output using multiplier                   | 3.09          | 3.55          | 4.24          | 4.24          | 5.42          | ns    |
| $T_{\text{DSPDO\_ACIN\_P}}$   | ACIN input to P output not using multiplier               | 1.16          | 1.33          | 1.59          | 1.59          | 2.07          | ns    |
| $T_{\text{DSPDO\_ACIN\_ACOUT}}$   | ACIN input to ACOUT output                                | 0.32          | 0.37          | 0.45          | 0.45          | 0.53          | ns    |
| $T_{\text{DSPDO\_ACIN\_CARRYCASCOULT}}$   | ACIN input to CARRYCASCOULT output using multiplier       | 3.30          | 3.79          | 4.52          | 4.52          | 5.76          | ns    |
| $T_{\text{DSPDO\_ACIN\_CARRYCASCOULT}}$   | ACIN input to CARRYCASCOULT output not using multiplier   | 1.37          | 1.57          | 1.87          | 1.87          | 2.40          | ns    |
| $T_{\text{DSPDO\_PCIN\_P}}$   | PCIN input to P output                                    | 0.94          | 1.08          | 1.29          | 1.29          | 1.54          | ns    |
| $T_{\text{DSPDO\_PCIN\_CARRYCASCOULT}}$   | PCIN input to CARRYCASCOULT output                        | 1.15          | 1.32          | 1.57          | 1.57          | 1.88          | ns    |

**Table 33: DSP48E1 Switching Characteristics (Cont'd)**

| Symbol  | Description   | Speed Grade |        |        |        |        | Units |
|---|---|-------------|--------|--------|--------|--------|-------|
|   |   | 1.0V        |        |        |        | 0.9V   |       |
|   |   | -3          | -2/-2L | -1     | -1M    | -2L    |       |
| <b>Clock to Outs from Output Register Clock to Output Pins</b>          |   |             |        |        |        |        |       |
| $T_{\text{DSPCKO\_P\_PREG}}$  | CLK PREG to P output                                    | 0.33        | 0.35   | 0.39   | 0.39   | 0.45   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_PREG}}$                                  | CLK PREG to CARRYCASCOU output                          | 0.44        | 0.50   | 0.59   | 0.59   | 0.71   | ns    |
| <b>Clock to Outs from Pipeline Register Clock to Output Pins</b>        |   |             |        |        |        |        |       |
| $T_{\text{DSPCKO\_P\_MREG}}$  | CLK MREG to P output                                    | 1.42        | 1.64   | 1.96   | 1.96   | 2.31   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_MREG}}$                                  | CLK MREG to CARRYCASCOU output                          | 1.63        | 1.87   | 2.24   | 2.24   | 2.65   | ns    |
| $T_{\text{DSPCKO\_P\_ADREG\_MULT}}$                                     | CLK ADREG to P output using multiplier                  | 2.30        | 2.63   | 3.13   | 3.13   | 3.90   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_ADREG\_MULT}}$                           | CLK ADREG to CARRYCASCOU output using multiplier        | 2.51        | 2.87   | 3.41   | 3.41   | 4.23   | ns    |
| <b>Clock to Outs from Input Register Clock to Output Pins</b>           |   |             |        |        |        |        |       |
| $T_{\text{DSPCKO\_P\_AREG\_MULT}}$                                      | CLK AREG to P output using multiplier                   | 3.34        | 3.83   | 4.55   | 4.55   | 5.80   | ns    |
| $T_{\text{DSPCKO\_P\_BREG}}$  | CLK BREG to P output not using multiplier               | 1.39        | 1.59   | 1.88   | 1.88   | 2.24   | ns    |
| $T_{\text{DSPCKO\_P\_CREG}}$  | CLK CREG to P output not using multiplier               | 1.43        | 1.64   | 1.95   | 1.95   | 2.32   | ns    |
| $T_{\text{DSPCKO\_P\_DREG\_MULT}}$                                      | CLK DREG to P output using multiplier                   | 3.32        | 3.80   | 4.51   | 4.51   | 5.74   | ns    |
| <b>Clock to Outs from Input Register Clock to Cascading Output Pins</b> |   |             |        |        |        |        |       |
| $T_{\text{DSPCKO\_}\{ACOUT; BCOUT\}\_}\{AREG; BREG\}$                   | CLK (ACOUT, BCOUT) to {A,B} register output             | 0.55        | 0.62   | 0.74   | 0.74   | 0.87   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_}\{AREG; BREG\}\_MULT}$                  | CLK (AREG, BREG) to CARRYCASCOU output using multiplier | 3.55        | 4.06   | 4.84   | 4.84   | 6.13   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_BREG}}$                                  | CLK BREG to CARRYCASCOU output not using multiplier     | 1.60        | 1.82   | 2.16   | 2.16   | 2.58   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_DREG\_MULT}}$                            | CLK DREG to CARRYCASCOU output using multiplier         | 3.52        | 4.03   | 4.79   | 4.79   | 6.07   | ns    |
| $T_{\text{DSPCKO\_CARRYCASCOU\_CREG}}$                                  | CLK CREG to CARRYCASCOU output                          | 1.64        | 1.88   | 2.23   | 2.23   | 2.65   | ns    |
| <b>Maximum Frequency</b>  |   |             |        |        |        |        |       |
| $F_{\text{MAX}}$  | With all registers used                                 | 741.84      | 650.20 | 547.95 | 547.95 | 429.37 | MHz   |
| $F_{\text{MAX\_PATDET}}$  | With pattern detector                                   | 627.35      | 549.75 | 463.61 | 463.61 | 365.90 | MHz   |
| $F_{\text{MAX\_MULT\_NOMREG}}$  | Two register multiply without MREG                      | 412.20      | 360.75 | 303.77 | 303.77 | 248.32 | MHz   |
| $F_{\text{MAX\_MULT\_NOMREG\_PATDET}}$                                  | Two register multiply without MREG with pattern detect  | 374.25      | 327.65 | 276.01 | 276.01 | 225.73 | MHz   |
| $F_{\text{MAX\_PREADD\_MULT\_NOADREG}}$                                 | Without ADREG   | 468.82      | 408.66 | 342.70 | 342.70 | 263.44 | MHz   |
| $F_{\text{MAX\_PREADD\_MULT\_NOADREG\_PATDET}}$                         | Without ADREG with pattern detect                       | 468.82      | 408.66 | 342.70 | 342.70 | 263.44 | MHz   |

Table 33: DSP48E1 Switching Characteristics (Cont'd)

| Symbol                                | Description  | Speed Grade |        |        |        |        | Units |
|---------------------------------------|--|-------------|--------|--------|--------|--------|-------|
|                                       |  | 1.0V        |        |        |        | 0.9V   |       |
|                                       |  | -3          | -2/-2L | -1     | -1M    | -2L    |       |
| F <sub>MAX_NOPIPELINEREG</sub>        | Without pipeline registers (MREG, ADREG)                     | 306.84      | 267.81 | 225.02 | 225.02 | 177.15 | MHz   |
| F <sub>MAX_NOPIPELINEREG_PATDET</sub> | Without pipeline registers (MREG, ADREG) with pattern detect | 285.23      | 249.13 | 209.38 | 209.38 | 165.32 | MHz   |

## Clock Buffers and Networks

Table 34: Global Clock Switching Characteristics (Including BUFCTRL)

| Symbol  | Description                   | Speed Grade |           |           |           |           | Units |
|---|-------------------------------|-------------|-----------|-----------|-----------|-----------|-------|
|   |                               | 1.0V        |           |           |           | 0.9V      |       |
|   |                               | -3          | -2/-2L    | -1        | -1M       | -2L       |       |
| T <sub>BCCCK_CE</sub> /T <sub>BCCCK_CE</sub> <sup>(1)</sup> | CE pins Setup/Hold            | 0.12/0.30   | 0.14/0.38 | 0.26/0.38 | 0.26/0.92 | 0.23/0.40 | ns    |
| T <sub>BCCCK_S</sub> /T <sub>BCCCK_S</sub> <sup>(1)</sup>   | S pins Setup/Hold             | 0.12/0.30   | 0.14/0.38 | 0.26/0.38 | 0.26/0.92 | 0.23/0.40 | ns    |
| T <sub>BCCCKO_O</sub> <sup>(2)</sup>                        | BUFCTRL delay from I0/I1 to O | 0.08        | 0.10      | 0.12      | 0.12      | 0.10      | ns    |
| <b>Maximum Frequency</b>                                    |                               |             |           |           |           |           |       |
| F <sub>MAX_BUFCTRL</sub>                                    | Global clock tree (BUFCTRL)   | 741.00      | 710.00    | 625.00    | 625.00    | 560.00    | MHz   |

**Notes:**

- T<sub>BCCCK\_CE</sub> and T<sub>BCCCK\_S</sub> must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFCTRL primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
- T<sub>BGCKO\_O</sub> (BUFCTRL delay from I0 to O) values are the same as T<sub>BCCCKO\_O</sub> values.

Table 35: Input/Output Clock Switching Characteristics (BUFIO)

| Symbol                   | Description                    | Speed Grade |        |        |        |        | Units |
|--------------------------|--------------------------------|-------------|--------|--------|--------|--------|-------|
|                          |                                | 1.0V        |        |        |        | 0.9V   |       |
|                          |                                | -3          | -2/-2L | -1     | -1M    | -2L    |       |
| T <sub>BIOCKO_O</sub>    | Clock to out delay from I to O | 1.04        | 1.14   | 1.32   | 1.32   | 1.48   | ns    |
| <b>Maximum Frequency</b> |                                |             |        |        |        |        |       |
| F <sub>MAX_BUFIO</sub>   | I/O clock tree (BUFIO)         | 800.00      | 800.00 | 710.00 | 710.00 | 710.00 | MHz   |

Table 36: Regional Clock Buffer Switching Characteristics (BUFR)

| Symbol                   | Description   | Speed Grade |        |      |      |      | Units |
|--------------------------|---|-------------|--------|------|------|------|-------|
|                          |   | 1.0V        |        |      |      | 0.9V |       |
|                          |   | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| T <sub>BRCKO_O</sub>     | Clock to out delay from I to O                                  | 0.60        | 0.65   | 0.77 | 0.77 | 1.06 | ns    |
| T <sub>BRCKO_O_BYP</sub> | Clock to out delay from I to O with Divide Bypass attribute set | 0.30        | 0.32   | 0.38 | 0.38 | 0.57 | ns    |
| T <sub>BRDO_O</sub>      | Propagation delay from CLR to O                                 | 0.71        | 0.75   | 0.96 | 0.96 | 0.93 | ns    |

Table 36: Regional Clock Buffer Switching Characteristics (BUFR) (Cont'd)

| Symbol                               | Description                | Speed Grade |        |        |        |        | Units |
|--------------------------------------|----------------------------|-------------|--------|--------|--------|--------|-------|
|                                      |                            | 1.0V        |        |        |        | 0.9V   |       |
|                                      |                            | -3          | -2/-2L | -1     | -1M    | -2L    |       |
| <b>Maximum Frequency</b>             |                            |             |        |        |        |        |       |
| F <sub>MAX_BUFR</sub> <sup>(1)</sup> | Regional clock tree (BUFR) | 600.00      | 540.00 | 450.00 | 450.00 | 450.00 | MHz   |

**Notes:**

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F<sub>MAX</sub> frequency.

Table 37: Horizontal Clock Buffer Switching Characteristics (BUFH)

| Symbol                                       | Description                    | Speed Grade |           |           |           |           | Units |
|--|--------------------------------|-------------|-----------|-----------|-----------|-----------|-------|
|  |                                | 1.0V        |           |           |           | 0.9V      |       |
|  |                                | -3          | -2/-2L    | -1        | -1M       | -2L       |       |
| T <sub>BHCKO_O</sub>                         | BUFH delay from I to O         | 0.10        | 0.11      | 0.13      | 0.13      | 0.12      | ns    |
| T <sub>BHCKK_CE</sub> /T <sub>BHCKC_CE</sub> | CE pin Setup and Hold          | 0.20/0.16   | 0.23/0.20 | 0.38/0.21 | 0.38/0.79 | 0.28/0.09 | ns    |
| <b>Maximum Frequency</b>                     |                                |             |           |           |           |           |       |
| F <sub>MAX_BUFH</sub>                        | Horizontal clock buffer (BUFH) | 741.00      | 710.00    | 625.00    | 625.00    | 560.00    | MHz   |

Table 38: Duty Cycle Distortion and Clock-Tree Skew

| Symbol                 | Description  | Device   | Speed Grade |        |      |      |      | Units |
|------------------------|--|----------|-------------|--------|------|------|------|-------|
|                        |  |          | 1.0V        |        |      |      | 0.9V |       |
|                        |  |          | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| T <sub>DGD_CLK</sub>   | Global Clock Tree Duty Cycle Distortion <sup>(1)</sup> | All      | 0.20        | 0.20   | 0.20 | 0.20 | 0.25 | ns    |
| T <sub>CKSKEW</sub>    | Global Clock Tree Skew <sup>(2)</sup>                  | XC7K70T  | 0.29        | 0.40   | 0.40 | N/A  | 0.47 | ns    |
|                        |  | XC7K160T | 0.42        | 0.53   | 0.57 | N/A  | 0.59 | ns    |
|                        |  | XC7K325T | 0.59        | 0.74   | 0.79 | N/A  | 0.91 | ns    |
|                        |  | XC7K355T | 0.45        | 0.57   | 0.59 | N/A  | 0.69 | ns    |
|                        |  | XC7K410T | 0.60        | 0.74   | 0.79 | N/A  | 0.91 | ns    |
|                        |  | XC7K420T | 0.60        | 0.74   | 0.79 | N/A  | 0.91 | ns    |
|                        |  | XC7K480T | 0.60        | 0.74   | 0.79 | N/A  | 0.91 | ns    |
|                        |  | XQ7K325T | N/A         | 0.74   | 0.79 | 0.79 | 0.91 | ns    |
| XQ7K410T               | N/A  | 0.74     | 0.79        | 0.79   | 0.91 | ns   |      |       |
| T <sub>DGD_BUFIO</sub> | I/O clock tree duty cycle distortion                   | All      | 0.12        | 0.12   | 0.12 | 0.12 | 0.12 | ns    |
| T <sub>BUFIOSKEW</sub> | I/O clock tree skew across one clock region            | All      | 0.02        | 0.02   | 0.02 | 0.02 | 0.03 | ns    |
| T <sub>DGD_BUFR</sub>  | Regional clock tree duty cycle distortion              | All      | 0.15        | 0.15   | 0.15 | 0.15 | 0.15 | ns    |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T<sub>CKSKEW</sub> value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

Table 39: MMCM Specification

| Symbol   | Description  | Speed Grade                             |           |           |           |           | Units   |
|--|--|---|-----------|-----------|-----------|-----------|---------|
|  |  | 1.0V                                    |           |           |           | 0.9V      |         |
|  |  | -3                                      | -2/-2L    | -1        | -1M       | -2L       |         |
| MMCM_F <sub>INMAX</sub>  | Maximum Input Clock Frequency                          | 1066.00                                 | 933.00    | 800.00    | 800.00    | 800.00    | MHz     |
| MMCM_F <sub>INMIN</sub>  | Minimum Input Clock Frequency                          | 10.00                                   | 10.00     | 10.00     | 10.00     | 10.00     | MHz     |
| MMCM_F <sub>INJITTER</sub>   | Maximum Input Clock Period Jitter                      | < 20% of clock input period or 1 ns Max |           |           |           |           |         |
| MMCM_F <sub>INDUTY</sub>   | Allowable Input Duty Cycle: 10–49 MHz                  | 25.00                                   | 25.00     | 25.00     | 25.00     | 25.00     | %       |
|  | Allowable Input Duty Cycle: 50–199 MHz                 | 30.00                                   | 30.00     | 30.00     | 30.00     | 30.00     | %       |
|  | Allowable Input Duty Cycle: 200–399 MHz                | 35.00                                   | 35.00     | 35.00     | 35.00     | 35.00     | %       |
|  | Allowable Input Duty Cycle: 400–499 MHz                | 40.00                                   | 40.00     | 40.00     | 40.00     | 40.00     | %       |
|  | Allowable Input Duty Cycle: >500 MHz                   | 45.00                                   | 45.00     | 45.00     | 45.00     | 45.00     | %       |
| MMCM_F <sub>MIN_PSCLK</sub>  | Minimum Dynamic Phase Shift Clock Frequency            | 0.01                                    | 0.01      | 0.01      | 0.01      | 0.01      | MHz     |
| MMCM_F <sub>MAX_PSCLK</sub>  | Maximum Dynamic Phase Shift Clock Frequency            | 550.00                                  | 500.00    | 450.00    | 450.00    | 450.00    | MHz     |
| MMCM_F <sub>VCOMIN</sub>   | Minimum MMCM VCO Frequency                             | 600.00                                  | 600.00    | 600.00    | 600.00    | 600.00    | MHz     |
| MMCM_F <sub>VCOMAX</sub>   | Maximum MMCM VCO Frequency                             | 1600.00                                 | 1440.00   | 1200.00   | 1200.00   | 1200.00   | MHz     |
| MMCM_F <sub>BANDWIDTH</sub>  | Low MMCM Bandwidth at Typical <sup>(1)</sup>           | 1.00                                    | 1.00      | 1.00      | 1.00      | 1.00      | MHz     |
|  | High MMCM Bandwidth at Typical <sup>(1)</sup>          | 4.00                                    | 4.00      | 4.00      | 4.00      | 4.00      | MHz     |
| MMCM_T <sub>STATPHAOFFSET</sub>  | Static Phase Offset of the MMCM Outputs <sup>(2)</sup> | 0.12                                    | 0.12      | 0.12      | 0.12      | 0.12      | ns      |
| MMCM_T <sub>OUTJITTER</sub>  | MMCM Output Jitter                                     | Note 3                                  |           |           |           |           |         |
| MMCM_T <sub>OUTDUTY</sub>  | MMCM Output Clock Duty Cycle Precision <sup>(4)</sup>  | 0.20                                    | 0.20      | 0.20      | 0.20      | 0.25      | ns      |
| MMCM_T <sub>LOCKMAX</sub>  | MMCM Maximum Lock Time                                 | 100.00                                  | 100.00    | 100.00    | 100.00    | 100.00    | µs      |
| MMCM_F <sub>OUTMAX</sub>   | MMCM Maximum Output Frequency                          | 1066.00                                 | 933.00    | 800.00    | 800.00    | 800.00    | MHz     |
| MMCM_F <sub>OUTMIN</sub>   | MMCM Minimum Output Frequency <sup>(5)(6)</sup>        | 4.69                                    | 4.69      | 4.69      | 4.69      | 4.69      | MHz     |
| MMCM_T <sub>EXTFDVAR</sub>   | External Clock Feedback Variation                      | < 20% of clock input period or 1 ns Max |           |           |           |           |         |
| MMCM_RST <sub>MINPULSE</sub>   | Minimum Reset Pulse Width                              | 5.00                                    | 5.00      | 5.00      | 5.00      | 5.00      | ns      |
| MMCM_F <sub>PFDMAX</sub>   | Maximum Frequency at the Phase Frequency Detector      | 550.00                                  | 500.00    | 450.00    | 450.00    | 450.00    | MHz     |
| MMCM_F <sub>PFDMIN</sub>   | Minimum Frequency at the Phase Frequency Detector      | 10.00                                   | 10.00     | 10.00     | 10.00     | 10.00     | MHz     |
| MMCM_T <sub>FBDELAY</sub>  | Maximum Delay in the Feedback Path                     | 3 ns Max or one CLKIN cycle             |           |           |           |           |         |
| <b>MMCM Switching Characteristics Setup and Hold</b>                     |  |   |           |           |           |           |         |
| T <sub>MMCMDCK_PSEN</sub> /<br>T <sub>MMCMCKD_PSEN</sub>                 | Setup and Hold of Phase Shift Enable                   | 1.04/0.00                               | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns      |
| T <sub>MMCMDCK_PSINCDEC</sub> /<br>T <sub>MMCMCKD_PSINCDEC</sub>         | Setup and Hold of Phase Shift Increment/Decrement      | 1.04/0.00                               | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns      |
| T <sub>MMCMCKO_PSDONE</sub>  | Phase Shift Clock-to-Out of PSDONE                     | 0.59                                    | 0.68      | 0.81      | 0.81      | 0.78      | ns      |
| <b>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</b> |  |   |           |           |           |           |         |
| T <sub>MMCMDCK_DADDR</sub> /<br>T <sub>MMCMCKD_DADDR</sub>               | DADDR Setup/Hold                                       | 1.25/0.15                               | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |



Table 39: MMCM Specification (Cont'd)

| Symbol                              | Description        | Speed Grade |           |           |           |           | Units    |
|-------------------------------------|--------------------|-------------|-----------|-----------|-----------|-----------|----------|
|                                     |                    | 1.0V        |           |           |           | 0.9V      |          |
|                                     |                    | -3          | -2/-2L    | -1        | -1M       | -2L       |          |
| $T_{MMCMCKD\_DI}/T_{MMCMCKD\_DI}$   | DI Setup/Hold      | 1.25/0.15   | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| $T_{MMCMCKD\_DEN}/T_{MMCMCKD\_DEN}$ | DEN Setup/Hold     | 1.76/0.00   | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min  |
| $T_{MMCMCKD\_DWE}/T_{MMCMCKD\_DWE}$ | DWE Setup/Hold     | 1.25/0.15   | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| $T_{MMCMCKO\_DRDY}$                 | CLK to out of DRDY | 0.65        | 0.72      | 0.99      | 0.99      | 0.70      | ns, Max  |
| $F_{DCK}$                           | DCLK frequency     | 200.00      | 200.00    | 200.00    | 200.00    | 100.00    | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See [www.xilinx.com/products/intellectual-property/clocking\\_wizard.htm](http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm).
4. Includes global clock buffer.
5. Calculated as  $F_{VCO}/128$  assuming output duty cycle is 50%.
6. When  $CLKOUT4\_CASCADE = TRUE$ ,  $MMCM\_F_{OUTMIN}$  is 0.036 MHz.

**PLL Switching Characteristics**

Table 40: PLL Specification

| Symbol                   | Description   | Speed Grade                             |         |         |         |         | Units |
|--------------------------|---|---|---------|---------|---------|---------|-------|
|                          |   | 1.0V                                    |         |         |         | 0.9V    |       |
|                          |   | -3                                      | -2/-2L  | -1      | -1M     | -2L     |       |
| $PLL\_F_{INMAX}$         | Maximum Input Clock Frequency                         | 1066.00                                 | 933.00  | 800.00  | 800.00  | 800.00  | MHz   |
| $PLL\_F_{INMIN}$         | Minimum Input Clock Frequency                         | 19.00                                   | 19.00   | 19.00   | 19.00   | 19.00   | MHz   |
| $PLL\_F_{INJITTER}$      | Maximum Input Clock Period Jitter                     | < 20% of clock input period or 1 ns Max |         |         |         |         |       |
| $PLL\_F_{INDUTY}$        | Allowable Input Duty Cycle: 19–49 MHz                 | 25.00                                   | 25.00   | 25.00   | 25.00   | 25.00   | %     |
|                          | Allowable Input Duty Cycle: 50–199 MHz                | 30.00                                   | 30.00   | 30.00   | 30.00   | 30.00   | %     |
|                          | Allowable Input Duty Cycle: 200–399 MHz               | 35.00                                   | 35.00   | 35.00   | 35.00   | 35.00   | %     |
|                          | Allowable Input Duty Cycle: 400–499 MHz               | 40.00                                   | 40.00   | 40.00   | 40.00   | 40.00   | %     |
|                          | Allowable Input Duty Cycle: >500 MHz                  | 45.00                                   | 45.00   | 45.00   | 45.00   | 45.00   | %     |
| $PLL\_F_{VCOMIN}$        | Minimum PLL VCO Frequency                             | 800.00                                  | 800.00  | 800.00  | 800.00  | 800.00  | MHz   |
| $PLL\_F_{VCOMAX}$        | Maximum PLL VCO Frequency                             | 2133.00                                 | 1866.00 | 1600.00 | 1600.00 | 1600.00 | MHz   |
| $PLL\_F_{BANDWIDTH}$     | Low PLL Bandwidth at Typical <sup>(1)</sup>           | 1.00                                    | 1.00    | 1.00    | 1.00    | 1.00    | MHz   |
|                          | High PLL Bandwidth at Typical <sup>(1)</sup>          | 4.00                                    | 4.00    | 4.00    | 4.00    | 4.00    | MHz   |
| $PLL\_T_{STATPHAOFFSET}$ | Static Phase Offset of the PLL Outputs <sup>(2)</sup> | 0.12                                    | 0.12    | 0.12    | 0.12    | 0.12    | ns    |
| $PLL\_T_{OUTJITTER}$     | PLL Output Jitter                                     | Note 3                                  |         |         |         |         |       |
| $PLL\_T_{OUTDUTY}$       | PLL Output Clock Duty Cycle Precision <sup>(4)</sup>  | 0.20                                    | 0.20    | 0.20    | 0.20    | 0.25    | ns    |
| $PLL\_T_{LOCKMAX}$       | PLL Maximum Lock Time                                 | 100                                     | 100     | 100     | 100     | 100     | μs    |
| $PLL\_F_{OUTMAX}$        | PLL Maximum Output Frequency                          | 1066.00                                 | 933.00  | 800.00  | 800.00  | 800.00  | MHz   |
| $PLL\_F_{OUTMIN}$        | PLL Minimum Output Frequency <sup>(5)</sup>           | 6.25                                    | 6.25    | 6.25    | 6.25    | 6.25    | MHz   |
| $PLL\_T_{EXTFDVAR}$      | External Clock Feedback Variation                     | < 20% of clock input period or 1 ns Max |         |         |         |         |       |
| $PLL\_RST_{MINPULSE}$    | Minimum Reset Pulse Width                             | 5.00                                    | 5.00    | 5.00    | 5.00    | 5.00    | ns    |

Table 40: PLL Specification (Cont'd)

| Symbol  | Description                                       | Speed Grade                 |           |           |           |           | Units    |
|---|---|-----------------------------|-----------|-----------|-----------|-----------|----------|
|   |   | 1.0V                        |           |           |           | 0.9V      |          |
|   |   | -3                          | -2/-2L    | -1        | -1M       | -2L       |          |
| PLL_FPFDMAX   | Maximum Frequency at the Phase Frequency Detector | 550.00                      | 500.00    | 450.00    | 450.00    | 450.00    | MHz      |
| PLL_FPFDMIN   | Minimum Frequency at the Phase Frequency Detector | 19.00                       | 19.00     | 19.00     | 19.00     | 19.00     | MHz      |
| PLL_TFBDELAY  | Maximum Delay in the Feedback Path                | 3 ns Max or one CLKIN cycle |           |           |           |           |          |
| <b>Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK</b> |   |                             |           |           |           |           |          |
| T <sub>PLLCKC_DADDR</sub> /<br>T <sub>PLLCKC_DADDR</sub>                | Setup and hold of D address                       | 1.25/0.15                   | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| T <sub>PLLCKC_DI</sub> /<br>T <sub>PLLCKC_DI</sub>                      | Setup and hold of D input                         | 1.25/0.15                   | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| T <sub>PLLCKC_DEN</sub> /<br>T <sub>PLLCKC_DEN</sub>                    | Setup and hold of D enable                        | 1.76/0.00                   | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min  |
| T <sub>PLLCKC_DWE</sub> /<br>T <sub>PLLCKC_DWE</sub>                    | Setup and hold of D write enable                  | 1.25/0.15                   | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| T <sub>PLLCKO_DRDY</sub>  | CLK to out of DRDY                                | 0.65                        | 0.72      | 0.99      | 0.99      | 0.70      | ns, Max  |
| F <sub>DCK</sub>  | DCLK frequency                                    | 200.00                      | 200.00    | 200.00    | 200.00    | 100.00    | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.  
See [www.xilinx.com/products/intellectual-property/clocking\\_wizard.htm](http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm).
4. Includes global clock buffer.
5. Calculated as  $F_{VCO}/128$  assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

| Symbol  | Description   | Device   | Speed Grade |        |      |      |      | Units |
|---|---|----------|-------------|--------|------|------|------|-------|
|   |   |          | 1.0V        |        |      |      | 0.9V |       |
|   |   |          | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL. |   |          |             |        |      |      |      |       |
| T <sub>ICKOFF</sub>   | Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region) | XC7K70T  | 4.98        | 5.49   | 6.17 | N/A  | 7.04 | ns    |
|   |   | XC7K160T | 5.23        | 5.77   | 6.48 | N/A  | 7.38 | ns    |
|   |   | XC7K325T | 5.72        | 6.31   | 7.09 | N/A  | 8.07 | ns    |
|   |   | XC7K355T | 5.34        | 5.87   | 6.57 | N/A  | 7.51 | ns    |
|   |   | XC7K410T | 5.84        | 6.44   | 7.22 | N/A  | 8.21 | ns    |
|   |   | XC7K420T | 5.50        | 6.04   | 6.77 | N/A  | 7.73 | ns    |
|   |   | XC7K480T | 5.50        | 6.04   | 6.77 | N/A  | 7.73 | ns    |
|   |   | XQ7K325T | N/A         | 6.31   | 7.09 | 7.09 | 8.07 | ns    |
|   |   | XQ7K410T | N/A         | 6.44   | 7.22 | 7.22 | 8.21 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 42: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

| Symbol  | Description  | Device   | Speed Grade |        |      |      |      | Units |
|---|--|----------|-------------|--------|------|------|------|-------|
|   |  |          | 1.0V        |        |      |      | 0.9V |       |
|   |  |          | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL. |  |          |             |        |      |      |      |       |
| T <sub>ICKOFFAR</sub>   | Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region) | XC7K70T  | 5.29        | 5.83   | 6.55 | N/A  | 7.47 | ns    |
|   |  | XC7K160T | 5.84        | 6.45   | 7.24 | N/A  | 8.24 | ns    |
|   |  | XC7K325T | 6.33        | 6.99   | 7.84 | N/A  | 8.92 | ns    |
|   |  | XC7K355T | 5.95        | 6.55   | 7.32 | N/A  | 8.36 | ns    |
|   |  | XC7K410T | 6.45        | 7.12   | 7.97 | N/A  | 9.07 | ns    |
|   |  | XC7K420T | 6.41        | 7.06   | 7.90 | N/A  | 9.01 | ns    |
|   |  | XC7K480T | 6.41        | 7.06   | 7.90 | N/A  | 9.01 | ns    |
|   |  | XQ7K325T | N/A         | 6.99   | 7.84 | 7.84 | 8.92 | ns    |
|   |  | XQ7K410T | N/A         | 7.12   | 7.97 | 7.97 | 9.07 | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 43: Clock-Capable Clock Input to Output Delay With MMCM

| Symbol  | Description                                   | Device   | Speed Grade |        |      |      |      | Units |
|---|---|----------|-------------|--------|------|------|------|-------|
|   |   |          | 1.0V        |        |      |      | 0.9V |       |
|   |   |          | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM. |   |          |             |        |      |      |      |       |
| T <sub>ICKOFMMCMCC</sub>  | Clock-capable clock input and OUTFF with MMCM | XC7K70T  | 0.95        | 0.95   | 0.95 | N/A  | 1.74 | ns    |
|   |   | XC7K160T | 0.96        | 0.96   | 0.96 | N/A  | 1.78 | ns    |
|   |   | XC7K325T | 1.00        | 1.00   | 1.00 | N/A  | 1.82 | ns    |
|   |   | XC7K355T | 1.00        | 1.00   | 1.00 | N/A  | 1.78 | ns    |
|   |   | XC7K410T | 1.00        | 1.00   | 1.00 | N/A  | 1.82 | ns    |
|   |   | XC7K420T | 1.07        | 1.07   | 1.07 | N/A  | 1.82 | ns    |
|   |   | XC7K480T | 1.07        | 1.07   | 1.07 | N/A  | 1.82 | ns    |
|   |   | XQ7K325T | N/A         | 1.00   | 1.00 | 1.00 | 1.82 | ns    |
|   |   | XQ7K410T | N/A         | 1.00   | 1.00 | 1.00 | 1.82 | ns    |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 44: Clock-Capable Clock Input to Output Delay With PLL

| Symbol   | Description                                  | Device   | Speed Grade |        |      |      |      | Units |
|--|--|----------|-------------|--------|------|------|------|-------|
|  |  |          | 1.0V        |        |      |      | 0.9V |       |
|  |  |          | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with PLL. |  |          |             |        |      |      |      |       |
| T <sub>ICKOFPLLCC</sub>  | Clock-capable clock input and OUTFF with PLL | XC7K70T  | 0.84        | 0.84   | 0.84 | N/A  | 1.45 | ns    |
|  |  | XC7K160T | 0.89        | 0.89   | 0.89 | N/A  | 1.54 | ns    |
|  |  | XC7K325T | 0.89        | 0.89   | 0.89 | N/A  | 1.54 | ns    |
|  |  | XC7K355T | 0.89        | 0.89   | 0.89 | N/A  | 1.50 | ns    |
|  |  | XC7K410T | 0.89        | 0.89   | 0.89 | N/A  | 1.54 | ns    |
|  |  | XC7K420T | 0.96        | 0.96   | 0.96 | N/A  | 1.54 | ns    |
|  |  | XC7K480T | 0.96        | 0.96   | 0.96 | N/A  | 1.54 | ns    |
|  |  | XQ7K325T | N/A         | 0.89   | 0.89 | 0.89 | 1.54 | ns    |
|  |  | XQ7K410T | N/A         | 0.89   | 0.89 | 0.89 | 1.54 | ns    |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 45: Pin-to-Pin, Clock-to-Out using BUFIO

| Symbol   | Description                                | Speed Grade |        |      |      |      | Units |
|--|--|-------------|--------|------|------|------|-------|
|  |  | 1.0V        |        |      |      | 0.9V |       |
|  |  | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO. |  |             |        |      |      |      |       |
| T <sub>ICKOFCS</sub>   | Clock-to-Out of I/O clock for HR I/O banks | 4.93        | 5.52   | 6.20 | 6.20 | 6.97 | ns    |
|  | Clock-to-Out of I/O clock for HP I/O banks | 4.85        | 5.44   | 6.11 | 6.11 | 6.90 | ns    |

## Device Pin-to-Pin Input Parameter Guidelines

Table 46: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD\_DELAY on HR I/O Banks

| Symbol  | Description   | Device   | Speed Grade |            |            |            |            | Units |
|---|---|----------|-------------|------------|------------|------------|------------|-------|
|   |   |          | 1.0V        |            |            |            | 0.9V       |       |
|   |   |          | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. <sup>(1)</sup> |   |          |             |            |            |            |            |       |
| T <sub>PSFD</sub> /T <sub>PHFD</sub>  | Full Delay (Legacy Delay or Default Delay)<br>Global Clock Input and IFF <sup>(2)</sup><br>without MMCM/PLL with<br>ZHOLD_DELAY on HR I/O Banks | XC7K70T  | 2.83/-0.29  | 2.95/-0.29 | 3.15/-0.29 | N/A        | 4.96/-0.33 | ns    |
|   |   | XC7K160T | 3.17/-0.35  | 3.29/-0.35 | 3.55/-0.35 | N/A        | 5.54/-0.49 | ns    |
|   |   | XC7K325T | 2.83/-0.06  | 2.94/-0.06 | 3.15/-0.06 | N/A        | 5.18/-0.14 | ns    |
|   |   | XC7K355T | 3.26/-0.32  | 3.41/-0.32 | 3.67/-0.32 | N/A        | 5.84/-0.49 | ns    |
|   |   | XC7K410T | 3.43/-0.34  | 3.59/-0.34 | 3.88/-0.34 | N/A        | 6.21/-0.54 | ns    |
|   |   | XC7K420T | 3.37/-0.27  | 3.48/-0.27 | 3.76/-0.27 | N/A        | 6.00/-0.52 | ns    |
|   |   | XC7K480T | 3.37/-0.27  | 3.48/-0.27 | 3.76/-0.27 | N/A        | 6.00/-0.52 | ns    |
|   |   | XQ7K325T | N/A         | 2.94/-0.06 | 3.15/-0.06 | 3.15/-0.06 | 5.18/-0.14 | ns    |
|   |   | XQ7K410T | N/A         | 3.59/-0.34 | 3.88/-0.34 | 3.88/-0.34 | 6.21/-0.54 | ns    |

**Notes:**

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch.

Table 47: Clock-Capable Clock Input Setup and Hold With MMCM

| Symbol  | Description  | Device   | Speed Grade |            |            |            |            | Units |
|---|--|----------|-------------|------------|------------|------------|------------|-------|
|   |  |          | 1.0V        |            |            |            | 0.9V       |       |
|   |  |          | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. <sup>(1)</sup> |  |          |             |            |            |            |            |       |
| T <sub>PSMMCMCC</sub> /<br>T <sub>PHMMCMCC</sub>  | No Delay clock-capable clock input<br>and IFF <sup>(2)</sup> with MMCM | XC7K70T  | 2.39/-0.22  | 2.65/-0.22 | 2.94/-0.22 | N/A        | 2.21/-0.44 | ns    |
|   |  | XC7K160T | 2.49/-0.20  | 2.77/-0.20 | 3.07/-0.20 | N/A        | 2.38/-0.47 | ns    |
|   |  | XC7K325T | 2.55/-0.16  | 2.85/-0.16 | 3.14/-0.16 | N/A        | 2.60/-0.47 | ns    |
|   |  | XC7K355T | 2.43/-0.16  | 2.73/-0.16 | 3.00/-0.16 | N/A        | 2.47/-0.43 | ns    |
|   |  | XC7K410T | 2.55/-0.16  | 2.84/-0.16 | 3.14/-0.16 | N/A        | 2.58/-0.47 | ns    |
|   |  | XC7K420T | 2.47/-0.09  | 2.73/-0.09 | 3.02/-0.09 | N/A        | 2.40/-0.41 | ns    |
|   |  | XC7K480T | 2.47/-0.09  | 2.73/-0.09 | 3.02/-0.09 | N/A        | 2.40/-0.41 | ns    |
|   |  | XQ7K325T | N/A         | 2.85/-0.16 | 3.14/-0.16 | 3.14/-0.16 | 2.60/-0.47 | ns    |
|   |  | XQ7K410T | N/A         | 2.84/-0.16 | 3.14/-0.16 | 3.14/-0.16 | 2.58/-0.47 | ns    |

**Notes:**

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Clock-Capable Clock Input Setup and Hold With PLL

| Symbol   | Description  | Device   | Speed Grade |            |            |            |            | Units |
|--|--|----------|-------------|------------|------------|------------|------------|-------|
|  |  |          | 1.0V        |            |            |            | 0.9V       |       |
|  |  |          | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. <sup>(1)</sup> |  |          |             |            |            |            |            |       |
| T <sub>PSPLLCC</sub> /<br>T <sub>PHPLLCC</sub>   | No Delay clock-capable clock input and IFF <sup>(2)</sup> with PLL | XC7K70T  | 2.75/-0.32  | 3.04/-0.32 | 3.33/-0.32 | N/A        | 2.42/-0.54 | ns    |
|  |  | XC7K160T | 2.85/-0.31  | 3.16/-0.31 | 3.46/-0.31 | N/A        | 2.59/-0.56 | ns    |
|  |  | XC7K325T | 2.91/-0.27  | 3.24/-0.27 | 3.54/-0.27 | N/A        | 2.80/-0.56 | ns    |
|  |  | XC7K355T | 2.79/-0.27  | 3.12/-0.27 | 3.40/-0.27 | N/A        | 2.67/-0.52 | ns    |
|  |  | XC7K410T | 2.91/-0.27  | 3.24/-0.27 | 3.53/-0.27 | N/A        | 2.78/-0.56 | ns    |
|  |  | XC7K420T | 2.83/-0.20  | 3.12/-0.20 | 3.41/-0.20 | N/A        | 2.61/-0.50 | ns    |
|  |  | XC7K480T | 2.83/-0.20  | 3.12/-0.20 | 3.41/-0.20 | N/A        | 2.61/-0.50 | ns    |
|  |  | XQ7K325T | N/A         | 3.24/-0.27 | 3.54/-0.27 | 3.54/-0.27 | 2.80/-0.56 | ns    |
|  |  | XQ7K410T | N/A         | 3.24/-0.27 | 3.53/-0.27 | 3.53/-0.27 | 2.78/-0.56 | ns    |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 49: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

| Symbol   | Description                              | Speed Grade |            |            |            |            | Units |
|--|--|-------------|------------|------------|------------|------------|-------|
|  |  | 1.0V        |            |            |            | 0.9V       |       |
|  |  | -3          | -2/-2L     | -1         | -1M        | -2L        |       |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. |  |             |            |            |            |            |       |
| T <sub>PSCS</sub> /T <sub>PHCS</sub>   | Setup/Hold of I/O clock for HR I/O banks | -0.36/1.36  | -0.36/1.50 | -0.36/1.70 | -0.36/1.70 | -0.44/1.87 | ns    |
|  | Setup/Hold of I/O clock for HP I/O banks | -0.34/1.39  | -0.34/1.53 | -0.34/1.73 | -0.34/1.73 | -0.44/1.87 | ns    |

Table 50: Sample Window

| Symbol                  | Description  | Speed Grade |        |      |      |      | Units |
|-------------------------|--|-------------|--------|------|------|------|-------|
|                         |  | 1.0V        |        |      |      | 0.9V |       |
|                         |  | -3          | -2/-2L | -1   | -1M  | -2L  |       |
| T <sub>SAMP</sub>       | Sampling Error at Receiver Pins <sup>(1)</sup>             | 0.51        | 0.56   | 0.61 | 0.61 | 0.56 | ns    |
| T <sub>SAMP_BUFIO</sub> | Sampling Error at Receiver Pins using BUFIO <sup>(2)</sup> | 0.30        | 0.35   | 0.40 | 0.40 | 0.35 | ns    |

Notes:

1. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 MMCM jitter
  - MMCM accuracy (phase offset)
  - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

*Table 51: Package Skew*

| Symbol               | Description                 | Device   | Package | Value  | Units |    |
|----------------------|-----------------------------|----------|---------|--------|-------|----|
| T <sub>PKGSKEW</sub> | Package Skew <sup>(1)</sup> | XC7K70T  | FBG484  | 108    | ps    |    |
|                      |                             |          | FBG676  | 135    | ps    |    |
|                      |                             | XC7K160T | FBG484  | 118    | ps    |    |
|                      |                             |          | FBG676  | 136    | ps    |    |
|                      |                             |          | FFG676  | 161    | ps    |    |
|                      |                             | XC7K325T | FBG676  | 146    | ps    |    |
|                      |                             |          | FFG676  | 154    | ps    |    |
|                      |                             |          | FBG900  | 163    | ps    |    |
|                      |                             |          | FFG900  | 161    | ps    |    |
|                      |                             | XC7K355T |         | FFG901 | 149   | ps |
|                      |                             | XC7K410T | FBG676  | 165    | ps    |    |
|                      |                             |          | FFG676  | 168    | ps    |    |
|                      |                             |          | FBG900  | 151    | ps    |    |
|                      |                             |          | FFG900  | 146    | ps    |    |
|                      |                             | XC7K420T | FFG901  | 149    | ps    |    |
|                      |                             |          | FFG1156 | 145    | ps    |    |
|                      |                             | XC7K480T | FFG901  | 149    | ps    |    |
|                      |                             |          | FFG1156 | 145    | ps    |    |
|                      |                             | XQ7K325T | RF676   | 154    | ps    |    |
|                      |                             |          | RF900   | 161    | ps    |    |
| XQ7K410T             | RF676                       | 168      | ps      |        |       |    |
|                      | RF900                       | 146      | ps      |        |       |    |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# GTX Transceiver Specifications

## GTX Transceiver DC Input and Output Levels

Table 52 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further details.

Table 52: GTX Transceiver DC Specifications

| Symbol               | DC Parameter  | Conditions   | Min                          | Typ                      | Max                  | Units |
|----------------------|---|--|------------------------------|--------------------------|----------------------|-------|
| DV <sub>PPOUT</sub>  | Differential peak-to-peak output voltage <sup>(1)</sup>       | Transmitter output swing is set to maximum setting | –                            | –                        | 1000                 | mV    |
| V <sub>CMOUTDC</sub> | DC common mode output voltage.                                | Equation based                                     | $V_{MGTAVTT} - DV_{PPOUT}/4$ |                          |                      | mV    |
| R <sub>OUT</sub>     | Differential output resistance                                |  | –                            | 100                      | –                    | Ω     |
| T <sub>OSKEW</sub>   | Transmitter output pair (TXP and TXN) intra-pair skew         |  | –                            | 2                        | 12                   | ps    |
| DV <sub>PPIN</sub>   | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s                                      | 150                          | –                        | 1250                 | mV    |
|                      |   | 6.6 Gb/s to 10.3125 Gb/s                           | 150                          | –                        | 1250                 | mV    |
|                      |   | ≤ 6.6 Gb/s   | 150                          | –                        | 2000                 | mV    |
| V <sub>IN</sub>      | Absolute input voltage  | DC coupled V <sub>MGTAVTT</sub> = 1.2V             | –200                         | –                        | V <sub>MGTAVTT</sub> | mV    |
| V <sub>CMIN</sub>    | Common mode input voltage                                     | DC coupled V <sub>MGTAVTT</sub> = 1.2V             | –                            | 2/3 V <sub>MGTAVTT</sub> | –                    | mV    |
| R <sub>IN</sub>      | Differential input resistance                                 |  | –                            | 100                      | –                    | Ω     |
| C <sub>EXT</sub>     | Recommended external AC coupling capacitor <sup>(2)</sup>     |  | –                            | 100                      | –                    | nF    |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

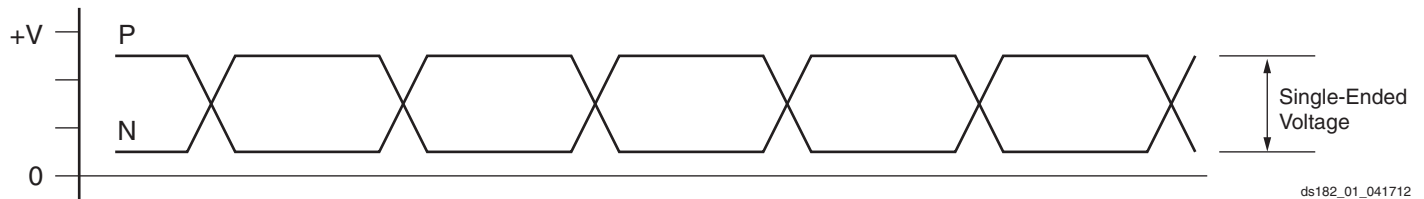


Figure 1: Single-Ended Peak-to-Peak Voltage

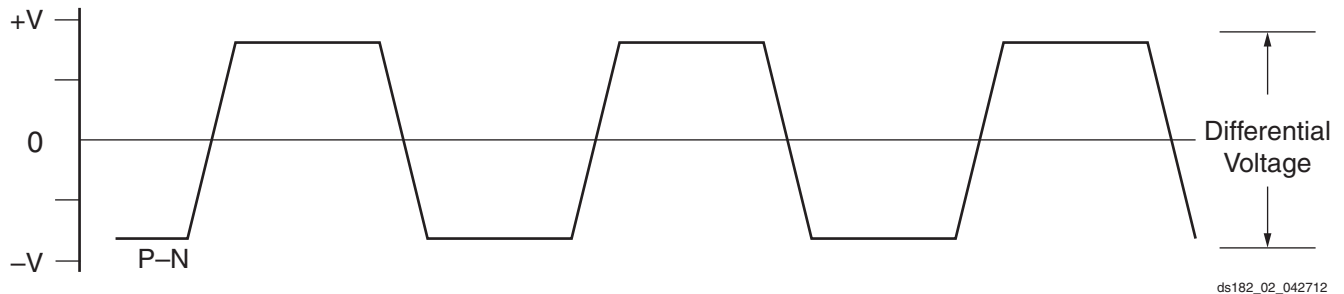


Figure 2: Differential Peak-to-Peak Voltage



Table 53 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further details.

Table 53: GTX Transceiver Clock DC Input Level Specification

| Symbol             | DC Parameter                            | Min | Typ | Max  | Units |
|--------------------|---|-----|-----|------|-------|
| V <sub>IDIFF</sub> | Differential peak-to-peak input voltage | 250 | –   | 2000 | mV    |
| R <sub>IN</sub>    | Differential input resistance           | –   | 100 | –    | Ω     |
| C <sub>EXT</sub>   | Required external AC coupling capacitor | –   | 100 | –    | nF    |

### GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further information.

Table 54: GTX Transceiver Performance

| Symbol                             | Description                            | Output Divider | Speed Grade    |          |                   |          |                       |          |                    |          | Units |
|------------------------------------|--|----------------|----------------|----------|-------------------|----------|-----------------------|----------|--------------------|----------|-------|
|                                    |  |                | 1.0V           |          |                   |          | 0.9V                  |          |                    |          |       |
|                                    |  |                | -3             |          | -2/-2L            |          | -1/-1M <sup>(1)</sup> |          | -2L <sup>(2)</sup> |          |       |
|                                    |  |                | Package Type   |          |                   |          |                       |          |                    |          |       |
| FF                                 |  | FB             |                | FF RF    |                   | FB       |                       | FF RF    |                    | FB       |       |
| F <sub>GTXMAX</sub> <sup>(3)</sup> | Maximum GTX transceiver data rate      |                | 12.5           | 6.6      | 10.3125           | 6.6      | 8.0                   | 6.6      | 6.6                | 6.6      | Gb/s  |
| F <sub>GTXMIN</sub> <sup>(3)</sup> | Minimum GTX transceiver data rate      |                | 0.500          | 0.500    | 0.500             | 0.500    | 0.500                 | 0.500    | 0.500              | 0.500    | Gb/s  |
| F <sub>GTXCRANGE</sub>             | CPLL line rate range                   | 1              | 3.2–6.6        |          |                   |          |                       |          |                    |          | Gb/s  |
|                                    |  | 2              | 1.6–3.3        |          |                   |          |                       |          |                    |          | Gb/s  |
|                                    |  | 4              | 0.8–1.65       |          |                   |          |                       |          |                    |          | Gb/s  |
|                                    |  | 8              | 0.5–0.825      |          |                   |          |                       |          |                    |          | Gb/s  |
|                                    |  | 16             | N/A            |          |                   |          |                       |          |                    |          | Gb/s  |
| F <sub>GTXQRANGE1</sub>            | QPLL line rate range 1                 | 1              | 5.93–8.0       | 5.93–6.6 | 5.93–8.0          | 5.93–6.6 | 5.93–8.0              | 5.93–6.6 | 5.93–6.6           | 5.93–6.6 | Gb/s  |
|                                    |  | 2              | 2.965–4.0      |          | 2.965–4.0         |          | 2.965–4.0             |          | 2.965–3.3          |          | Gb/s  |
|                                    |  | 4              | 1.4825–2.0     |          | 1.4825–2.0        |          | 1.4825–2.0            |          | 1.4825–1.65        |          | Gb/s  |
|                                    |  | 8              | 0.74125–1.0    |          | 0.74125–1.0       |          | 0.74125–1.0           |          | 0.74125–0.825      |          | Gb/s  |
|                                    |  | 16             | N/A            |          | N/A               |          | N/A                   |          | N/A                |          | Gb/s  |
| F <sub>GTXQRANGE2</sub>            | QPLL line rate range 2 <sup>(4)</sup>  | 1              | 9.8–12.5       | N/A      | 9.8–10.3125       | N/A      | N/A                   | N/A      | N/A                | N/A      | Gb/s  |
|                                    |  | 2              | 4.9–6.25       |          | 4.9–5.15625       |          | N/A                   |          | N/A                |          | Gb/s  |
|                                    |  | 4              | 2.45–3.125     |          | 2.45–2.578125     |          | N/A                   |          | N/A                |          | Gb/s  |
|                                    |  | 8              | 1.225–1.5625   |          | 1.225–1.2890625   |          | N/A                   |          | N/A                |          | Gb/s  |
|                                    |  | 16             | 0.6125–0.78125 |          | 0.6125–0.64453125 |          | N/A                   |          | N/A                |          | Gb/s  |
| F <sub>GCPLL</sub> RANGE           | GTX transceiver CPLL frequency range   |                | 1.6–3.3        |          | 1.6–3.3           |          | 1.6–3.3               |          | 1.6–3.3            |          | GHz   |
| F <sub>GQPLL</sub> RANGE1          | GTX transceiver QPLL frequency range 1 |                | 5.93–8.0       |          | 5.93–8.0          |          | 5.93–8.0              |          | 5.93–6.6           |          | GHz   |

Table 54: GTX Transceiver Performance (Cont'd)

| Symbol                    | Description                            | Output Divider | Speed Grade  |       |             |    |                       |       |                    |    | Units |
|---------------------------|--|----------------|--------------|-------|-------------|----|-----------------------|-------|--------------------|----|-------|
|                           |  |                | 1.0V         |       |             |    | 0.9V                  |       |                    |    |       |
|                           |  |                | -3           |       | -2/-2L      |    | -1/-1M <sup>(1)</sup> |       | -2L <sup>(2)</sup> |    |       |
|                           |  |                | Package Type |       |             |    |                       |       |                    |    |       |
| FF                        |  | FB             |              | FF RF |             | FB |                       | FF RF |                    | FB |       |
| F <sub>GQPLL</sub> RANGE2 | GTX transceiver QPLL frequency range 2 |                | 9.8–12.5     |       | 9.8–10.3125 |    | N/A                   |       | N/A                |    | GHz   |

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 55: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol                 | Description                 | Speed Grade |        |        |        | Units |
|------------------------|-----------------------------|-------------|--------|--------|--------|-------|
|                        |                             | 1.0V        |        | 0.9V   |        |       |
|                        |                             | -3          | -2/-2L | -1/-1M | -2L    |       |
| F <sub>GTXDRPCLK</sub> | GTXDRPCLK maximum frequency | 175.01      | 175.01 | 156.25 | 125.00 | MHz   |

Table 56: GTX Transceiver Reference Clock Switching Characteristics

| Symbol             | Description                     | Conditions             | All Speed Grades |     |     | Units |
|--------------------|---------------------------------|------------------------|------------------|-----|-----|-------|
|                    |                                 |                        | Min              | Typ | Max |       |
| F <sub>GCLK</sub>  | Reference clock frequency range | -3 speed grade         | 60               | –   | 700 | MHz   |
|                    |                                 | All other speed grades | 60               | –   | 670 | MHz   |
| T <sub>RCLK</sub>  | Reference clock rise time       | 20% – 80%              | –                | 200 | –   | ps    |
| T <sub>FCLK</sub>  | Reference clock fall time       | 80% – 20%              | –                | 200 | –   | ps    |
| T <sub>DCREF</sub> | Reference clock duty cycle      | Transceiver PLL only   | 40               | 50  | 60  | %     |

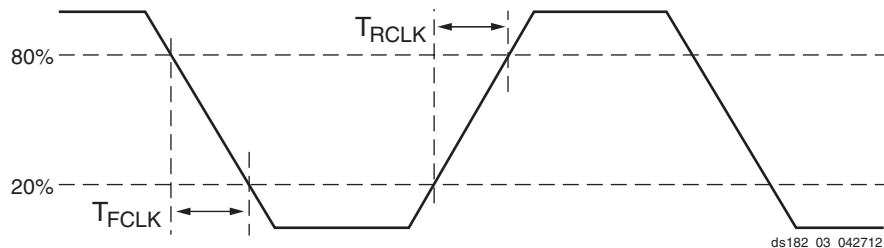


Figure 3: Reference Clock Timing Parameters

Table 57: GTX Transceiver PLL /Lock Time Adaptation

| Symbol             | Description   | Conditions  | All Speed Grades |        |                      | Units |
|--------------------|---|---|------------------|--------|----------------------|-------|
|                    |   |   | Min              | Typ    | Max                  |       |
| T <sub>LOCK</sub>  | Initial PLL lock  |   | –                | –      | 1                    | ms    |
| T <sub>DLOCK</sub> | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).             | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | –                | 50,000 | 37 x10 <sup>6</sup>  | UI    |
|                    | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. |   | –                | 50,000 | 2.3 x10 <sup>6</sup> | UI    |

Table 58: GTX Transceiver User Clock Switching Characteristics<sup>(1)(2)</sup>

| Symbol             | Description                 | Conditions       | Speed Grade       |                       |                       |                    | Units |
|--------------------|-----------------------------|------------------|-------------------|-----------------------|-----------------------|--------------------|-------|
|                    |                             |                  | 1.0V              |                       |                       | 0.9V               |       |
|                    |                             |                  | -3 <sup>(3)</sup> | -2/-2L <sup>(3)</sup> | -1/-1M <sup>(4)</sup> | -2L <sup>(5)</sup> |       |
| F <sub>TXOUT</sub> | TXOUTCLK maximum frequency  |                  | 412.500           | 412.500               | 312.500               | 237.500            | MHz   |
| F <sub>RXOUT</sub> | RXOUTCLK maximum frequency  |                  | 412.500           | 412.500               | 312.500               | 237.500            | MHz   |
| F <sub>TXIN</sub>  | TXUSRCLK maximum frequency  | 16-bit data path | 412.500           | 412.500               | 312.500               | 237.500            | MHz   |
|                    |                             | 32-bit data path | 390.625           | 322.266               | 250.000               | 206.250            | MHz   |
| F <sub>RXIN</sub>  | RXUSRCLK maximum frequency  | 16-bit data path | 412.500           | 412.500               | 312.500               | 237.500            | MHz   |
|                    |                             | 32-bit data path | 390.625           | 322.266               | 250.000               | 206.250            | MHz   |
| F <sub>TXIN2</sub> | TXUSRCLK2 maximum frequency | 16-bit data path | 412.500           | 412.500               | 312.500               | 237.500            | MHz   |
|                    |                             | 32-bit data path | 390.625           | 322.266               | 250.000               | 206.250            | MHz   |
|                    |                             | 64-bit data path | 195.313           | 161.133               | 125.000               | 103.125            | MHz   |
| F <sub>RXIN2</sub> | RXUSRCLK2 maximum frequency | 16-bit data path | 412.500           | 412.500               | 312.500               | 237.500            | MHz   |
|                    |                             | 32-bit data path | 390.625           | 322.266               | 250.000               | 206.250            | MHz   |
|                    |                             | 64-bit data path | 195.313           | 161.133               | 125.000               | 103.125            | MHz   |

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceivers User Guide* ([UG476](#)).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 59: GTX Transceiver Transmitter Switching Characteristics

| Symbol                       | Description                            | Condition  | Min   | Typ | Max                   | Units |
|------------------------------|--|------------|-------|-----|-----------------------|-------|
| F <sub>GTXTX</sub>           | Serial data rate range                 |            | 0.500 | –   | F <sub>GTXTXMAX</sub> | Gb/s  |
| T <sub>RTX</sub>             | TX Rise time                           | 20%–80%    | –     | 40  | –                     | ps    |
| T <sub>FTX</sub>             | TX Fall time                           | 80%–20%    | –     | 40  | –                     | ps    |
| T <sub>LLSKEW</sub>          | TX lane-to-lane skew <sup>(1)</sup>    |            | –     | –   | 500                   | ps    |
| V <sub>TXOOBVDDP</sub>       | Electrical idle amplitude              |            | –     | –   | 15                    | mV    |
| T <sub>TXOOBTRANSITION</sub> | Electrical idle transition time        |            | –     | –   | 140                   | ns    |
| T <sub>J12.5</sub>           | Total Jitter <sup>(2)(4)</sup>         | 12.5 Gb/s  | –     | –   | 0.28                  | UI    |
| D <sub>J12.5</sub>           | Deterministic Jitter <sup>(2)(4)</sup> |            | –     | –   | 0.17                  | UI    |
| T <sub>J11.18</sub>          | Total Jitter <sup>(2)(4)</sup>         | 11.18 Gb/s | –     | –   | 0.28                  | UI    |
| D <sub>J11.18</sub>          | Deterministic Jitter <sup>(2)(4)</sup> |            | –     | –   | 0.17                  | UI    |

**Table 59: GTX Transceiver Transmitter Switching Characteristics (Cont'd)**

| Symbol                 | Description                            | Condition                | Min | Typ | Max  | Units |
|------------------------|--|--------------------------|-----|-----|------|-------|
| TJ <sub>10.3125</sub>  | Total Jitter <sup>(2)(4)</sup>         | 10.3125 Gb/s             | –   | –   | 0.28 | UI    |
| DJ <sub>10.3125</sub>  | Deterministic Jitter <sup>(2)(4)</sup> |                          | –   | –   | 0.17 | UI    |
| TJ <sub>9.953</sub>    | Total Jitter <sup>(2)(4)</sup>         | 9.953 Gb/s               | –   | –   | 0.28 | UI    |
| DJ <sub>9.953</sub>    | Deterministic Jitter <sup>(2)(4)</sup> |                          | –   | –   | 0.17 | UI    |
| TJ <sub>9.8</sub>      | Total Jitter <sup>(2)(4)</sup>         | 9.8 Gb/s                 | –   | –   | 0.28 | UI    |
| DJ <sub>9.8</sub>      | Deterministic Jitter <sup>(2)(4)</sup> |                          | –   | –   | 0.17 | UI    |
| TJ <sub>8.0</sub>      | Total Jitter <sup>(2)(4)</sup>         | 8.0 Gb/s                 | –   | –   | 0.30 | UI    |
| DJ <sub>8.0</sub>      | Deterministic Jitter <sup>(2)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>6.6_QPLL</sub> | Total Jitter <sup>(2)(4)</sup>         | 6.6 Gb/s                 | –   | –   | 0.28 | UI    |
| DJ <sub>6.6_QPLL</sub> | Deterministic Jitter <sup>(2)(4)</sup> |                          | –   | –   | 0.17 | UI    |
| TJ <sub>6.6_CPLL</sub> | Total Jitter <sup>(3)(4)</sup>         | 6.6 Gb/s                 | –   | –   | 0.30 | UI    |
| DJ <sub>6.6_CPLL</sub> | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>5.0</sub>      | Total Jitter <sup>(3)(4)</sup>         | 5.0 Gb/s                 | –   | –   | 0.30 | UI    |
| DJ <sub>5.0</sub>      | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>4.25</sub>     | Total Jitter <sup>(3)(4)</sup>         | 4.25 Gb/s                | –   | –   | 0.30 | UI    |
| DJ <sub>4.25</sub>     | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>3.75</sub>     | Total Jitter <sup>(3)(4)</sup>         | 3.75 Gb/s                | –   | –   | 0.30 | UI    |
| DJ <sub>3.75</sub>     | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>3.2</sub>      | Total Jitter <sup>(3)(4)</sup>         | 3.20 Gb/s <sup>(5)</sup> | –   | –   | 0.2  | UI    |
| DJ <sub>3.2</sub>      | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.1  | UI    |
| TJ <sub>3.2L</sub>     | Total Jitter <sup>(3)(4)</sup>         | 3.20 Gb/s <sup>(6)</sup> | –   | –   | 0.32 | UI    |
| DJ <sub>3.2L</sub>     | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.16 | UI    |
| TJ <sub>2.5</sub>      | Total Jitter <sup>(3)(4)</sup>         | 2.5 Gb/s <sup>(7)</sup>  | –   | –   | 0.20 | UI    |
| DJ <sub>2.5</sub>      | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.08 | UI    |
| TJ <sub>1.25</sub>     | Total Jitter <sup>(3)(4)</sup>         | 1.25 Gb/s <sup>(8)</sup> | –   | –   | 0.15 | UI    |
| DJ <sub>1.25</sub>     | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.06 | UI    |
| TJ <sub>500</sub>      | Total Jitter <sup>(3)(4)</sup>         | 500 Mb/s                 | –   | –   | 0.1  | UI    |
| DJ <sub>500</sub>      | Deterministic Jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.03 | UI    |

**Notes:**

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL\_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL\_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of  $1e^{-12}$ .
- CPLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT\_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 4.

Table 60: GTX Transceiver Receiver Switching Characteristics

| Symbol   | Description  |                                     | Min   | Typ | Max                 | Units |
|--|--|-------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTXR</sub>  | Serial data rate   |                                     | 0.500 | –   | F <sub>GTXMAX</sub> | Gb/s  |
| T <sub>RXLECIDLE</sub>                                     | Time for RXLECIDLE to respond to loss or restoration of data |                                     | –     | 10  | –                   | ns    |
| RX <sub>OOBVDDPP</sub>                                     | OOB detect threshold peak-to-peak                            |                                     | 60    | –   | 150                 | mV    |
| RX <sub>SST</sub>  | Receiver spread-spectrum tracking <sup>(1)</sup>             | Modulated @ 33 KHz                  | –5000 | –   | 0                   | ppm   |
| RX <sub>RL</sub>   | Run length (CID)   |                                     | –     | –   | 512                 | UI    |
| RX <sub>PPMTOL</sub>                                       | Data/REFCLK PPM offset tolerance                             | Bit rates ≤ 6.6 Gb/s                | –1250 | –   | 1250                | ppm   |
|  |  | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700  | –   | 700                 | ppm   |
|  |  | Bit rates > 8.0 Gb/s                | –200  | –   | 200                 | ppm   |
| <b>SJ Jitter Tolerance<sup>(2)</sup></b>                   |  |                                     |       |     |                     |       |
| JT_SJ <sub>12.5</sub>                                      | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 12.5 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>11.18</sub>                                     | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 11.18 Gb/s                          | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>10.32</sub>                                     | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 10.32 Gb/s                          | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>9.95</sub>                                      | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 9.95 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>9.8</sub>                                       | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 9.8 Gb/s                            | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>8.0</sub>                                       | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 8.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>6.6_QPLL</sub>                                  | Sinusoidal Jitter (QPLL) <sup>(3)</sup>                      | 6.6 Gb/s                            | 0.48  | –   | –                   | UI    |
| JT_SJ <sub>6.6_CPLL</sub>                                  | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 6.6 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>5.0</sub>                                       | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 5.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>4.25</sub>                                      | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 4.25 Gb/s                           | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>3.75</sub>                                      | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 3.75 Gb/s                           | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>3.2</sub>                                       | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 3.2 Gb/s <sup>(4)</sup>             | 0.45  | –   | –                   | UI    |
| JT_SJ <sub>3.2L</sub>                                      | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 3.2 Gb/s <sup>(5)</sup>             | 0.45  | –   | –                   | UI    |
| JT_SJ <sub>2.5</sub>                                       | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 2.5 Gb/s <sup>(6)</sup>             | 0.5   | –   | –                   | UI    |
| JT_SJ <sub>1.25</sub>                                      | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 1.25 Gb/s <sup>(7)</sup>            | 0.5   | –   | –                   | UI    |
| JT_SJ <sub>500</sub>                                       | Sinusoidal Jitter (CPLL) <sup>(3)</sup>                      | 500 Mb/s                            | 0.4   | –   | –                   | UI    |
| <b>SJ Jitter Tolerance with Stressed Eye<sup>(2)</sup></b> |  |                                     |       |     |                     |       |
| JT_TJSE <sub>3.2</sub>                                     | Total Jitter with Stressed Eye <sup>(8)</sup>                | 3.2 Gb/s                            | 0.70  | –   | –                   | UI    |
| JT_TJSE <sub>6.6</sub>                                     |  | 6.6 Gb/s                            | 0.70  | –   | –                   | UI    |
| JT_SJSE <sub>3.2</sub>                                     | Sinusoidal Jitter with Stressed Eye <sup>(8)</sup>           | 3.2 Gb/s                            | 0.1   | –   | –                   | UI    |
| JT_SJSE <sub>6.6</sub>                                     |  | 6.6 Gb/s                            | 0.1   | –   | –                   | UI    |

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e<sup>-12</sup>.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT\_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- Composite jitter with RX in LPM or DFE mode.

## GTX Transceiver Protocol Jitter Characteristics

For Table 61 through Table 66, the 7 Series FPGAs GTX/GTH Transceivers User Guide (UG476) contains recommended settings for optimal usage of protocol specific characteristics.

Table 61: Gigabit Ethernet Protocol Characteristics

| Description  | Line Rate (Mb/s) | Min   | Max  | Units |
|--|------------------|-------|------|-------|
| <b>Gigabit Ethernet Transmitter Jitter Generation</b>            |                  |       |      |       |
| Total transmitter jitter (T_TJ)                                  | 1250             | –     | 0.24 | UI    |
| <b>Gigabit Ethernet Receiver High Frequency Jitter Tolerance</b> |                  |       |      |       |
| Total receiver jitter tolerance                                  | 1250             | 0.749 | –    | UI    |

Table 62: XAUI Protocol Characteristics

| Description  | Line Rate (Mb/s) | Min  | Max  | Units |
|--|------------------|------|------|-------|
| <b>XAUI Transmitter Jitter Generation</b>            |                  |      |      |       |
| Total transmitter jitter (T_TJ)                      | 3125             | –    | 0.35 | UI    |
| <b>XAUI Receiver High Frequency Jitter Tolerance</b> |                  |      |      |       |
| Total receiver jitter tolerance                      | 3125             | 0.65 | –    | UI    |

Table 63: PCI Express Protocol Characteristics<sup>(1)</sup>

| Standard  | Description                                   | Line Rate (Mb/s) | Min  | Max    | Units |    |
|---|---|------------------|------|--------|-------|----|
| <b>PCI Express Transmitter Jitter Generation</b>            |   |                  |      |        |       |    |
| PCI Express Gen 1   | Total transmitter jitter                      | 2500             | –    | 0.25   | UI    |    |
| PCI Express Gen 2   | Total transmitter jitter                      | 5000             | –    | 0.25   | UI    |    |
| PCI Express Gen 3 <sup>(2)</sup>                            | Total transmitter jitter uncorrelated         | 8000             | –    | 31.25  | ps    |    |
|   | Deterministic transmitter jitter uncorrelated |                  | –    | 12     | ps    |    |
| <b>PCI Express Receiver High Frequency Jitter Tolerance</b> |   |                  |      |        |       |    |
| PCI Express Gen 1   | Total receiver jitter tolerance               | 2500             | 0.65 | –      | UI    |    |
| PCI Express Gen 2 <sup>(3)</sup>                            | Receiver inherent timing error                | 5000             | 0.40 | –      | UI    |    |
|   | Receiver inherent deterministic timing error  |                  | 0.30 | –      | UI    |    |
| PCI Express Gen 3 <sup>(2)</sup>                            | Receiver sinusoidal jitter tolerance          | 0.03 MHz–1.0 MHz | 8000 | 1.00   | –     | UI |
|   |   | 1.0 MHz–10 MHz   |      | Note 4 | –     | UI |
|   |   | 10 MHz–100 MHz   |      | 0.10   | –     | UI |

**Notes:**

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 64: CEI-6G and CEI-11G Protocol Characteristics

| Description   | Line Rate (Mb/s) | Interface     | Min   | Max | Units |
|---|------------------|---------------|-------|-----|-------|
| <b>CEI-6G Transmitter Jitter Generation</b>             |                  |               |       |     |       |
| Total transmitter jitter <sup>(1)</sup>                 | 4976–6375        | CEI-6G-SR     | –     | 0.3 | UI    |
|   |                  | CEI-6G-LR     | –     | 0.3 | UI    |
| <b>CEI-6G Receiver High Frequency Jitter Tolerance</b>  |                  |               |       |     |       |
| Total receiver jitter tolerance <sup>(1)</sup>          | 4976–6375        | CEI-6G-SR     | 0.6   | –   | UI    |
|   |                  | CEI-6G-LR     | 0.95  | –   | UI    |
| <b>CEI-11G Transmitter Jitter Generation</b>            |                  |               |       |     |       |
| Total transmitter jitter <sup>(2)</sup>                 | 9950–11100       | CEI-11G-SR    | –     | 0.3 | UI    |
|   |                  | CEI-11G-LR/MR | –     | 0.3 | UI    |
| <b>CEI-11G Receiver High Frequency Jitter Tolerance</b> |                  |               |       |     |       |
| Total receiver jitter tolerance <sup>(2)</sup>          | 9950–11100       | CEI-11G-SR    | 0.65  | –   | UI    |
|   |                  | CEI-11G-MR    | 0.65  | –   | UI    |
|   |                  | CEI-11G-LR    | 0.825 | –   | UI    |

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 65: SFP+ Protocol Characteristics

| Description                                     | Line Rate (Mb/s)       | Min | Max  | Units |
|---|------------------------|-----|------|-------|
| <b>SFP+ Transmitter Jitter Generation</b>       |                        |     |      |       |
| Total transmitter jitter                        | 9830.40 <sup>(1)</sup> | –   | 0.28 | UI    |
|   | 9953.00                |     |      |       |
|   | 10312.50               |     |      |       |
|   | 10518.75               |     |      |       |
|   | 11100.00               |     |      |       |
| <b>SFP+ Receiver Frequency Jitter Tolerance</b> |                        |     |      |       |
| Total receiver jitter tolerance                 | 9830.40 <sup>(1)</sup> | 0.7 | –    | UI    |
|   | 9953.00                |     |      |       |
|   | 10312.50               |     |      |       |
|   | 10518.75               |     |      |       |
|   | 11100.00               |     |      |       |

**Notes:**

1. Line rated used for CPRI over SFP+ applications.

Table 66: CPRI Protocol Characteristics

| Description                                     | Line Rate (Mb/s) | Min    | Max    | Units |
|---|------------------|--------|--------|-------|
| <b>CPRI Transmitter Jitter Generation</b>       |                  |        |        |       |
| Total transmitter jitter                        | 614.4            | –      | 0.35   | UI    |
|   | 1228.8           | –      | 0.35   | UI    |
|   | 2457.6           | –      | 0.35   | UI    |
|   | 3072.0           | –      | 0.35   | UI    |
|   | 4915.2           | –      | 0.3    | UI    |
|   | 6144.0           | –      | 0.3    | UI    |
|   | 9830.4           | –      | Note 1 | UI    |
| <b>CPRI Receiver Frequency Jitter Tolerance</b> |                  |        |        |       |
| Total receiver jitter tolerance                 | 614.4            | 0.65   | –      | UI    |
|   | 1228.8           | 0.65   | –      | UI    |
|   | 2457.6           | 0.65   | –      | UI    |
|   | 3072.0           | 0.65   | –      | UI    |
|   | 4915.2           | 0.95   | –      | UI    |
|   | 6144.0           | 0.95   | –      | UI    |
|   | 9830.4           | Note 1 | –      | UI    |

**Notes:**

1. Tested per SFP+ specification, see Table 65.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

[www.xilinx.com/technology/protocols/pciexpress.htm](http://www.xilinx.com/technology/protocols/pciexpress.htm)

Table 67: Maximum Performance for PCI Express Designs

| Symbol                | Description                    | Speed Grade           |                       |        |        | Units |
|-----------------------|--------------------------------|-----------------------|-----------------------|--------|--------|-------|
|                       |                                | 1.0V                  |                       |        | 0.9V   |       |
|                       |                                | -3                    | -2/-2L                | -1/-1M | -2L    |       |
| F <sub>PIPECLK</sub>  | Pipe clock maximum frequency   | 250.00                | 250.00                | 250.00 | 250.00 | MHz   |
| F <sub>USERCLK</sub>  | User clock maximum frequency   | 500.00 <sup>(1)</sup> | 500.00 <sup>(1)</sup> | 250.00 | 250.00 | MHz   |
| F <sub>USERCLK2</sub> | User clock 2 maximum frequency | 250.00                | 250.00                | 250.00 | 250.00 | MHz   |
| F <sub>DRPCLK</sub>   | DRP clock maximum frequency    | 250.00                | 250.00                | 250.00 | 250.00 | MHz   |

**Notes:**

1. PCI Express x8 Gen 3 operation is only supported in -2 and -3 speed grades.



## XADC Specifications

Table 68: XADC Specifications

| Parameter   | Symbol     | Comments/Conditions  | Min  | Typ | Max         | Units               |
|---|------------|--|------|-----|-------------|---------------------|
| $V_{CCADC} = 1.8V \pm 5\%$ , $V_{REFP} = 1.25V$ , $V_{REFN} = 0V$ , $ADCCLK = 26\text{ MHz}$ , $T_j = -40^\circ\text{C}$ to $100^\circ\text{C}$ , Typical values at $T_j = +40^\circ\text{C}$ |            |  |      |     |             |                     |
| <b>ADC Accuracy<sup>(1)</sup></b>   |            |  |      |     |             |                     |
| Resolution  |            |  | 12   | –   | –           | Bits                |
| Integral Nonlinearity <sup>(2)</sup>  | INL        |  | –    | –   | $\pm 3$     | LSBs                |
| Differential Nonlinearity   | DNL        | No missing codes, guaranteed monotonic   | –    | –   | $\pm 1$     | LSBs                |
| Offset Error  |            | Offset calibration enabled   | –    | –   | $\pm 6$     | LSBs                |
| Gain Error  |            | Gain calibration disabled  | –    | –   | $\pm 0.5$   | %                   |
| Offset Matching   |            | Offset calibration enabled   | –    | –   | 4           | LSBs                |
| Gain Matching   |            | Gain calibration disabled  | –    | –   | 0.3         | %                   |
| Sample Rate   |            |  | 0.1  | –   | 1           | MS/s                |
| Signal to Noise Ratio <sup>(2)</sup>  | SNR        | $F_{SAMPLE} = 500\text{KS/s}$ , $F_{IN} = 20\text{KHz}$  | 60   | –   | –           | dB                  |
| RMS Code Noise  |            | External 1.25V reference   | –    | –   | 2           | LSBs                |
|   |            | On-chip reference  | –    | 3   | –           | LSBs                |
| Total Harmonic Distortion <sup>(2)</sup>  | THD        | $F_{SAMPLE} = 500\text{KS/s}$ , $F_{IN} = 20\text{KHz}$  | –    | 70  | –           | dB                  |
| <b>ADC Accuracy at Extended Temperatures</b>  |            |  |      |     |             |                     |
| Resolution  |            | $T_j = -55^\circ\text{C}$ to $125^\circ\text{C}$   | 10   | –   | –           | Bits                |
| Integral Nonlinearity <sup>(2)</sup>  | INL        | $T_j = -55^\circ\text{C}$ to $125^\circ\text{C}$   | –    | –   | $\pm 1$     | LSB<br>(at 10 bits) |
| Differential Nonlinearity   | DNL        | No missing codes, guaranteed monotonic,<br>$T_j = -55^\circ\text{C}$ to $125^\circ\text{C}$          | –    | –   | $\pm 1$     |                     |
| <b>Analog Inputs<sup>(3)</sup></b>  |            |  |      |     |             |                     |
| ADC Input Ranges  |            | Unipolar operation   | 0    | –   | 1           | V                   |
|   |            | Bipolar operation  | –0.5 | –   | +0.5        | V                   |
|   |            | Unipolar common mode range (FS input)  | 0    | –   | +0.5        | V                   |
|   |            | Bipolar common mode range (FS input)   | +0.5 | –   | +0.6        | V                   |
| Maximum External Channel Input Ranges   |            | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels       | –0.1 | –   | $V_{CCADC}$ | V                   |
| Auxiliary Channel Full Resolution Bandwidth   | FRBW       |  | 250  | –   | –           | KHz                 |
| <b>On-Chip Sensors</b>  |            |  |      |     |             |                     |
| Temperature Sensor Error  |            | $T_j = -40^\circ\text{C}$ to $100^\circ\text{C}$ .   | –    | –   | $\pm 4$     | $^\circ\text{C}$    |
|   |            | $T_j = -55^\circ\text{C}$ to $+125^\circ\text{C}$  | –    | –   | $\pm 6$     | $^\circ\text{C}$    |
| Supply Sensor Error   |            | Measurement range of $V_{CCAUX}$ $1.8V \pm 5\%$<br>$T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$ | –    | –   | $\pm 1$     | %                   |
|   |            | Measurement range of $V_{CCAUX}$ $1.8V \pm 5\%$<br>$T_j = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | –    | –   | $\pm 2$     | %                   |
| <b>Conversion Rate<sup>(4)</sup></b>  |            |  |      |     |             |                     |
| Conversion Time - Continuous  | $t_{CONV}$ | Number of ADCCLK cycles  | 26   | –   | 32          | Cycles              |
| Conversion Time - Event   | $t_{CONV}$ | Number of CLK cycles   | –    | –   | 21          | Cycles              |
| DRP Clock Frequency   | DCLK       | DRP clock frequency  | 8    | –   | 250         | MHz                 |
| ADC Clock Frequency   | ADCCLK     | Derived from DCLK  | 1    | –   | 26          | MHz                 |

Table 68: XADC Specifications (Cont'd)

| Parameter                           | Symbol            | Comments/Conditions   | Min    | Typ  | Max    | Units |
|-------------------------------------|-------------------|---|--------|------|--------|-------|
| DCLK Duty Cycle                     |                   |   | 40     | –    | 60     | %     |
| <b>XADC Reference<sup>(5)</sup></b> |                   |   |        |      |        |       |
| External Reference                  | V <sub>REFP</sub> | Externally supplied reference voltage                                 | 1.20   | 1.25 | 1.30   | V     |
| On-Chip Reference                   |                   | Ground V <sub>REFP</sub> pin to AGND, T <sub>j</sub> = –40°C to 100°C | 1.2375 | 1.25 | 1.2625 | V     |

**Notes:**

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for bitstream option XADCEnhancedLinearity = ON.
- For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480)*.
- For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480)*.
- Any variation in the reference voltage from the nominal V<sub>REFP</sub> = 1.25V and V<sub>REFN</sub> = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

## Configuration Switching Characteristics

Table 69: Configuration Switching Characteristics

| Symbol                                 | Description   | Speed Grade |        |        |       | Units       |
|--|---|-------------|--------|--------|-------|-------------|
|  |   | 1.0V        |        |        | 0.9V  |             |
|  |   | -3          | -2/-2L | -1/-1M | -2L   |             |
| <b>Power-up Timing Characteristics</b> |   |             |        |        |       |             |
| T <sub>PL</sub> <sup>(1)</sup>         | Program latency   | 5           | 5      | 5      | 5     | ms, Max     |
| T <sub>POR</sub> <sup>(1)</sup>        | Power-on reset (50 ms ramp rate time)                         | 10/50       | 10/50  | 10/50  | 10/50 | ms, Min/Max |
|  | Power-on reset (1 ms ramp rate time)                          | 10/35       | 10/35  | 10/35  | 10/35 | ms, Min/Max |
| T <sub>PROGRAM</sub>                   | Program pulse width   | 250         | 250    | 250    | 250   | ns, Min     |
| <b>CCLK Output (Master Mode)</b>       |   |             |        |        |       |             |
| T <sub>ICCK</sub>                      | Master CCLK output delay                                      | 150         | 150    | 150    | 150   | ns, Min     |
| T <sub>MCCKL</sub>                     | Master CCLK clock Low time duty cycle                         | 40/60       | 40/60  | 40/60  | 40/60 | %, Min/Max  |
| T <sub>MCCKH</sub>                     | Master CCLK clock High time duty cycle                        | 40/60       | 40/60  | 40/60  | 40/60 | %, Min/Max  |
| F <sub>MCCK</sub>                      | Master CCLK frequency   | 100.00      | 100.00 | 100.00 | 70.00 | MHz, Max    |
|  | Master CCLK frequency for AES encrypted x16                   | 50.00       | 50.00  | 50.00  | 35.00 | MHz, Max    |
| F <sub>MCCK_START</sub>                | Master CCLK frequency at start of configuration               | 3.00        | 3.00   | 3.00   | 3.00  | MHz, Typ    |
| F <sub>MCCKTOL</sub>                   | Frequency tolerance, master mode with respect to nominal CCLK | ±50         | ±50    | ±50    | ±50   | %, Max      |
| <b>CCLK Input (Slave Modes)</b>        |   |             |        |        |       |             |
| T <sub>SCCKL</sub>                     | Slave CCLK clock minimum Low time                             | 2.50        | 2.50   | 2.50   | 2.50  | ns, Min     |
| T <sub>SCCKH</sub>                     | Slave CCLK clock minimum High time                            | 2.50        | 2.50   | 2.50   | 2.50  | ns, Min     |
| F <sub>SCCK</sub>                      | Slave CCLK frequency  | 100.00      | 100.00 | 100.00 | 70.00 | MHz, Max    |
| <b>EMCCLK Input (Master Mode)</b>      |   |             |        |        |       |             |
| T <sub>EMCCKL</sub>                    | External master CCLK Low time                                 | 2.50        | 2.50   | 2.50   | 2.50  | ns, Min     |
| T <sub>EMCCKH</sub>                    | External master CCLK High time                                | 2.50        | 2.50   | 2.50   | 2.50  | ns, Min     |
| F <sub>EMCCK</sub>                     | External master CCLK frequency                                | 100.00      | 100.00 | 100.00 | 70.00 | MHz, Max    |

Table 69: Configuration Switching Characteristics (Cont'd)

| Symbol  | Description  | Speed Grade |            |            |            | Units       |
|---|--|-------------|------------|------------|------------|-------------|
|   |  | 1.0V        |            |            | 0.9V       |             |
|   |  | -3          | -2/-2L     | -1/-1M     | -2L        |             |
| <b>Internal Configuration Access Port</b>             |  |             |            |            |            |             |
| F <sub>ICAPCK</sub>                                   | Internal configuration access port (ICAPE2)                | 100.00      | 100.00     | 100.00     | 70.00      | MHz, Max    |
| <b>Master/Slave Serial Mode Programming Switching</b> |  |             |            |            |            |             |
| T <sub>DCCK</sub> /T <sub>CCKD</sub>                  | DIN Setup/Hold   | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 5.00/0.00  | ns, Min     |
| T <sub>CCO</sub>                                      | DOOUT clock to out   | 8.00        | 8.00       | 8.00       | 9.00       | ns, Max     |
| <b>SelectMAP Mode Programming Switching</b>           |  |             |            |            |            |             |
| T <sub>SMDCCK</sub> /T <sub>SMCCKD</sub>              | D[31:00] Setup/Hold  | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 4.50/0.00  | ns, Min     |
| T <sub>SMCSCCK</sub> /T <sub>SMCCKCS</sub>            | CSI_B Setup/Hold   | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 5.00/0.00  | ns, Min     |
| T <sub>SMWCK</sub> /T <sub>SMCKKW</sub>               | RDWR_B Setup/Hold  | 10.00/0.00  | 10.00/0.00 | 10.00/0.00 | 12.00/0.00 | ns, Min     |
| T <sub>SMCKCSO</sub>                                  | CSO_B clock to out (330Ω pull-up resistor required)        | 7.00        | 7.00       | 7.00       | 8.00       | ns, Max     |
| T <sub>SMCO</sub>                                     | D[31:00] clock to out in readback                          | 8.00        | 8.00       | 8.00       | 10.00      | ns, Max     |
| F <sub>RBCK</sub>                                     | Readback frequency   | 100.00      | 100.00     | 100.00     | 70.00      | MHz, Max    |
| <b>Boundary-Scan Port Timing Specifications</b>       |  |             |            |            |            |             |
| T <sub>TAPTCK</sub> /T <sub>TCKTAP</sub>              | TMS and TDI Setup/Hold                                     | 3.00/2.00   | 3.00/2.00  | 3.00/2.00  | 3.00/2.00  | ns, Min     |
| T <sub>TCKTDO</sub>                                   | TCK falling edge to TDO output                             | 7.00        | 7.00       | 7.00       | 8.50       | ns, Max     |
| F <sub>TCK</sub>                                      | TCK frequency  | 66.00       | 66.00      | 66.00      | 50.00      | MHz, Max    |
| <b>BPI Flash Master Mode Programming Switching</b>    |  |             |            |            |            |             |
| T <sub>BPICCO</sub> <sup>(2)</sup>                    | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out | 8.50        | 8.50       | 8.50       | 10.00      | ns, Max     |
| T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>              | D[15:00] Setup/Hold  | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 4.50/0.00  | ns, Min     |
| <b>SPI Flash Master Mode Programming Switching</b>    |  |             |            |            |            |             |
| T <sub>SPIDCC</sub> /T <sub>SPICCD</sub>              | D[03:00] Setup/Hold  | 3.00/0.00   | 3.00/0.00  | 3.00/0.00  | 3.00/0.00  | ns, Min     |
| T <sub>SPICCM</sub>                                   | MOSI clock to out  | 8.00        | 8.00       | 8.00       | 9.00       | ns, Max     |
| T <sub>SPICFC</sub>                                   | FCS_B clock to out   | 8.00        | 8.00       | 8.00       | 9.00       | ns, Max     |
| <b>USRCCLK Output</b>                                 |  |             |            |            |            |             |
| T <sub>USRCCLKO</sub>                                 | STARTUPE2 USRCCLKO input to CCLK output                    | 0.50/6.00   | 0.50/6.70  | 0.50/7.50  | 0.50/7.50  | ns, Min/Max |
| <b>Device DNA Access Port</b>                         |  |             |            |            |            |             |
| F <sub>DNACK</sub>                                    | DNA access port (DNA_PORT)                                 | 100.00      | 100.00     | 100.00     | 70.00      | MHz, Max    |

**Notes:**

- To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## eFUSE Programming Conditions

Table 70 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide (UG470)*.

Table 70: eFUSE Programming Conditions<sup>(1)</sup>

| Symbol   | Description                | Min | Typ | Max | Units |
|----------|----------------------------|-----|-----|-----|-------|
| $I_{FS}$ | $V_{CCAUX}$ supply current | –   | –   | 115 | mA    |
| $t_j$    | Temperature range          | 15  | –   | 125 | °C    |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.

## Revision History

The following table shows the revision history for this document:

| Date       | Version | Description   |
|------------|---------|---|
| 03/01/2011 | 1.0     | Initial Xilinx release.   |
| 04/01/2011 | 1.1     | Added the XC7K355T, XC7K420T, and XC7K480T devices throughout data sheet. Added the extended temperature range discussion to <a href="#">page 1</a> . Updated $V_{CCAUX\_IO}$ in <a href="#">Table 2</a> . Edits to clarify <a href="#">Power-On/Off Power Supply Sequencing</a> power sequencing discussion. Added $I_{CCAUX\_IO}$ and $I_{CCBRAM}$ to <a href="#">Table 6</a> and <a href="#">Table 7</a> . Updated $MMCM\_F_{INDUTY}$ and added $F_{INJITTER}$ , $T_{OUTJITTER}$ , $T_{EXTFDVAR}$ , and <a href="#">Note 3</a> to <a href="#">Table 39</a> . Removed the SBG324 package from <a href="#">Table 51</a> . Updated the <a href="#">Notice of Disclaimer</a> .   |
| 10/04/2011 | 1.2     | Replaced -1L with -2L throughout this data sheet. Updated Min/Max values and removed Note 5 from <a href="#">Table 2</a> . Clarified <a href="#">Power-On/Off Power Supply Sequencing</a> power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to <a href="#">Table 8</a> . Updated $V_{ICM}$ in <a href="#">Table 12</a> and <a href="#">Table 13</a> . Added Note 1 to table 12. Updated <a href="#">Table 70</a> including adding <a href="#">Note 1</a> . Added <i>Absolute Maximum Ratings for GTX Transceivers</i> . Revised the reference clock maximum frequency ( $F_{GCLK}$ ) in <a href="#">Table 56</a> . Added <a href="#">Table 58</a> . Added LVTTTL and removed SSTL135_II and SSTL15_II specifications from <a href="#">Table 20</a> . Removed HSTL_III from <a href="#">Table 21</a> . Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated $T_{DELAYPAT\_JIT}$ in <a href="#">Table 27</a> . Added $T_{AS}/T_{AH}$ to <a href="#">Table 29</a> . Added $T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$ and $T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$ to <a href="#">Table 32</a> . Completely updated <a href="#">Table 69</a> . Updated the <a href="#">AC Switching Characteristics</a> in <a href="#">Table 20</a> , <a href="#">Table 21</a> , <a href="#">Table 22</a> , <a href="#">Table 23</a> , <a href="#">Table 24</a> , <a href="#">Table 25</a> , <a href="#">Table 27</a> through <a href="#">Table 39</a> , <a href="#">Table 41</a> though <a href="#">Table 38</a> , and <a href="#">Table 67</a> .   |
| 11/03/2011 | 1.3     | Revised the $V_{OCM}$ specification in <a href="#">Table 12</a> . Updated the <a href="#">AC Switching Characteristics</a> based upon the ISE 13.3 v1.02 speed specification throughout document including <a href="#">Table 20</a> and <a href="#">Table 21</a> . Added $MMCM\_T_{FBDELAY}$ while adding $MMCM\_$ to the symbol names of a few specifications in <a href="#">Table 39</a> and PLL to the symbol names in <a href="#">Table 40</a> . In <a href="#">Table 41</a> through <a href="#">Table 48</a> , updated the pin-to-pin descriptions with the SSTL15 standard. Updated units in <a href="#">Table 50</a> .   |
| 02/13/2012 | 1.4     | Updated summary description on <a href="#">page 1</a> . In <a href="#">Table 2</a> , revised $V_{CCO}$ for the 3.3V HR I/O banks and updated $T_j$ . Added typical values to <a href="#">Table 3</a> . Updated the notes in <a href="#">Table 6</a> . Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to <a href="#">Table 8</a> . Rearranged <a href="#">Table 9</a> , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added <a href="#">Table 10</a> and <a href="#">Table 11</a> . Revised the specifications in <a href="#">Table 12</a> and <a href="#">Table 13</a> . Updated the <a href="#">eFUSE Programming Conditions</a> section and removed the endurance table. Added the <a href="#">IO_FIFO Switching Characteristics</a> table. Revised $I_{CCADC}$ and updated <a href="#">Note 1</a> in <a href="#">Table 68</a> . Revised DDR LVDS transmitter data width in <a href="#">Table 17</a> . Updated the <a href="#">AC Switching Characteristics</a> based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from <a href="#">Table 29</a> as they are no longer applicable. Updated specifications in <a href="#">Table 69</a> . Updated <a href="#">Note 1</a> in <a href="#">Table 38</a> .<br>In the <a href="#">GTX Transceiver DC Input and Output Levels</a> section: Revised $V_{IN}$ , and added $I_{DCIN}$ and $I_{DCOUT}$ to <a href="#">Table 52</a> . Added <a href="#">Note 4</a> to <a href="#">Table 54</a> . In <a href="#">Table 56</a> , revised $F_{GCLK}$ , removed $T_{PHASE}$ , and added $T_{DLOCK}$ . Revised specifications and added <a href="#">Note 2</a> to <a href="#">Table 58</a> . Added <a href="#">Table 59</a> and <a href="#">Table 60</a> along with <a href="#">GTX Transceiver Protocol Jitter Characteristics</a> in <a href="#">Table 61</a> through <a href="#">Table 66</a> . |

| Date       | Version | Description   |
|------------|---------|---|
| 05/23/2012 | 1.5     | <p>Reorganized entire data sheet including adding <a href="#">Table 45</a> and <a href="#">Table 49</a>.</p> <p>Updated <math>T_{SOL}</math> in <a href="#">Table 1</a>. Updated <math>I_{BATT}</math> and added <math>R_{IN\_TERM}</math> to <a href="#">Table 3</a>. Added values to <a href="#">Table 6</a> and <a href="#">Table 7</a>. Updated <a href="#">Power-On/Off Power Supply Sequencing</a>, <a href="#">page 6</a> with regards to GTX transceivers.</p> <p>Updated many parameters in <a href="#">Table 9</a> including SSTL135 and SSTL135_R. Removed <math>V_{OX}</math> column and added DIFF_HSUL_12 to <a href="#">Table 11</a>. Updated <math>V_{OL}</math> in <a href="#">Table 12</a>. Updated <a href="#">Table 17</a> and removed notes 2 and 3. Updated <a href="#">Table 18</a>.</p> <p>Updated the <a href="#">AC Switching Characteristics</a> based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and -2L (0.9V) speed specifications throughout the document.</p> <p>In <a href="#">Table 32</a>, updated <a href="#">Reset Delays</a> section including <a href="#">Note 10</a> and <a href="#">Note 11</a>. Added data for <math>T_{LOCK}</math> and <math>T_{DLOCK}</math> in <a href="#">Table 56</a>. Updated many of the XADC specifications in <a href="#">Table 68</a> and added <a href="#">Note 2</a>. Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from <a href="#">Table 69</a> to <a href="#">Table 39</a> and <a href="#">Table 40</a>.</p>  |
| 07/25/2012 | 1.6     | <p>Updated the descriptions, changed <math>V_{IN}</math> and <a href="#">Note 2</a> and added <a href="#">Note 4</a> in <a href="#">Table 1</a>. In <a href="#">Table 2</a>, changed descriptions and notes, removed <a href="#">Note 7</a>, changed GTX transceiver parameters and values and added <a href="#">Note 12</a>. Updated parameters in <a href="#">Table 3</a>. Added <a href="#">Table 4</a> and <a href="#">Table 5</a>.</p> <p>Changed the typical values for many of the devices in <a href="#">Table 7</a>. Updated LVCMOS12 and the SSTLs in <a href="#">Table 9</a>. Updated many of the specifications in <a href="#">Table 10</a> and <a href="#">Table 11</a>.</p> <p>Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to <a href="#">Table 15</a> and <a href="#">Table 16</a> including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations.</p> <p>Added notes and specifications to <a href="#">Table 18</a> and <a href="#">Table 19</a>.</p> <p>Updated the <a href="#">IOB Pad Input/Output/3-State</a> discussion and changed <a href="#">Table 22</a> by adding <math>T_{IOBUFDISABLE}</math>.</p> <p>Removed many of the combinatorial delay specifications and <math>T_{CINCK}/T_{CKCIN}</math> from <a href="#">Table 29</a>.</p> <p>Rearranged <a href="#">Table 52</a> including moving some parameters to <a href="#">Table 1</a>. Added <a href="#">Table 57</a>. Updated <a href="#">Table 58</a>. In <a href="#">Table 60</a>, updated SJ Jitter Tolerance with Stressed Eye section, <a href="#">page 53</a> and <a href="#">Note 8</a>. Added <a href="#">Note 1</a>, <a href="#">Note 2</a>, and <a href="#">Note 3</a> to <a href="#">Table 63</a>. Added <a href="#">Note 1</a> and <a href="#">Note 2</a> to <a href="#">Table 64</a>, and line rate ranges. Updated <a href="#">Table 65</a> including adding <a href="#">Note 1</a>. Updated <a href="#">Table 66</a> including adding <a href="#">Note 1</a>. In <a href="#">Table 68</a> updated <a href="#">Note 1</a> and added <a href="#">Note 4</a>. In <a href="#">Table 69</a>, updated <math>T_{POR}</math> and <math>F_{EMCCK}</math>.</p> |
| 09/04/2012 | 1.7     | <p>Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.</p>  |
| 09/26/2012 | 1.8     | <p>In <a href="#">Table 2</a>, revised <math>V_{CCINT}</math> and <math>V_{CCBRAM}</math> and added <a href="#">Note 3</a>. Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.</p>   |
| 10/10/2012 | 1.9     | <p>Updated the <math>I_{CCINTMIN}</math> value for the XC7K355T in <a href="#">Table 7</a>. Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.</p>   |
| 10/25/2012 | 2.0     | <p>Updated the <a href="#">AC Switching Characteristics</a> based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document.</p> <p>Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the XC7K325T and XC7K410T in the -2L (0.9V).</p> <p>Added values for <a href="#">Table 17</a> -2L (0.9V). Added package skew values to <a href="#">Table 51</a>. In <a href="#">Table 54</a>, increased -1 speed grade (FF package) <math>F_{GTXMAX}</math> value from 6.6 Gb/s to 8.0 Gb/s.</p>   |
| 10/31/2012 | 2.1     | <p>Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.</p>   |
| 11/26/2012 | 2.2     | <p>Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed <a href="#">Note 4</a> from <a href="#">Table 68</a>.</p>  |
| 12/05/2012 | 2.3     | <p>Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated <a href="#">Note 1</a> in <a href="#">Table 51</a>.</p>   |
| 12/12/2012 | 2.4     | <p>Updated <a href="#">Table 15</a> and <a href="#">Table 16</a> for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added <a href="#">Internal Configuration Access Port</a> section to <a href="#">Table 69</a>.</p>   |

| Date       | Version | Description   |
|------------|---------|---|
| 10/04/2013 | 2.5     | In <a href="#">Table 1</a> , revised $V_{IN}$ (I/O input voltage) to match values in <a href="#">Table 4</a> and <a href="#">Table 5</a> , and combined <a href="#">Note 4</a> with old <a href="#">Note 5</a> and then added new <a href="#">Note 5</a> . Also in <a href="#">Table 1</a> , updated $I_{DCIN}$ and $I_{DCOUT}$ sections. Revised $V_{IN}$ description and added <a href="#">Note 3</a> and <a href="#">Note 8</a> in <a href="#">Table 2</a> . Updated first 3 rows in <a href="#">Table 4</a> and <a href="#">Table 5</a> . Replaced XPower with Xilinx Power Estimator (XPE) in sentence before <a href="#">Table 7</a> . Updated $V_{IL}$ minimum for PCI33_3 in <a href="#">Table 9</a> . Added <a href="#">Note 1</a> to <a href="#">Table 12</a> . Added <a href="#">Note 1</a> to <a href="#">Table 13</a> . Added Vivado Design Suite to <a href="#">AC Switching Characteristics</a> . Updated titles of <a href="#">Table 18</a> and <a href="#">Table 19</a> , and removed the following note: <i>RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP</i> . Updated $T_{IOOP}$ and $T_{IOTP}$ values in <a href="#">Table 20</a> . Replaced “TRACE report” with “timing report” in notes for <a href="#">Table 26</a> , <a href="#">Table 27</a> , <a href="#">Table 28</a> , <a href="#">Table 30</a> , and <a href="#">Table 32</a> . Removed this note: <i>A Zero “0” Hold Time listing indicates no hold time or a negative hold time</i> from <a href="#">Table 30</a> , <a href="#">Table 31</a> , and <a href="#">Table 46</a> . Updated <a href="#">Note 1</a> in <a href="#">Table 36</a> . Updated <a href="#">Table 58</a> to more accurately show transceiver user clocks for supported line rates. Updated <a href="#">Note 8</a> and description of $F_{GTXRX}$ in <a href="#">Table 60</a> . Updated <a href="#">Note 2</a> , <a href="#">Note 3</a> , and <a href="#">Note 4</a> in <a href="#">Table 68</a> . Added $T_{USRCLK0}$ to <a href="#">Table 69</a> . |
| 11/27/2013 | 2.6     | Added Kintex-7Q defense-grade devices throughout. Added -1M speed grade throughout. Added reference to <i>7 Series FPGAs Overview</i> and <i>Defense-Grade 7 Series FPGAs Overview</i> in <a href="#">Introduction</a> . In <a href="#">Table 2</a> , added junction temperature operating range for military (M) devices. In <a href="#">Table 3</a> , removed commercial (C), industrial (I), and extended (E) from descriptions of $R_{IN\_TERM}$ . Updated temperature ranges in <a href="#">Table 4</a> and <a href="#">Table 5</a> . Removed <a href="#">Note 1</a> and <a href="#">Note 2</a> from <a href="#">Table 7</a> . Added $T_J = 125^{\circ}\text{C}$ to Conditions column for $T_{VCCO2VCCAUX}$ in <a href="#">Table 8</a> . Added <a href="#">Table 14</a> . Updated description of $MMCM\_F_{PFDMAX}$ in <a href="#">Table 39</a> . Updated description of $PLL\_F_{PFDMAX}$ in <a href="#">Table 40</a> . Added RF package type to <a href="#">Table 54</a> . Added $F_{DNACK}$ to <a href="#">Table 69</a> .   |
| 02/07/2014 | 2.7     | Updated the <a href="#">AC Switching Characteristics</a> based upon ISE 14.7 and Vivado 2013.4. Updated <a href="#">Note 5</a> and added <a href="#">Note 6</a> to <a href="#">Table 2</a> . Added <a href="#">Note 2</a> to <a href="#">Table 4</a> . Added <a href="#">Note 2</a> and updated <a href="#">Note 3</a> in <a href="#">Table 5</a> . Added HSUL_12_F, DIFF_HSUL_12_F, MOBILE_DDR_S, MOBILE_DDR_F, DIFF_MOBILE_DDR_S, and DIFF_MOBILE_DDR_F standards to and updated values in <a href="#">Table 20</a> . Added HSUL_12_F, DIFF_HSUL_12_F, DIFF_HSUL_12_DCI_S, and DIFF_HSUL_12_DCI_F standards to and updated values in <a href="#">Table 21</a> . In <a href="#">Table 33</a> , corrected $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ from 478.27 to 478.24 MHz to match software behavior. Removed introductory paragraph of <a href="#">Device Pin-to-Pin Output Parameter Guidelines</a> and <a href="#">Device Pin-to-Pin Input Parameter Guidelines</a> . Updated display format of “ADC Accuracy at Extended Temperatures” section in <a href="#">Table 68</a> .   |
| 03/04/2014 | 2.8     | Updated <a href="#">Note 2</a> in <a href="#">Table 4</a> and <a href="#">Note 2</a> in <a href="#">Table 5</a> . For XQ7K325T and XQ7K410T in <a href="#">Table 15</a> , changed -2 and -1 speed grades to -2I and -1I, respectively, and moved all XQ7K325T speed grades from Preliminary to Production. In <a href="#">Table 16</a> , added production software for XQ7K325T -2/2L, -1, -1M, and (0.9V) -2L speed grades. Removed “and FB” from title of <a href="#">Table 19</a> . Removed notes from <a href="#">Table 20</a> and <a href="#">Table 21</a> . Added <a href="#">Note 1</a> to <a href="#">Table 67</a> .  |

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