74HC30; 74HCT30

8-input NAND gate Rev. 6 — 27 December 2012

Product data sheet

1. **General description**

The 74HC30; 74HCT30 is an 8-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features and benefits 2.

- Complies with JEDEC standard JESD7A
- Input levels:
 - ◆ For 74HC30: CMOS level
 - ◆ For 74HCT30: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

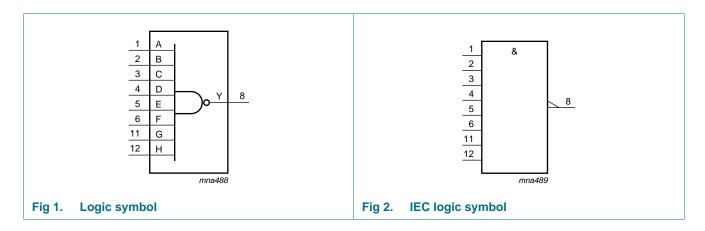
Ordering information 3.

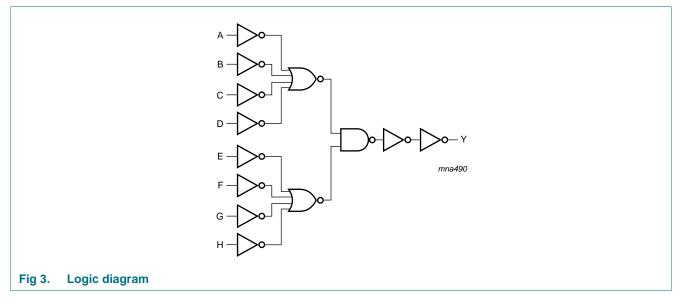
Table 1. **Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74HC30N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT30N				
74HC30D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1
74HCT30D			body width 3.9 mm	
74HC30DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body	SOT337-1
74HCT30DB			width 5.3 mm	
74HC30PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1
74HCT30PW			body width 4.4 mm	



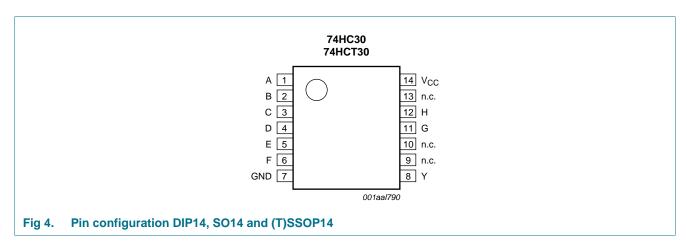
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

14510 2: 1 111 4	Coonplion	
Symbol	Pin	Description
Α	1	data input
В	2	data input
С	3	data input
D	4	data input
E	5	data input
F	6	data input
GND	7	ground (0 V)
Υ	8	data output
n.c.	9	not connected
n.c.	10	not connected
G	11	data input
Н	12	data input
n.c.	13	not connected
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input								Output
Α	В	С	D	E	F	G	Н	Y
L	Χ	X	X	X	X	Χ	X	Н
X	L	Х	Х	Х	Х	Χ	Х	Н
X	Х	L	Х	Х	Х	Х	Х	Н
X	Χ	Х	L	Х	Х	Χ	Χ	Н
X	Χ	Х	Х	L	Х	Χ	Χ	Н
X	Χ	Х	Х	Х	L	Χ	Χ	Н
Χ	Х	Χ	Х	Х	Х	L	Χ	Н
Χ	Х	Χ	Х	Х	Х	Χ	L	Н
Н	Н	Н	Н	Н	Н	Н	Н	L

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
I _{OK}	output clamping current	V_{O} < -0.5 V or V_{O} > V_{CC} + 0.5 V	<u>[1]</u> _	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation				
	DIP14 package		[2] _	750	mW
	SO14, (T)SSOP14 packages		[2] _	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC30		•	74HCT30)	Unit
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
Vo	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC30										
V _{IH}	HIGH-level	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	8.0	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A$; $V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
II	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μΑ

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Uni
			Min	Тур	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT3	0									
V _{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	8.0	-	0.8	-	0.8	V
V_{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = -20 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = 20 \mu A$	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 4.0 \text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Δl _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.4 \text{ V; } I_O = 0 \text{ A;}$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	60	216	-	275	-	294	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

 Table 7.
 Dynamic characteristics

 $GND = 0 \text{ V; } C_L = 50 \text{ pF; for load circuit see } Figure 6.$

Symbol	Parameter	Conditions			25 °C		-40 °C to	+125 °C	Unit
				Min	Тур	Max	Max (85 °C)	Max (125 °C)	
74HC30									
t _{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see Figure 5	[1]						
		V _{CC} = 2.0 V		-	41	130	165	195	ns
		$V_{CC} = 4.5 \text{ V}$		-	15	26	33	39	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	12	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	12	22	28	33	ns
t _t	transition time	see Figure 5	[2]						
		$V_{CC} = 2.0 \text{ V}$		-	19	75	95	110	ns
		V _{CC} = 4.5 V		-	7	15	19	22	ns
		V _{CC} = 6.0 V		-	6	13	16	19	ns

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Table 7. Dynamic characteristics ...continued GND = 0 V; $C_L = 50$ pF; for load circuit see Figure 6.

Symbol	Parameter	Conditions			25 °C		-40 °C to	+125 °C	Unit
				Min	Тур	Max	Max (85 °C)	Max (125 °C)	
C_{PD}	power dissipation capacitance	per package; $V_I = GND$ to V_{CC}	[3]	-	15	-	-	-	pF
74HCT30	0								
t _{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see Figure 5	[1]						
		V _{CC} = 4.5 V		-	16	28	35	42	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	12	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Figure 5</u>	[2]	-	7	15	19	22	ns
C_{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} – 1.5 V	[3]	-	15	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum \left(C_L \times V_{CC}{}^2 \times f_o \right)$ where:

f_i = input frequency in MHz;

 f_o = output frequency in MHz;

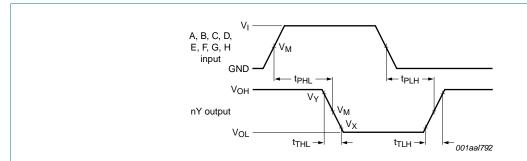
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

11. Waveforms



Measurement points are given in Table 8.

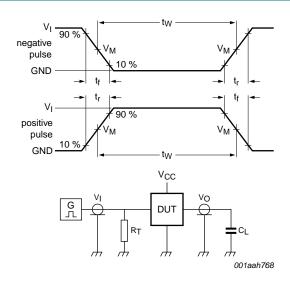
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output		
	V _M	V _M	V _X	V _Y
74HC30	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}
74HCT30	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}

74HC_HCT30



Test data is given in Table 9.

Definitions for test circuit:

 R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig 6. Test circuit for measuring switching times

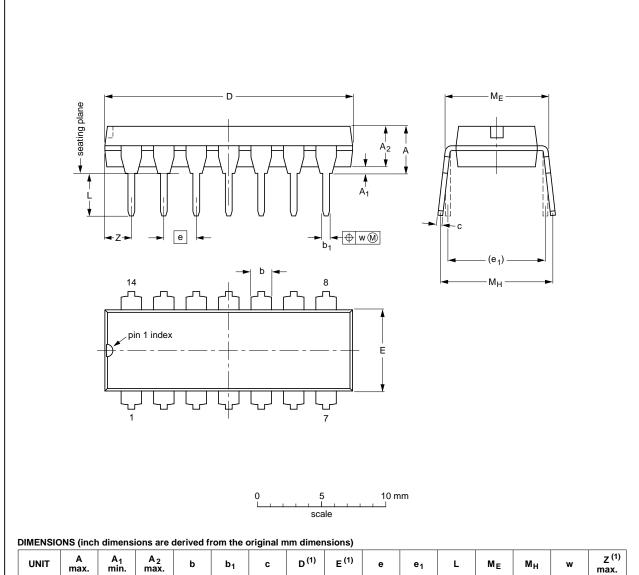
Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC30	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT30	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT27-1	050G04	MO-001	SC-501-14		99-12-27 03-02-13

Fig 7. Package outline SOT27-1 (DIP14)

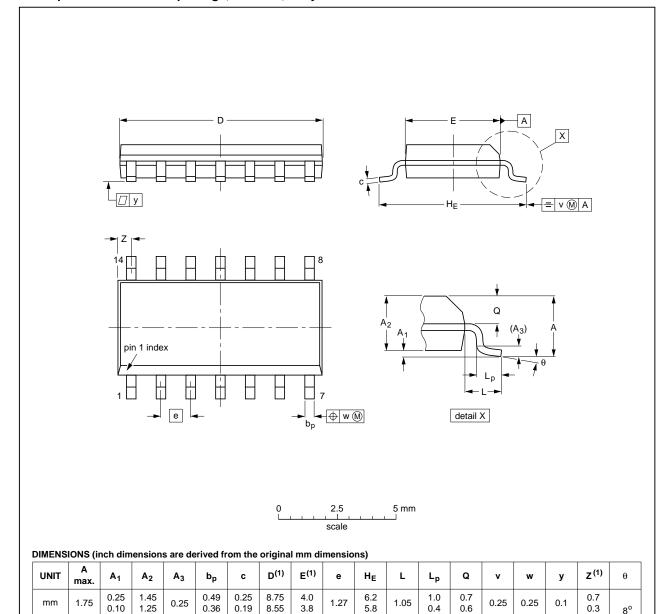
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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

inches

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.019 0.0100

0.014 0.0075

0.35

0.34

0.16

0.15

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012			99-12-27 03-02-19

0.05

0.244

0.228

0.041

0.039

0.016

0.028

0.024

0.01

0.01

Fig 8. Package outline SOT108-1 (SO14)

0.010

0.004

0.069

0.057

0.049

0.01

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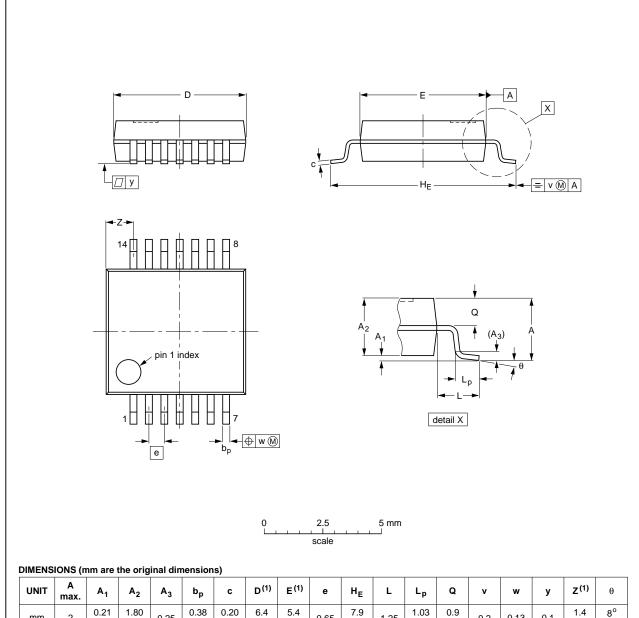
0°

0.028

0.004

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

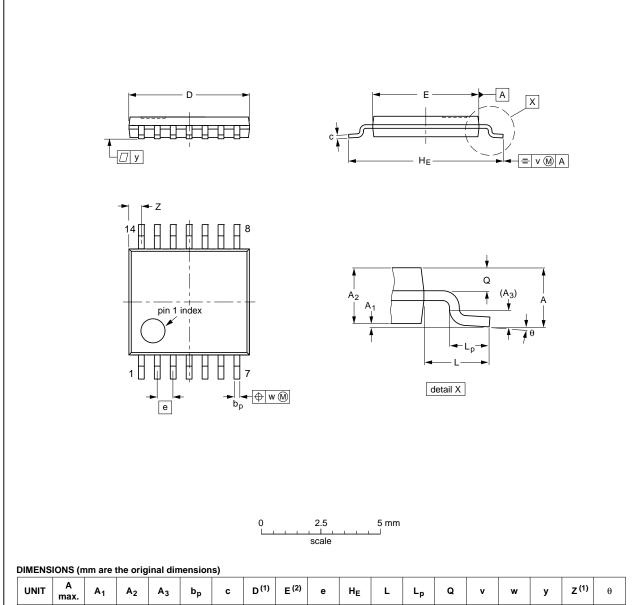
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT337-1		MO-150				-99-12-27 03-02-19

Fig 9. Package outline SOT337-1 (SSOP14)

74HC_HCT30

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

VERSION IEC JEDEC JEITA PROJECTION 99-12-2	OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
SO(402-1)	VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
03-02-	SOT402-1		MO-153			99-12-27 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT30 v.6	20121227	Product data sheet	-	74HC_HCT30 v.5
Modifications:	 New general 	al description.		
74HC_HCT30 v.5	20111213	Product data sheet	-	74HC_HCT30 v.4
Modifications:	 Legal page 	s updated.		
74HC_HCT30 v.4	20100504	Product data sheet	-	74HC_HCT30 v.3
74HC_HCT30 v.3	20100420	Product data sheet	-	74HC_HCT30 v.2
74HC_HCT30 v.2	19970829	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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