

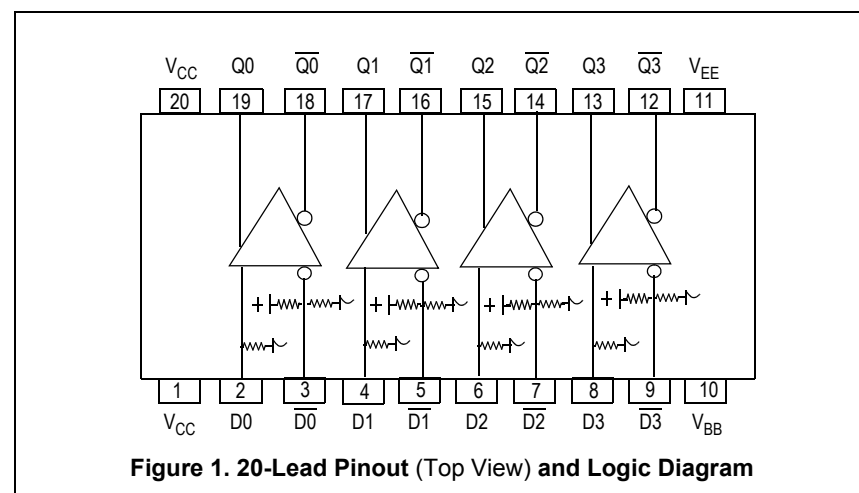
## 3.3 V ECL/PECL Quad Differential Receiver

The MC100ES6017 is a 3.3 V ECL/PECL quad differential receiver. Under open input conditions, the  $\bar{D}$  input will be biased at  $V_{CC}/2$  and the D input will be pulled down to  $V_{EE}$ . This operation will force the Q output LOW and ensure stability.

For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### Features

- High bandwidth output transitions
- LVPECL operating range:  $V_{CC} = 3.0$  V to 3.6 V
- Internal input pulldown resistors on D inputs, pullup and pulldown resistors on  $\bar{D}$  inputs
- 20 lead SOIC package
- Ambient temperature range -40°C to +85°C
- 20-lead Pb-free package available



**MC100ES6017**

**ECL/PECL QUAD  
DIFFERENTIAL RECEIVER**



**DW SUFFIX  
20-LEAD SOIC PACKAGE  
CASE 751D-07**



**EG SUFFIX  
20-LEAD SOIC PACKAGE  
Pb-FREE PACKAGE  
CASE 751D-07**

### ORDERING INFORMATION

Device	Package
MC100ES6017DW	SO-20
MC100ES6017DWR2	SO-20
MC100ES6017EG	SO-20 (Pb-Free)
MC100ES6017EGR2	SO-20 (Pb-Free)

### PIN DESCRIPTION

Pin	Function
$D_n, \bar{D}_n$	ECL Differential Data Inputs
$Q_n, \bar{Q}_n$	ECL Differential Data Outputs
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

**Table 1. General Specifications**

Characteristics		Value
Internal Input Pulldown Resistor		75 k $\Omega$
Internal Input Pullup Resistor		75 k $\Omega$
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2000 V > 200 V > 1500 V
$\theta_{JA}$ Thermal Resistance (Junction to Ambient)	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	90 °C/W 60 °C/W
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

**Table 2. Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Parameter	Conditions	Rating	Unit
V <sub>SUPPLY</sub>	Power Supply Voltage	difference between V <sub>CC</sub> & V <sub>EE</sub>	3.9	V
V <sub>IN</sub>	Input Voltage	V <sub>CC</sub> - V <sub>EE</sub> $\leq$ 3.6 V	V <sub>CC</sub> + 0.3 V <sub>EE</sub> - 0.3	V V
I <sub>OUT</sub>	Output Current	Continuous Surge	50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source		$\pm$ 0.5	mA
TA	Operating Temp Range		-40 to +85	°C
T <sub>STG</sub>	Storage Temp Range		-65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 3. DC Characteristics** (V<sub>CC</sub> = 3.0 to 3.6 V; V<sub>EE</sub> = 0 V or V<sub>CC</sub> = 0 V; V<sub>EE</sub> = -3.6 to -3.0 V)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		20	31		28	35	mA
V <sub>OH</sub> <sup>(1)</sup>	Output HIGH Voltage	V <sub>CC</sub> - 1150	V <sub>CC</sub> - 1020	V <sub>CC</sub> - 800	V <sub>CC</sub> - 1200	V <sub>CC</sub> - 970	V <sub>CC</sub> - 750	mV
V <sub>OL</sub> <sup>(1)</sup>	Output LOW Voltage	V <sub>CC</sub> - 1950	V <sub>CC</sub> - 1620	V <sub>CC</sub> - 1250	V <sub>CC</sub> - 2000	V <sub>CC</sub> - 1680	V <sub>CC</sub> - 1300	mV
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> - 1165		V <sub>CC</sub> - 880	V <sub>CC</sub> - 1165		V <sub>CC</sub> - 880	mV
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> - 1810		V <sub>CC</sub> - 1475	V <sub>CC</sub> - 1810		V <sub>CC</sub> - 1475	mV
V <sub>BB</sub> <sup>(2)</sup>	Output Voltage Reference (I <sub>BB</sub> = 0.5 mA)	V <sub>CC</sub> - 1440		V <sub>CC</sub> - 1235	V <sub>CC</sub> - 1440		V <sub>CC</sub> - 1235	mV
V <sub>PP</sub>	Differential Input Voltage	0.12		1.3	0.12		1.3	V
V <sub>CMR</sub>	Differential Cross Point Voltage	V <sub>EE</sub> + 1.3		V <sub>CC</sub> - 0.9	V <sub>EE</sub> + 1.3		V <sub>CC</sub> - 0.9	V
I <sub>IH</sub>	Input HIGH Current			150			150	$\mu$ A
I <sub>IL</sub>	Input LOW Current	$\frac{Dn}{Dn}$ 0.5 -300			0.5 -300			$\mu$ A $\mu$ A

1. Outputs are terminated through a 50 $\Omega$  resistor to V<sub>CC</sub>-2 volts.  
2. Input swing is centered around V<sub>BB</sub>.

**Table 4. AC Characteristics** ( $V_{CC} = 3.0$  to  $3.6$  V;  $V_{EE} = 0$  V or  $V_{CC} = 0$  V;  $V_{EE} = -3.6$  to  $-3.0$  V)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		1.75			1.75			1.75		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Diff S.E. <sup>(1)</sup>	310 225		510 595	310 225		510 595	310 225		510 595	ps
$t_{SKEW}$	Data Path Skew <sup>(2)</sup> (differential) Part-to-Part Skew <sup>(2)</sup> (differential) Pulse Width Skew <sup>(2)(3)</sup> (differential)			50 200 50			50 200 50			50 200 50	ps
$t_{JITTER}$	Cycle to Cycle Jitter			1			1			1	ps
$V_{PP}^{(4)}$	Input Swing	150		1000	150		1000	150		1000	mV
$t_r / t_f$	Output Rise/Fall Times (20% - 80%)	50		250	50		250	50		250	ps

1. Single-ended input propagation delay requires  $t_r$  and  $t_f \leq 350$  ps to meet specified propagation delay. Device will function with larger  $t_r$  and  $t_f$  values.
2. Skews are valid across specified voltage range, part-to-part skew is for a given temperature and frequency
3. Pulse width skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
4.  $V_{PP}$  (min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of approximately 40.

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Advanced Clock Drivers Device Data  
Freescale Semiconductor

## PACKAGE DIMENSIONS

### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

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TITLE: 20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE			DOCUMENT NO: 98ASB42343B		REV: J
			CASE NUMBER: 751D-07		23 MAR 2005
			STANDARD: JEDEC MS-013AC		

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**CASE 751D-07  
ISSUE J  
20-LEAD SOIC PACKAGE**

**MC100ES6017**

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