74ALVC541

Octal buffer/line driver; 3-state Rev. 3 — 20 January 2014

Product data sheet

1. **General description**

The 74ALVC541 is an octal non-inverting buffer/line drivers with 3-state bus compatible outputs. The 3-state outputs are controlled by the output enable inputs OE0 and OE1. A HIGH on $\overline{\text{OE}}$ n causes the outputs to assume a high-impedance OFF-state.

Features and benefits 2.

- Wide supply voltage range from 1.65 V to 3.6 V
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.5 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- 3.6 V tolerant inputs/outputs
- CMOS LOW power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V

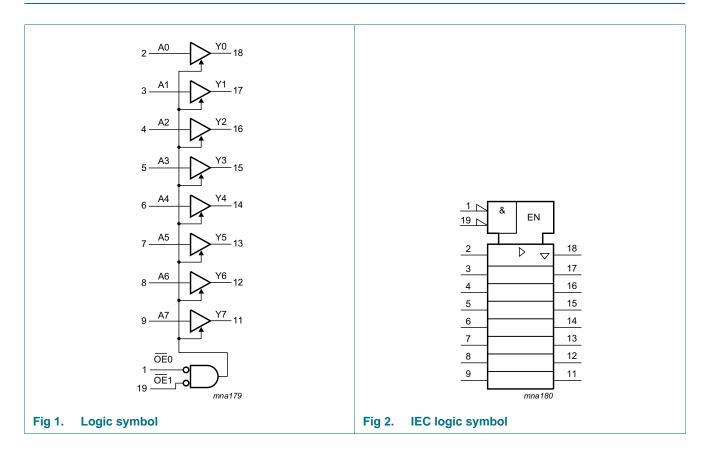
Ordering information

Table 1. **Ordering information**

Type number	Package								
	Temperature range	Name	Description	Version					
74ALVC541D	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1					
74ALVC541PW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1					
74ALVC541BQ	–40 °C to +85 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package no leads; 20 terminals; body $2.5\times4.5\times0.85$ mm	SOT764-1					

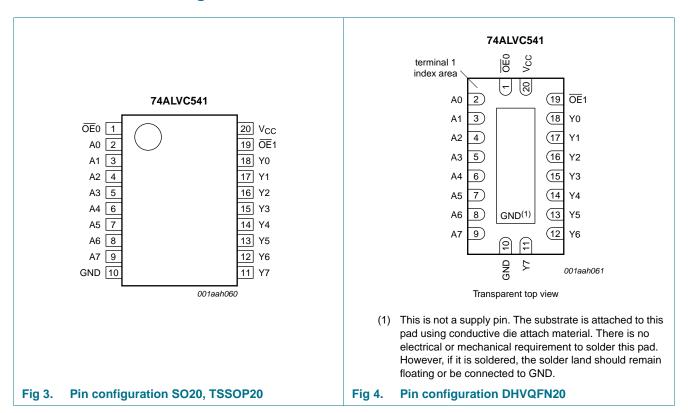


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE0	1	output enable input (active LOW)
A[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y[0:7]	18, 17, 16, 15, 14, 13, 12, 11	data output
OE1	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table[1]

Control		Input	Output
OE0	OE1	An	Yn
L	L	L	L
L	L	Н	Н
X	Н	X	Z
Н	X	X	Z

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
VI	input voltage			-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	[1]	-50	-	mA
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 V$		-	±50	mA
V _O	output voltage	output HIGH or LOW state	[2]	-0.5	$V_{CC} + 0.5$	V
		output 3-state	[2]	-0.5	+4.6	V
		power-down mode, V _{CC} = 0 V	[3]	-0.5	+4.6	V
I _O	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$				
	SO20 package		[4]	-	500	mW
	TSSOP20 package		[5]	-	500	mW
	DHVQFN20 package		[6]	-	500	mW

^[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

^[2] The output voltage ratings may be exceeded if the output current ratings are observed.

^[3] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 3.6 V in normal operation.

^[4] Ptot derates linearly with 8 mW/K above 70 °C.

^[5] Ptot derates linearly with 5.5 mW/K above 60 °C.

^[6] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	3.6	V
		power-down mode, $V_{CC} = 0 \text{ V}$	0	3.6	V
T _{amb}	ambient temperature		-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -$	-40 °C to	o +85 °C	Unit
			Min	Typ[1]	Max	
V_{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V _{CC} = 2.3 V to 2.7V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V _{IL} LOW-le	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100 \mu A$; $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	ςXX-0.2	-	-	V
		$I_{O} = 6mA$; $V_{CC} = 1.65 V$	1.25	-	-	V
		I_{O} = 12 mA; V_{CC} = 2.3 V	1.8	-	-	V
		I_{O} = 18 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_{O} = 12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		$I_{O} = 18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	V
		$I_{O} = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_{O} = -100 \ \mu A; \ V_{CC} = 1.65 \ V \ to \ 3.6 \ V$	-	-	0.2	V
		$I_{O} = -6mA$; $V_{CC} = 1.65 V$	-	-	0.3	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.4	V
		$I_{O} = -18 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	V
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.4	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	V
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 3.6 \text{ V}$	-	±0.1	±10.0	μА

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Octal buffer/line driver; 3-state

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} =	Unit		
			Min	Typ[1]	Max	
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 3.6 \text{ V}$	-	±0.1	±5.0	μΑ
I _{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	±0.1	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 3.6$ V	-	0.2	10	μΑ
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A;	-	5	750	μΑ
C _I	input capacitance		-	3.5	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V and Tamb = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		T _{aml}	_b = -40 °C to	+85 °C	Unit
					Typ[1]	Max	
t _{pd}	propagation	An to Yn; see Figure 5	[2]				·
	delay	$V_{CC} = 1.65V$ to 1.95 V		1.0	3.0	4.6	ns
		$V_{CC} = 2.3V \text{ to } 2.7 \text{ V}$		1.0	2.2	3.3	ns
		V _{CC} = 27 V		1.0	2.5	3.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.3	3.0	ns
t _{en}	enable time	OEn to Yn; see Figure 6	[2]				
		$V_{CC} = 1.65V \text{ to } 1.95 \text{ V}$		1.0	4.2	7.5	ns
		$V_{CC} = 2.3 V \text{ to } 2.7 V$		1.0	3.3	5.4	ns
		V _{CC} = 27 V		1.0	3.7	5.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	3.3	4.9	ns
t _{dis}	disable time	OEn to Yn; see Figure 6	[2]				
		$V_{CC} = 1.65V \text{ to } 1.95 \text{ V}$		1.0	4.8	7.5	ns
		$V_{CC} = 2.3 V \text{ to } 2.7 V$		1.0	3.1	4.5	ns
		V _{CC} = 27 V		1.0	3.1	4.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.9	4.6	ns

Octal buffer/line driver; 3-state

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	T _{aml}	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$			
			Min	Typ[1]	Max		
C _{PD} power		per buffer; $V_I = GND$ to V_{CC} ; $V_{CC} = 3.3 \text{ V}$					
	dissipation capacitance	outputs enabled	-	25	-	pF	
	capacitarice	outputs disabled	-	0	-	pF	

- [1] All typical values are measured at Tamb = 25 $^{\circ}$ C and V_{CC} = 1.8 V, 2.5 V, 2.7 V and 3.3 V.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .

 t_{en} is the same as t_{PZL} and $t_{\text{PZH}}.$

 t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$

f_i = input frequency in MHz;

 f_o = output frequency in MHz;

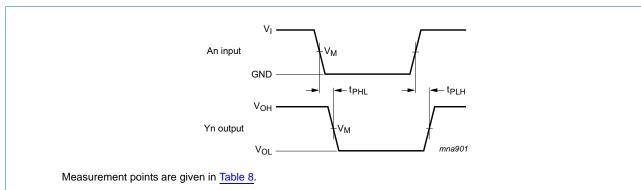
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

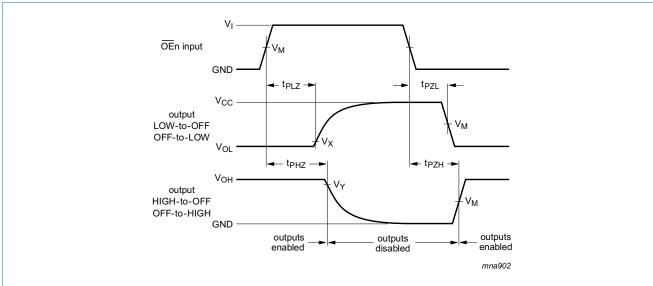
11. Waveforms



 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (An) to output (Yn)

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Measurement points are given in Table 8.

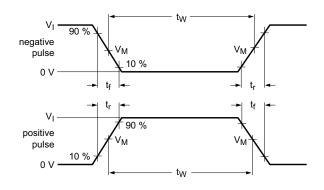
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

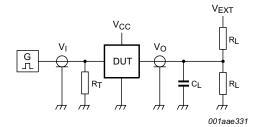
Fig 6. Enable and disable times

Table 8. Measurement points

Supply voltage	e Input			Output			
V _{CC}	VI	V _M	V _M	V _X	V _Y		
1.65 V to 1.65V	V _{CC}	$0.5 \times V_{\text{CC}}$	$0.5 \times V_{CC}$	V _{OL} + 0.15 V	$V_{OH} - 0.15 V$		
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{\text{CC}}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH}-0.15\ V$		
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	$V_{OH}-0.3\ V$		
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	$V_{OH} - 0.3 V$		

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Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

Fig 7. Test circuit for measuring switching times

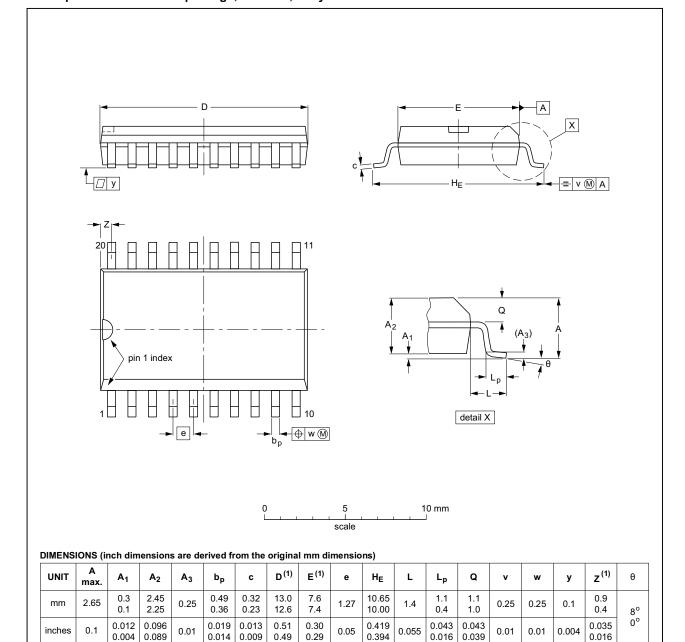
Table 9. Test data

Supply voltage	Input	Input		d V _{EXT}			Load		
V _{CC}	VI	t _r , t _f	CL	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}		
1.65 V to 1.95 V	V_{CC}	\leq 2.0 ns	30 pF	1 kΩ	open	$2\times V_{CC}$	GND		
2.3 V to 2.7 V	V_{CC}	\leq 2.0 ns	30 pF	$500~\Omega$	open	$2\times V_{CC}$	GND		
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6	GND		
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500Ω	open	6	GND		

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Fig 8. Package outline SOT163-1 (SO20)

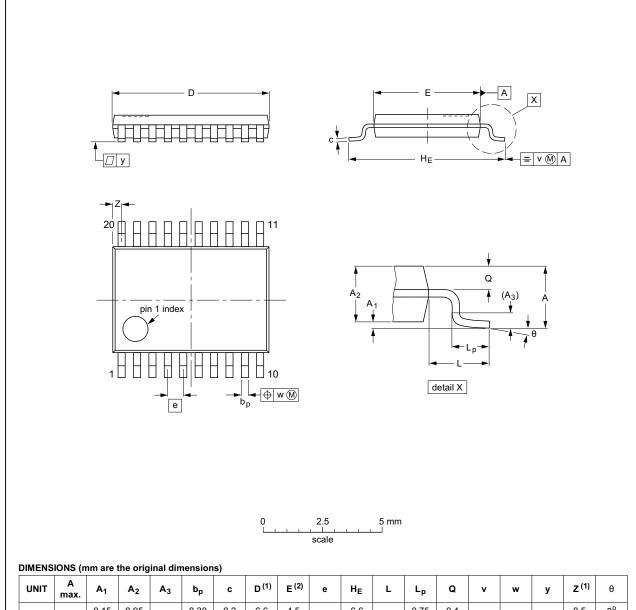
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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	٧	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

		EUROPEAN	ISSUE DATE			
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
	MO-153				99-12-27 03-02-19	
_	IEC				IEC JEDEC JEHA	

Package outline SOT360-1 (TSSOP20) Fig 9.

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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm SOT764-1

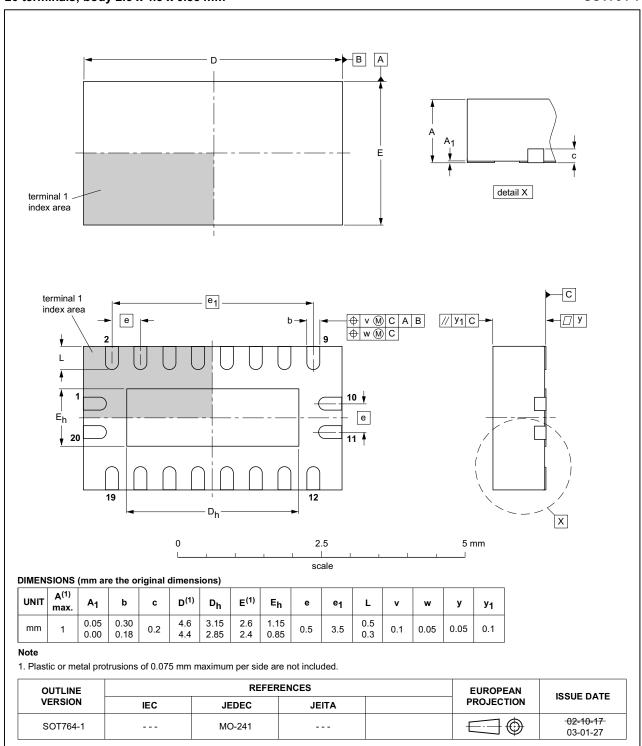


Fig 10. Package outline SOT764-1 (DHVQFN20)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description			
CDM	Charge Device Model			
CMOS	Complementary Metal Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			
MM	Machine Model			
TTL	Transistor-Transistor Logic			

14. Revision history

Table 11. Revision history

Document ID Release date		Data sheet status	Change notice	Supersedes					
74ALVC541 v.3	20140120	Product data sheet	-	74ALVC541 v.2					
	 The format of to of NXP Semicon 		designed to comply with	the new identity guidelines					
	 Legal texts have been adapted to the new company name where appropriate. 								
74ALVC541 v.2	20071210	Product data sheet	-	74ALVC541 v.1					
74ALVC541 v.1	20021115	Product specification	-	-					

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.