74LVC126A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

Rev. 8 — 8 April 2014

Product data sheet

1. General description

The 74LVC126A consists of four non-inverting buffers/line drivers with 3-state outputs, which are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

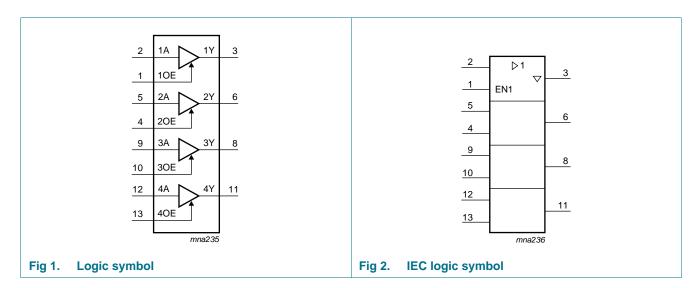
Table 1. Ordering information

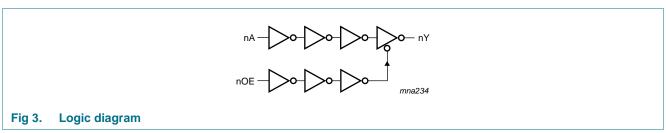
Type number	Package	Package										
	Temperature range	Name	Description	Version								
74LVC126AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1								
74LVC126ADB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1								
74LVC126APW	–40 °C to +125 °C	TSSOP14	plastic thin small outline package; 14 leads; body width 4.4 mm	SOT402-1								
74LVC126ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1								



Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

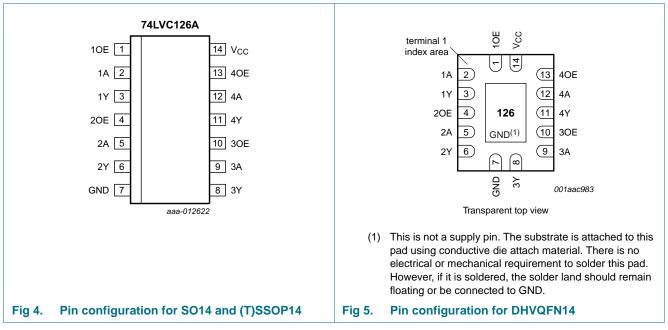
4. Functional diagram





5. Pinning information

5.1 Pinning



74LVC126A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
10E	1	data enable input (active HIGH)
1A	2	data input
1Y	3	data output
20E	4	data enable input (active HIGH)
2A	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
30E	10	data enable input (active HIGH)
4Y	11	data output
4A	12	data input
40E	13	data enable input (active HIGH)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection[1]

Inputs nOE		Output
nOE	nA	nY
Н	L	L
Н	Н	Н
L	X	Z

^[1] H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
Vo	output voltage	output HIGH or LOW-state	-0.5	V _{CC} + 0.5	V
		output 3-state [2]	-0.5	+6.5	V
Io	output current	$V_O = 0 \text{ V to } V_{CC}$	-	±50	mA

74LVC126A

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3 of 16

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature	[3]	-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	-	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
- [2] The output voltage ratings may be exceeded if the output current ratings are observed.
- [3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
Vo		output 3-state	0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
	and fall rate	V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	–40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

 Table 6.
 Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	35 °C	–40 °C t	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	V _{CC} – 0.2	-	-	V _{CC} - 0.3	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
	$I_0 = -24 \text{ mA}; V_{CO}$		2.2	-	-	2.0	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
l _l	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 3.6$ V; $V_O = 5.5$ V or GND;	-	±0.1	±5	-	±20	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_1 \text{ or } V_0 = 5.5 \text{ V}$	-	±0.1	±10	-	±20	μΑ
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.1	10	-	40	μА
Δl _{CC}	additional supply current	per input pin; $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V;}$ $V_{I} = V_{CC} - 0.6 \text{ V; } I_{O} = 0 \text{ A}$	-	5	500	-	5000	μΑ
C _I	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$	-	4.0	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

10. Dynamic characteristics

Table 7. Dynamic characteristics

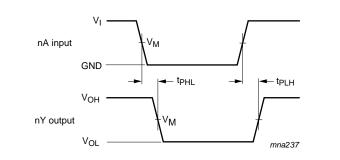
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 6	[2]						
		V _{CC} = 1.2 V		-	11.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		1.5	5.2	10.8	1.5	12.6	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.0	2.8	5.6	1.0	6.6	ns
		V _{CC} = 2.7 V		1.5	2.7	5.2	1.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	2.4	4.7	1.0	6.0	ns
t _{en}	enable time	nOE to nY; see Figure 7	[2]						
		V _{CC} = 1.2 V		-	15.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		2.4	6.7	12.9	2.4	15.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2.0	3.8	7.1	2.0	8.3	ns
		V _{CC} = 2.7 V		1.5	3.1	6.3	1.5	8.0	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	3.1	5.7	1.0	7.5	ns
t _{dis}	disable time	nOE to nY; see Figure 7	[2]						
		V _{CC} = 1.2 V		-	8.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		1.0	3.3	10.0	1.0	11.5	ns
		V _{CC} = 2.3 V to 2.7 V		0.5	1.8	5.6	0.5	6.5	ns
		V _{CC} = 2.7 V		1.5	3.4	6.7	1.5	8.5	ns
		V _{CC} = 3.0 V to 3.6 V		1.3	2.5	6.0	1.3	7.5	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation	per buffer; $V_I = GND$ to V_{CC}	<u>[4]</u>						
	capacitance	V _{CC} = 1.65 V to 1.95 V		-	6.0	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V		-	9.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V		-	12.2	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
 - ten is the same as tPZL and tPZH.
 - t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 - $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$
 - f_i = input frequency in MHz; f_o = output frequency in MHz
 - C_L = output load capacitance in pF
 - V_{CC} = supply voltage in Volts
 - N = number of inputs switching
 - $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

11. AC waveforms

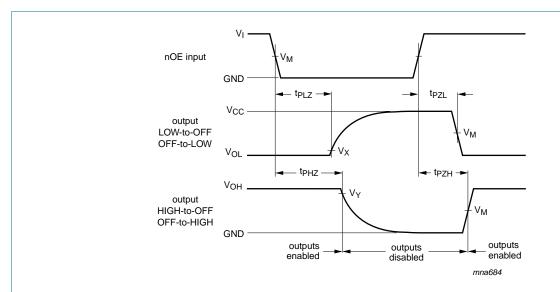


 $V_{M} = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V};$

 V_{M} = 0.5 $\,\times\,V_{CC}$ at V_{CC} < 2.7 V;

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The input nA to output nY propagation delays



Measurement points are given in Table 8.

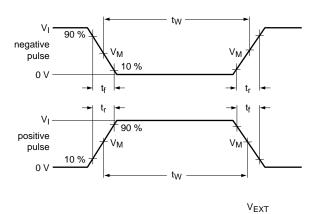
 $\ensuremath{V_{\text{OL}}}$ and $\ensuremath{V_{\text{OH}}}$ are typical output voltage levels that occur with the output load.

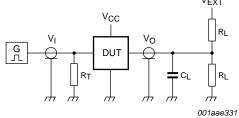
Fig 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output								
V _{CC}	V _M	V _M	V _X	V _Y						
V _{CC} < 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{OL} + 0.15 V	V _{OH} – 0.15 V						
$V_{CC} \ge 2.7 \text{ V}$	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} – 0.3 V						

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state





Test data is given in Table 9.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

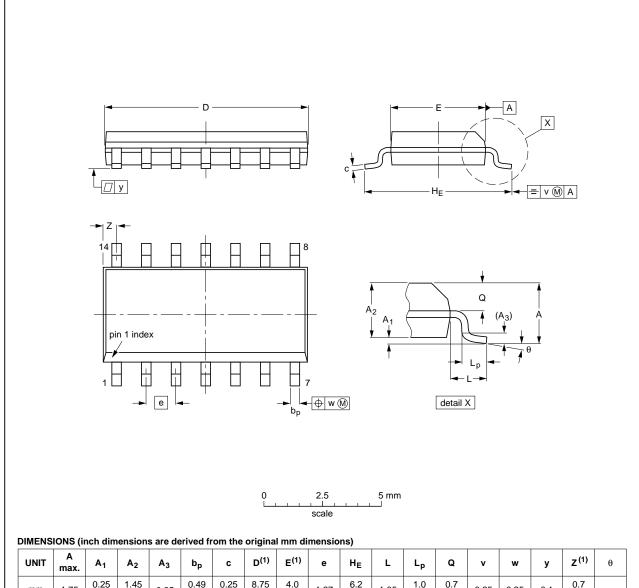
Supply voltage			Load		V _{EXT}			
	VI	t _r , t _f	CL	R_L	t _{PLH} , t _{PHL}	t_{PLZ}, t_{PZL}	t _{PHZ} , t _{PZH}	
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2\times V_{CC}$	GND	
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2\times V_{CC}$	GND	
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	$2\times V_{CC}$	GND	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND	

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	l	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Fig 9. Package outline SOT108-1 (SO14)

74LVC126A

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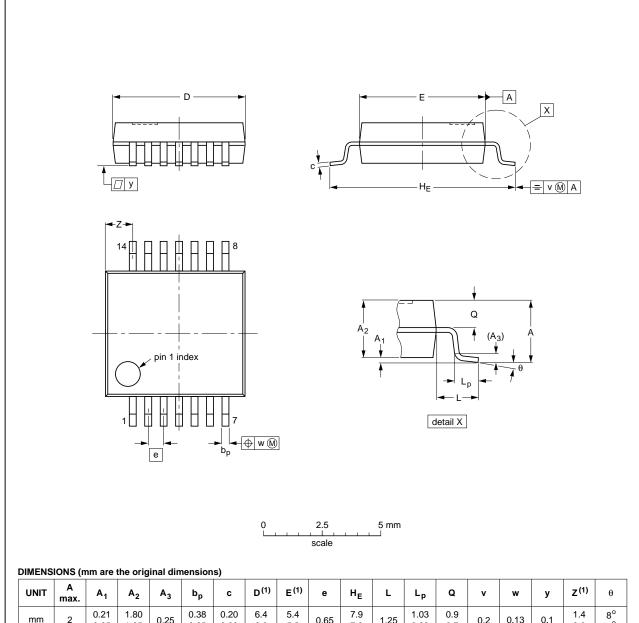
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74LVC126A **NXP Semiconductors**

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



-							-,												
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT337-1		MO-150			-99-12-27 03-02-19	

Fig 10. Package outline SOT337-1 (SSOP14)

74LVC126A

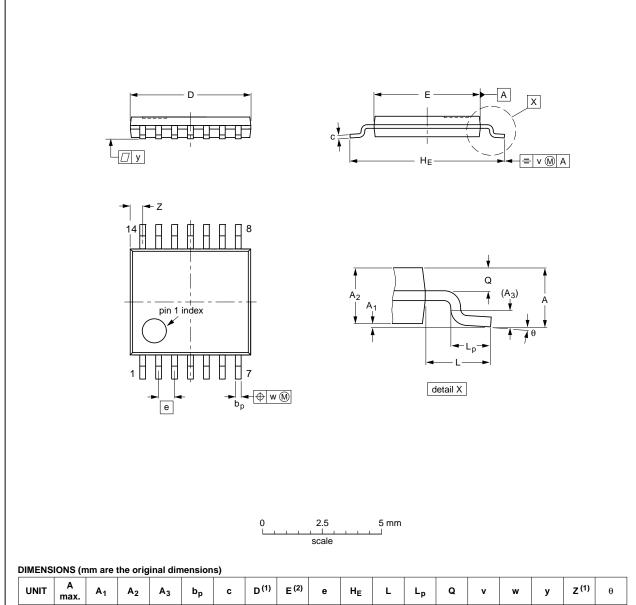
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Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	C	D ⁽¹⁾	E (2)	e	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT402-1		MO-153			99-12-27 03-02-18
				·	

Fig 11. Package outline SOT402-1 (TSSOP14)

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Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

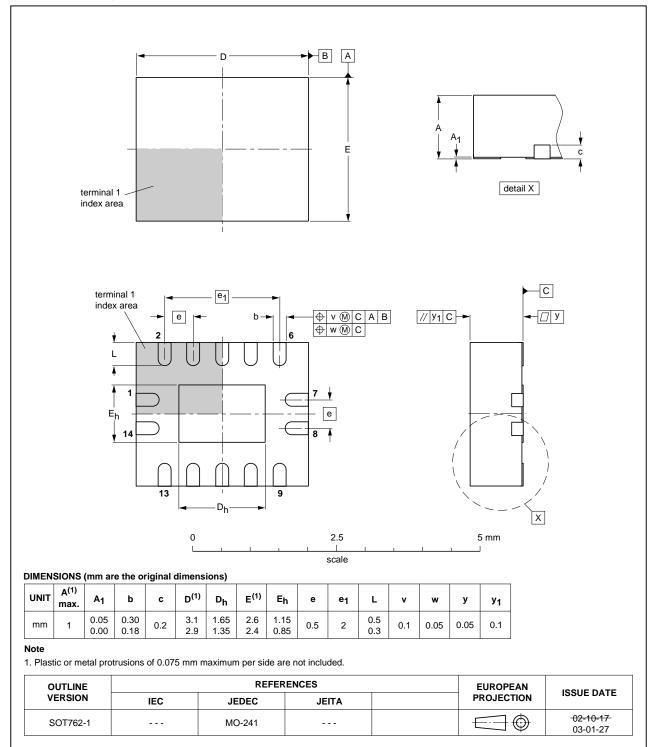


Fig 12. Package outline SOT762-1 (DHVQFN14)

74LVC126A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Release date	Data sheet status	Change notice	Supersedes
20140408	Product data sheet	-	74LVC126A v.7
 Legal pages update 	d.		
20111209	Product data sheet	-	74LVC126A v.6
 Legal pages update 	d.		
20110926	Product data sheet	-	74LVC126A v.5
20030228	Product specification	-	74LVC126A v.4
20020308	Product specification	-	74LVC126A v.3
19980428	Product specification	-	74LVC126A v.2
19970801	Product specification	-	74LVC126A v.1
-	-	-	-
	20140408 • Legal pages update 20111209 • Legal pages update 20110926 20030228 20020308 19980428	20140408 Product data sheet • Legal pages updated. 20111209 Product data sheet • Legal pages updated. 20110926 Product data sheet 20030228 Product specification 20020308 Product specification 19980428 Product specification	20140408 Product data sheet - Legal pages updated. 20111209 Product data sheet - Legal pages updated. 20110926 Product data sheet - 20030228 Product specification - 20020308 Product specification - 19980428 Product specification -

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

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17. Contents

1	General description 1
2	Features and benefits 1
3	Ordering information 1
4	Functional diagram 2
5	Pinning information
5.1	Pinning
5.2	Pin description
6	Functional description 3
7	Limiting values
8	Recommended operating conditions 4
9	Static characteristics 4
10	Dynamic characteristics 6
11	AC waveforms 7
12	Package outline 9
13	Abbreviations
14	Revision history
15	Legal information14
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks
16	Contact information
17	Contents

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