

74LVC1G125-Q100

Bus buffer/line driver; 3-state

Rev. 1 — 9 July 2012

Product data sheet

1. General description

The 74LVC1G125-Q100 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (\overline{OE}). A HIGH-level at pin \overline{OE} causes the output to assume a high-impedance OFF-state.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- $\pm 24\text{ mA}$ output drive ($V_{CC} = 3.0\text{ V}$)
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pf}$, $R = 0\text{ }\Omega$)
- CMOS low power consumption
- Inputs accept voltages up to 5 V
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC1G125GW-Q100	−40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G125GV-Q100	−40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G125GW-Q100	VM
74LVC1G125GV-Q100	V25

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

Fig 1. Logic symbol

Fig 2. IEC logic symbol

Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

74LVC1G125-Q100

Fig 4. Pin configuration SOT353-1 and SOT753

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
\overline{OE}	1	output enable input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
\overline{OE}	A	Y
L	L	L
L	H	H
H	X	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode	^{[1][2]} -0.5	V _{CC} + 0.5	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	250	mW
T _{stg}	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.
 [3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40$ °C to $+85$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 1.65$ V to 5.5 V; $I_O = 100$ μ A	-	-	0.1	V
		$V_{CC} = 1.65$ V; $I_O = 4$ mA	-	-	0.45	V
		$V_{CC} = 2.3$ V; $I_O = 8$ mA	-	-	0.3	V
		$V_{CC} = 2.7$ V; $I_O = 12$ mA	-	-	0.4	V
		$V_{CC} = 3.0$ V; $I_O = 24$ mA	-	-	0.55	V
		$V_{CC} = 4.5$ V; $I_O = 32$ mA	-	-	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 1.65$ V to 5.5 V; $I_O = -100$ μ A	$V_{CC} - 0.1$	-	-	V
		$V_{CC} = 1.65$ V; $I_O = -4$ mA	1.2	-	-	V
		$V_{CC} = 2.3$ V; $I_O = -8$ mA	1.9	-	-	V
		$V_{CC} = 2.7$ V; $I_O = -12$ mA	2.2	-	-	V
		$V_{CC} = 3.0$ V; $I_O = -24$ mA	2.3	-	-	V
		$V_{CC} = 4.5$ V; $I_O = -32$ mA	3.8	-	-	V
I_I	input leakage current	$V_{CC} = 0$ V to 5.5 V; $V_I = 5.5$ V or GND	-	± 0.1	± 5	μ A
I_{OZ}	OFF-state output current	$V_{CC} = 3.6$ V; $V_I = V_{IH}$ or V_{IL} ; $V_O = 5.5$ V or GND	-	± 0.1	± 10	μ A

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 5.5\text{ V}$	-	± 0.1	± 10	μA
I_{CC}	supply current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 1.65\text{ V}$ to 5.5 V ; $I_O = 0\text{ A}$	-	0.1	10	μA
ΔI_{CC}	additional supply current	per pin; $V_{CC} = 2.3\text{ V}$ to 5.5 V ; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	500	μA
C_I	input capacitance		-	5	-	pF
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V}$ to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 1.65\text{ V}$ to 5.5 V ; $I_O = 100\text{ }\mu\text{A}$	-	-	0.1	V
		$V_{CC} = 1.65\text{ V}$; $I_O = 4\text{ mA}$	-	-	0.70	V
		$V_{CC} = 2.3\text{ V}$; $I_O = 8\text{ mA}$	-	-	0.45	V
		$V_{CC} = 2.7\text{ V}$; $I_O = 12\text{ mA}$	-	-	0.60	V
		$V_{CC} = 3.0\text{ V}$; $I_O = 24\text{ mA}$	-	-	0.80	V
		$V_{CC} = 4.5\text{ V}$; $I_O = 32\text{ mA}$	-	-	0.80	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 1.65\text{ V}$ to 5.5 V ; $I_O = -100\text{ }\mu\text{A}$	$V_{CC} - 0.1$	-	-	V
		$V_{CC} = 1.65\text{ V}$; $I_O = -4\text{ mA}$	0.95	-	-	V
		$V_{CC} = 2.3\text{ V}$; $I_O = -8\text{ mA}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V}$; $I_O = -12\text{ mA}$	1.9	-	-	V
		$V_{CC} = 3.0\text{ V}$; $I_O = -24\text{ mA}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V}$; $I_O = -32\text{ mA}$	3.4	-	-	V
I_I	input leakage current	$V_{CC} = 0\text{ V}$ to 5.5 V ; $V_I = 5.5\text{ V}$ or GND	-	-	± 100	μA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $V_O = 5.5\text{ V}$ or GND	-	-	± 200	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 5.5\text{ V}$	-	-	± 200	μA
I_{CC}	supply current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 1.65\text{ V}$ to 5.5 V ; $I_O = 0\text{ A}$	-	-	200	μA
ΔI_{CC}	additional supply current	per pin; $V_{CC} = 2.3\text{ V}$ to 5.5 V ; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	-	5000	μA

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A to Y; see Figure 5 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.3	8.0	1.0	10.5	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	5.5	0.5	7	ns
		V _{CC} = 2.7 V	0.5	2.5	5.5	0.5	7	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.1	4.5	0.5	6	ns
t _{en}	enable time	OE to Y; see Figure 6 [3]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.1	9.4	1.0	12	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.8	6.6	0.5	8.5	ns
		V _{CC} = 2.7 V	0.5	3.3	6.6	0.5	8.5	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.4	5.3	0.5	7	ns
t _{dis}	disable time	OE to Y; see Figure 6 [4]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.3	9.2	1.0	12	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.7	5.0	0.5	6.5	ns
		V _{CC} = 2.7 V	0.5	3.0	5.0	0.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	3.1	5.0	0.5	6.5	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} [5]						
		output enabled	-	25	-	-	-	pF
		output disabled	-	6	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] t_{en} is the same as t_{PZH} and t_{PZL}

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

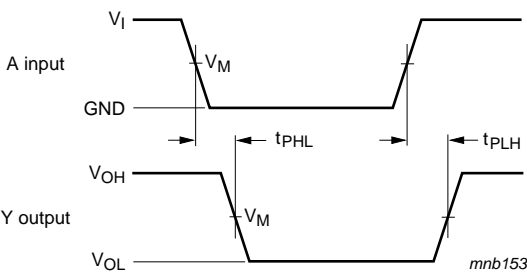
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

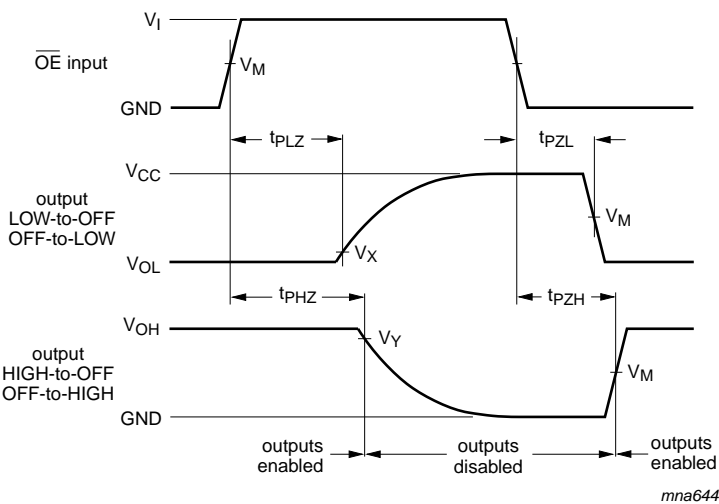
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Input A to output Y propagation delay times

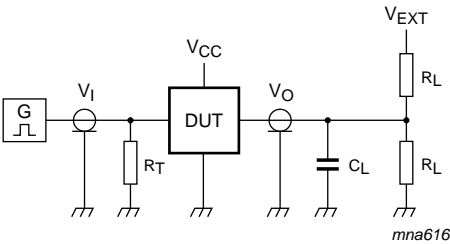


Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2V _{CC}
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2V _{CC}

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mmSOT353-1

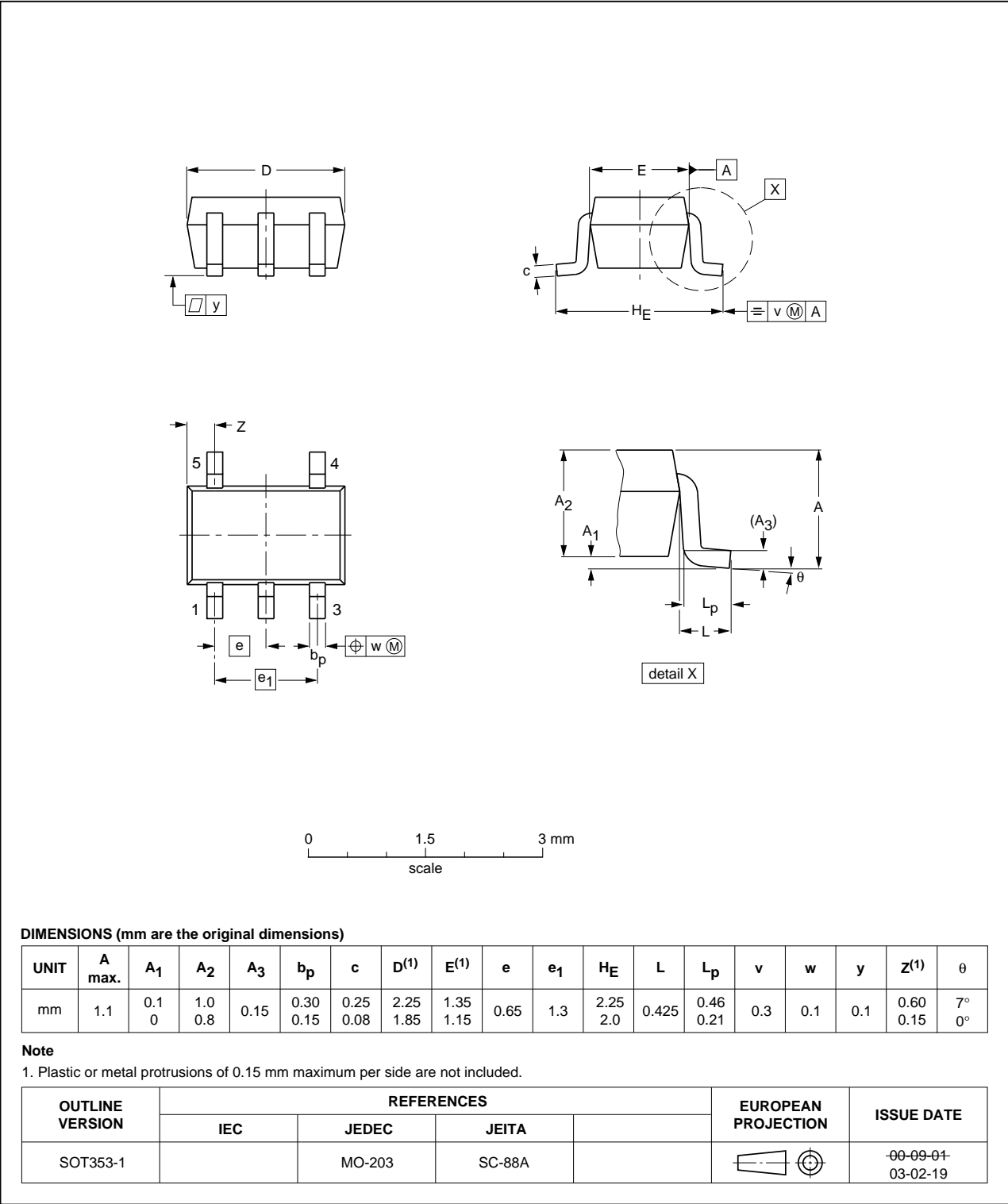


Fig 8. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

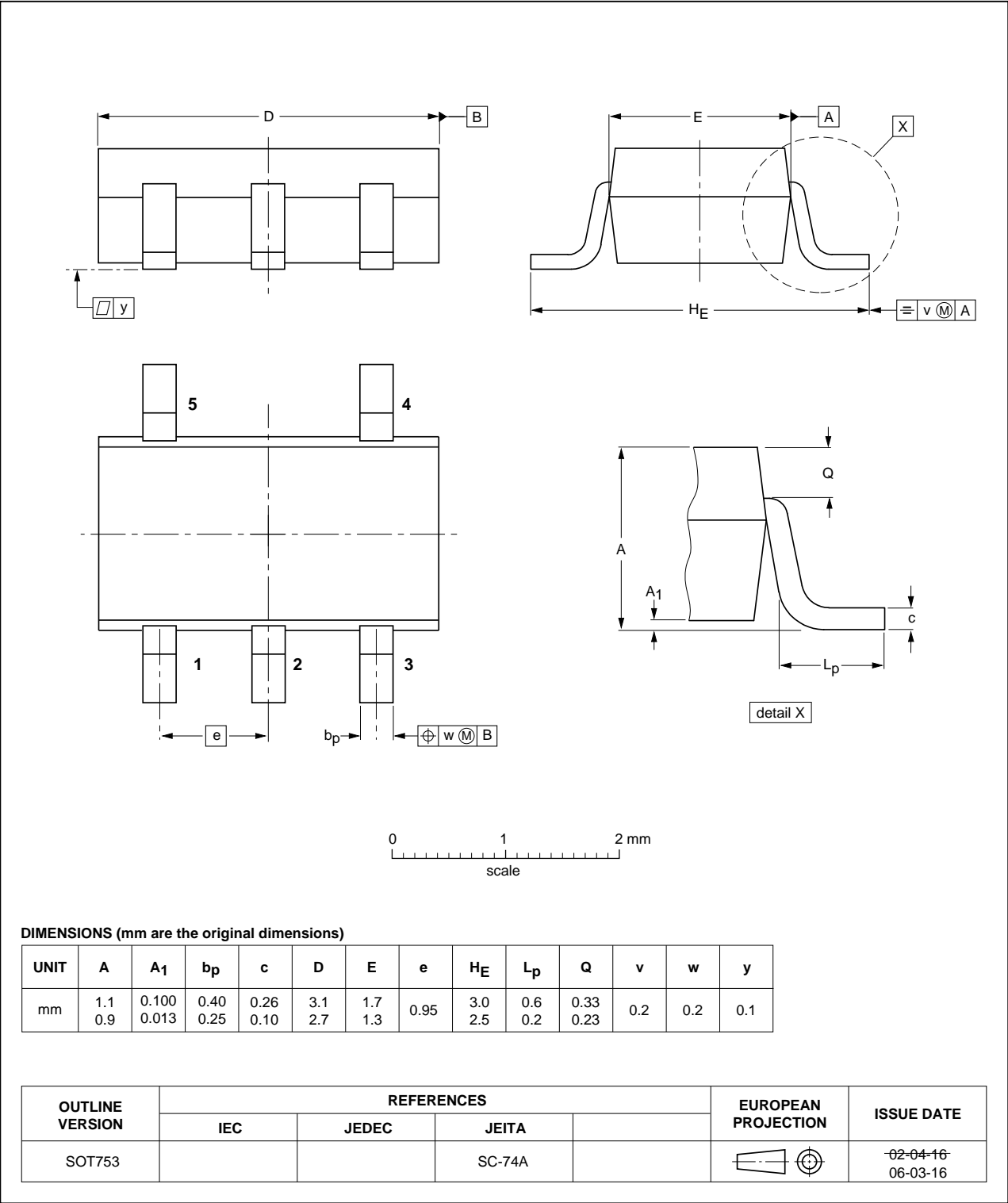


Fig 9. Package outline SOT753

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
MIL	Military

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G125_Q100 v.1	20120709	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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