

# 74VHC245FT

## 1. Functional Description

- Octal Bus Transceiver

## 2. General

The 74VHC245 is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ( $\overline{G}$ ) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

## 3. Features (Note)

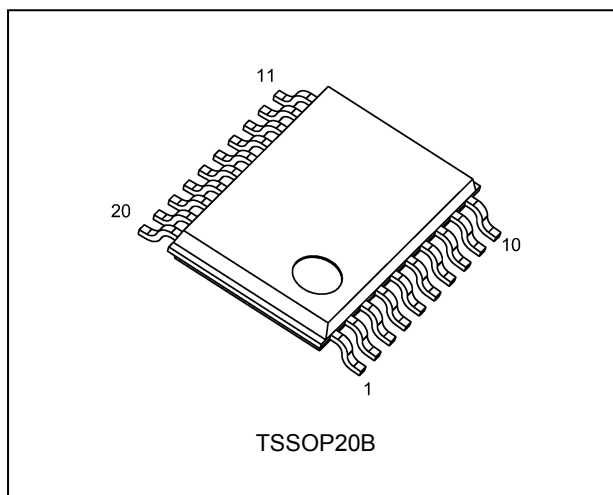
- (1) High speed: Propagation delay time = 4.0 ns (typ.) at  $V_{CC} = 5\text{ V}$
- (2) Low power dissipation:  $I_{CC} = 4\text{ }\mu\text{A}$  (max) at  $T_a = 25\text{ }^\circ\text{C}$
- (3) High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- (4) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (5) Wide operating voltage range:  $V_{CC(opr)} = 2\text{ V to } 5.5\text{ V}$
- (6) Low noise:  $V_{OLP} = 1.0\text{ V}$  (max)
- (7) Pin and function compatible with the 74 series (74AC/HC/AHC etc.) 245 type.

Note: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

A parasitic diode is formed between the bus and  $V_{CC}$  terminals. Therefore bus terminal can not be used to interface 5 V to 3 V systems directly.

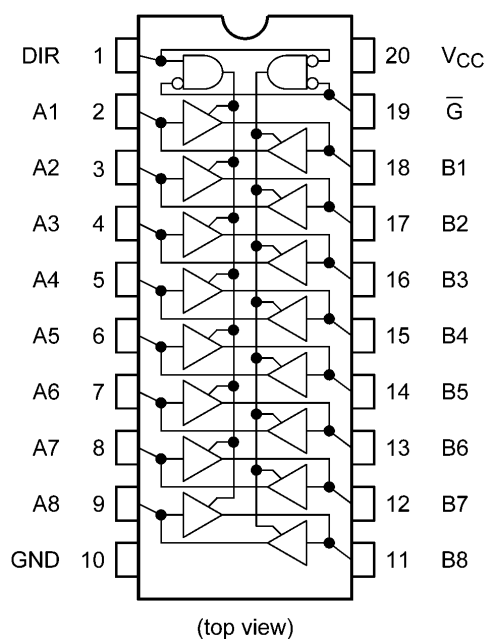
## 4. Packaging



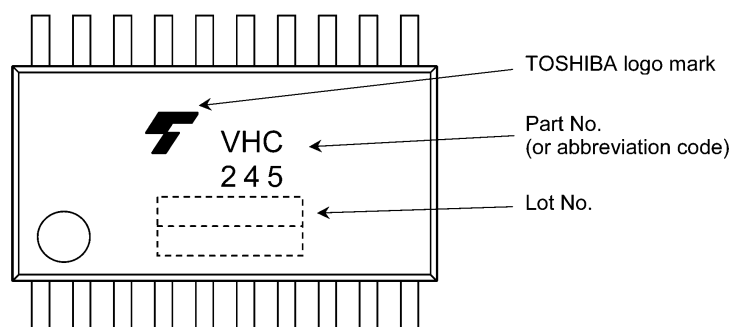
Start of commercial production

2013-04

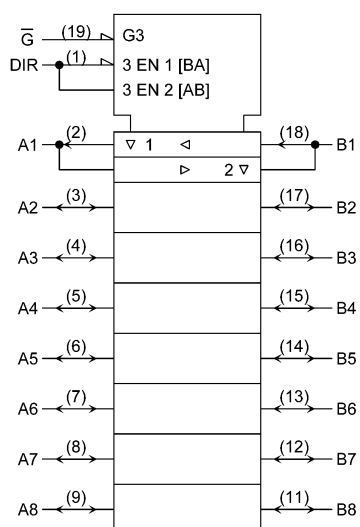
## 5. Pin Assignment



## 6. Marking



## 7. IEC Logic Symbol



## 8. Truth Table

Input $\overline{G}$	Input DIR	A BUS	B BUS	Output
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

X: Don't care

Z: High impedance

## 9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	-0.5 to 7.0	V
Input voltage(DIR, $\overline{G}$ )	$V_{IN}$	-0.5 to 7.0	V
Bus I/O voltage	$V_{I/O}$	-0.5 to $V_{CC}+0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
Output current	$I_{OUT}$	$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

## 10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage(DIR, $\overline{G}$ )	$V_{IN}$		0 to 5.5	V
Bus I/O voltage	$V_{I/O}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 85	°C
Input rise and fall times	dt/dv	$V_{CC}=3.3\pm 0.3$	0 to 100	ns/V
		$V_{CC}=5.0\pm 0.5$	0 to 20	

Note: The operating ranges are required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND. Please connect both bus inputs and the bus outputs with  $V_{CC}$  or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

## 11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.94	—	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } \text{GND}$		5.5	—	—	$\pm 0.25$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V or GND}$		0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or } \text{GND}$		5.5	—	—	4.0	$\mu\text{A}$

11.2. DC Characteristics (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
			$I_{OL} = 8\text{ mA}$	4.5	—	0.44	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } \text{GND}$		5.5	—	$\pm 2.50$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V or GND}$		0 to 5.5	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or } \text{GND}$		5.5	—	40.0	$\mu\text{A}$

### 11.3. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 3\text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	5.8	8.4	ns
					50	—	8.3	11.9	
				$5.0 \pm 0.5$	15	—	4.0	5.5	
					50	—	5.5	7.5	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	—	8.5	13.2	ns
					50	—	11.0	16.7	
				$5.0 \pm 0.5$	15	—	5.8	8.5	
					50	—	7.3	10.6	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	—	11.5	15.8	ns
				$5.0 \pm 0.5$	50	—	7.0	9.7	
Output skew	$t_{osLH}, t_{osHL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	—	1.5	ns
				$5.0 \pm 0.5$	50	—	—	1.0	
Input capacitance	$C_{IN}$		DIR, $\overline{G}$			—	4	10	pF
Bus I/O capacitance	$C_{I/O}$		$A_n, B_n$			—	8	—	pF
Power dissipation capacitance	$C_{PD}$	(Note 2)	—			—	21	—	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{osHL} = |t_{PHLm} - t_{PHLn}|$ )

Note 2:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per bit)}$$

### 11.4. AC Characteristics

(Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )

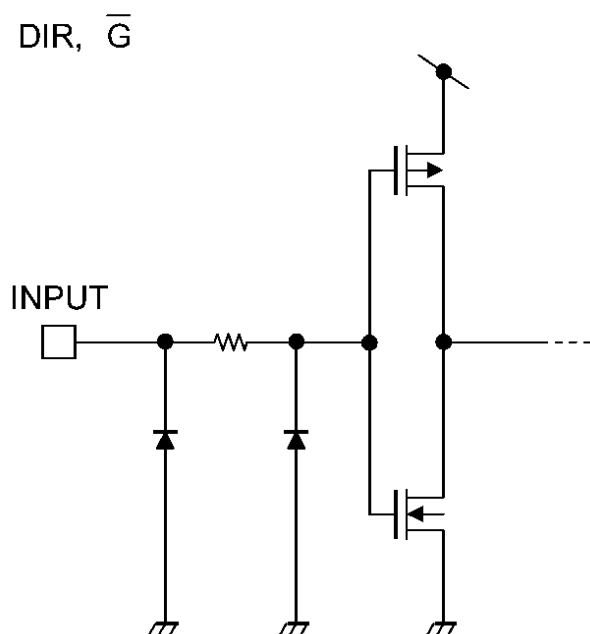
Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	10.0	ns
					50	1.0	13.5	
				$5.0 \pm 0.5$	15	1.0	6.5	
					50	1.0	8.5	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	1.0	15.5	ns
					50	1.0	19.0	
				$5.0 \pm 0.5$	15	1.0	10.0	
					50	1.0	12.0	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	1.0	18.0	ns
				$5.0 \pm 0.5$	50	1.0	11.0	
Output skew	$t_{osLH}, t_{osHL}$	(Note 1)	—	$5.0 \pm 0.5$	50	—	1.0	ns
Input capacitance	$C_{IN}$		DIR, $\overline{G}$			—	10	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{osHL} = |t_{PHLm} - t_{PHLn}|$ )

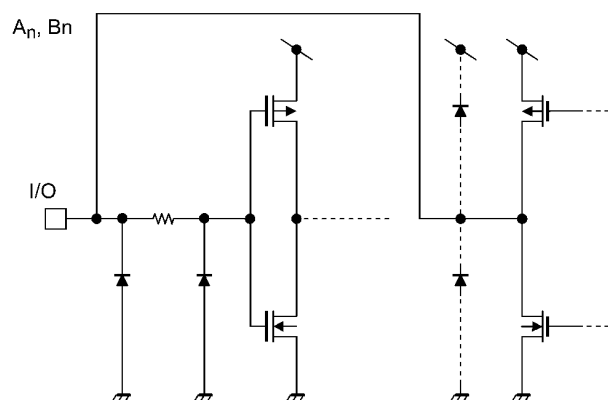
### 11.5. Noise Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 3\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$C_L = 50\text{ pF}$	5.0	0.7	1.0	V
Quiet output minimum dynamic $V_{OL}$	$V_{OLV}$	$C_L = 50\text{ pF}$	5.0	-0.7	-1.0	V
Minimum high-level dynamic input voltage	$V_{IHD}$	$C_L = 50\text{ pF}$	5.0	—	3.5	V
Maximum low-level dynamic input voltage	$V_{ILD}$	$C_L = 50\text{ pF}$	5.0	—	1.5	V

## 12. Internal Equivalent Circuit

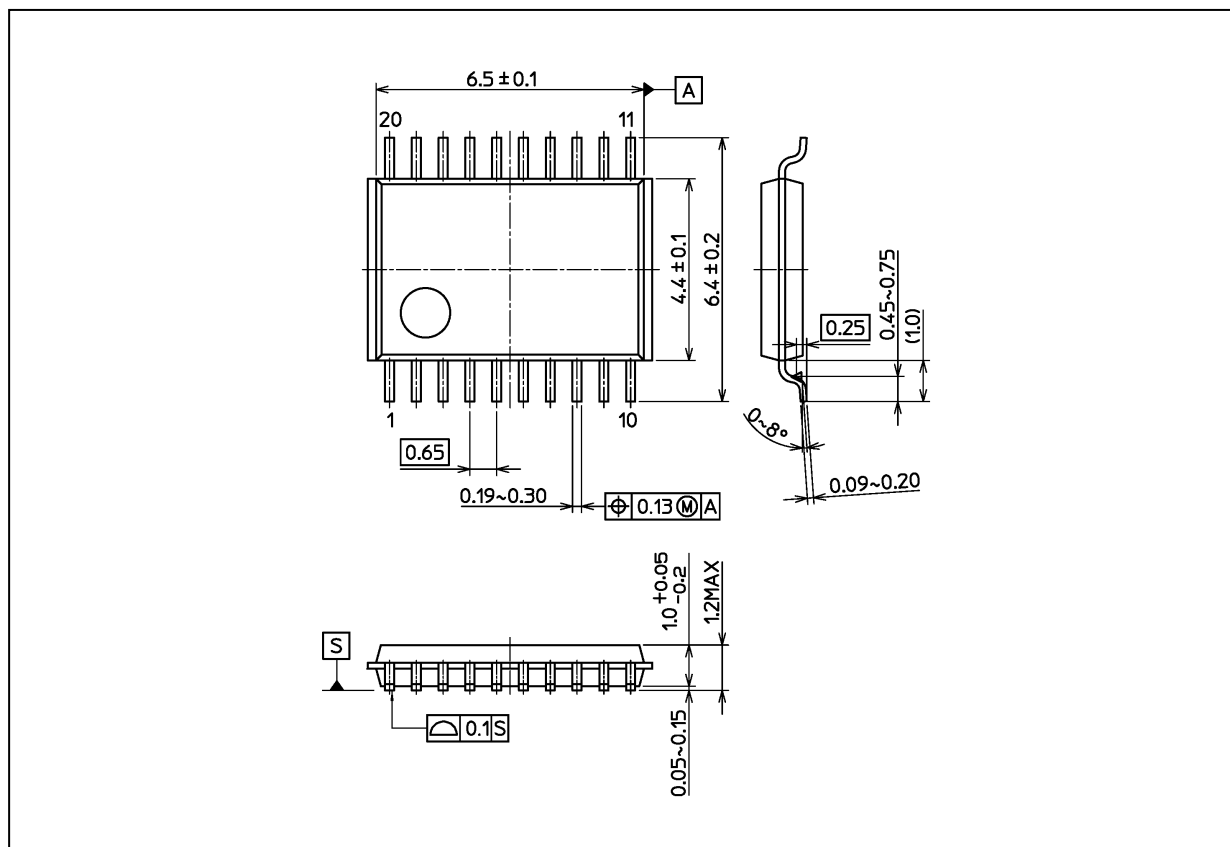


## 13. Bus Terminal Equivalent Circuit



## Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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