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## **Evaluating the AD9523-1 Clock Generator**

#### **FEATURES**

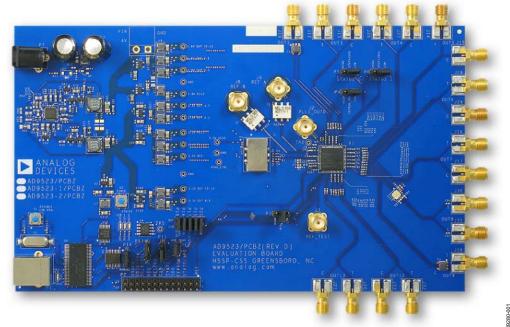
Simple power connection using USB connection and on-board LDO voltage regulators LDOs are easily bypassed for power measurements AC-coupled differential SMA connectors **SMA connectors for** 2 reference inputs 2 PLL status outputs 1 reference test input 2 VCXO interface inputs/outputs Microsoft Windows®-based evaluation software with simple graphical user interface **On-board PLL loop filter** Easy access to digital I/O and diagnostic signals via I/O header **Status LEDs for diagnostic signals USB** computer interface Software calculator provides flexibility, allowing programming of almost any rational input/output frequency ratio

### **GENERAL DESCRIPTION**

This user guide describes the hardware and software of the AD9523-1 evaluation boards. The evaluation board schematic and PCB layout artwork can be found at www.analog.com.

The AD9523-1 is designed to support the clock requirements for long-term evolution (LTE) and multicarrier GSM base station designs. It relies on an external VCXO to provide the reference jitter cleanup to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance. The AD9523-1 evaluation board is a compact, easy-to-use platform for evaluating all features of the AD9523-1. A 122.88 MHz VCXO is mounted on the evaluation board to provide a complete solution.

The input receivers are configured as differential but the evaluation board has baluns to provide a single-ended input for easy evaluation using common laboratory single-ended signal sources. Output 8 is connected to an ADCLK905 clock buffer to provide a way to evaluate an Analog Devices, Inc., buffer. Although the ADCLK905 is a 1-to-1 buffer, the performance is similar to the larger fanout buffer, for example, the 1-to-2 buffer, ADCLK925. Output 1 and Output 9 are configured with baluns to provide a single-ended output to drive most test equipment. Output 0 is configured for differential zero delay operation.



## DIGITAL PICTURE OF EVALUATION BOARD

Figure 1. AD9523-1 Evaluation Board

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### **REVISION HISTORY**

10/10—Revision 0: Initial Version

## **EVALUATION BOARD HARDWARE**

The following instructions are for setting up the physical connections to the AD9523-1 evaluation board.

### SETTING UP JUMPER CONNECTIONS

The evaluation board is configured for proper PC control and operation. If the jumpers are inadvertently moved, use Figure 2 and Figure 3 to reconfigure the board.

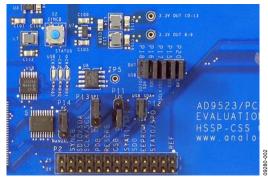


Figure 2. USB and SPI Jumper Connections

### SETTING UP THE POWER AND PC CONNECTIONS

Set up the power and PC connections as follows:

- 1. Install the AD9523-1 evaluation software before connecting the evaluation board to the PC for the first time (see the Installing the Software section). Administrative privileges are required for installation.
- 2. Connect the 6 V wall adapter to Connector P7 of the evaluation board.
- 3. Connect the USB cables to the evaluation board and the computer.
- 4. Found New Hardware Wizard automatically appears when the evaluation board is connected. Select Install the software automatically and then click Next.

The **Found New Hardware Wizard** may appear twice, and a system restart may be required.

Refer to the Evaluation Board Software Setup section for details on running the AD9523-1 evaluation board software.

### SETTING UP THE SIGNAL CONNECTIONS

After setting up the power and PC connections, use the following procedure to set up the signal connections:

- 1. Connect a signal generator to REF A SMA Connector J9. By default, the reference inputs on this evaluation board are ac-coupled and terminated with 50  $\Omega$  to ground. An amplitude setting of 6 dBm is sufficient.
- 2. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the OUTx SMA connectors on the right side of the board. The output connectors are single-ended outputs of a differential pair. A 50  $\Omega$  termination should be placed on all unused differential output pairs.

### SETTING UP THE PLL2 LOOP FILTER CAPACITOR

PLL2 requires an external loop filter capacitor. To achieve the best jitter performance, reference Capacitor C6 to LDO\_VCO, Pin 12. This can done by installing R6 and removing R4. These connections should have been performed at the factory.

# BYPASSING THE 6 V WALL SOCKET POWER SUPPLY

The evaluation board contains a dc-to-dc converter to step down the 6 V to 2.2 V and 4 V. Linear regulators are then used to further regulate the 2.2 V to 1.8 V supply domain and the 4 V to the 3.3 V supply domain. The evaluation board can be configured to bypass the dc-to-dc converter and linear regulators or the dcto-dc converter only. This is useful for measuring AD9523-1 power consumption. Refer to the evaluation board schematics provided on the CD in the evaluation board kit (also available at www.analog.com) for further details.

Bypass the 6 V power supply (dc-to-dc converter and linear regulators) as follows:

- 1. Note that it is very important to not have the 6 V supply connected to the evaluation board while using external supplies. To be safe, remove the inductors from each linear regulator output (L4 to L15).
- 2. Connect a bench power supply to each of the supply pins on Header TP3 through Header TP15. If the inductors were not removed in Step 1, then some of the supply pins are connected together on the evaluation board and damage to the external supply and/or evaluation board may occur.

Bypass the 6 V power supply (dc-to-dc converter only) as follows:

- 1. Remove L1, L2, L3, R39, R41, R40, and R42.
- 2. Connect a 2.2 V bench supply to Connector P19.
- 3. Connect a 4 V bench supply to the L1 pad.

## **Evaluation Board User Guide**

## USING I<sup>2</sup>C SERIAL PORT MODE

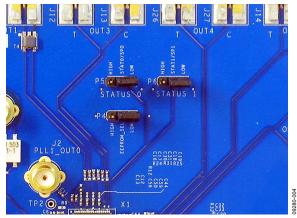


Figure 3. I<sup>2</sup>C Address Jumper Setting

To use the I2C serial Port mode, follow these steps:

- 1. Power down the board and shut down the software.
- 2. Set Jumpers P11 and P13 to the **I2C** position (see Figure 2).
- 3. Select the desired I<sup>2</sup>C address using Jumpers P5 and P6 (see Figure 3). Note that setting P5 and P6 low is reserved for SPI mode.
- 4. Power up the board and connect the USB cable to the board.
- 5. Start the evaluation board software.
- 6. On the evaluation software, select **Configure Serial Port** from the **I/O** menu (see the I/O Menu section).
- Click the Reset Serial Port button, and then click Detect Current Configuration (see Figure 8). A dialog box should appear to acknowledge the I<sup>2</sup>C mode and address.

## **EVALUATION BOARD SOFTWARE SETUP**

The instructions included in this section are for setting up the AD9523-1 evaluation board software.

## **INSTALLING THE SOFTWARE**

Do not connect the evaluation board until the software installation is complete. To install the software,

- 1. Insert the AD9523-1 evaluation software CD-ROM into a PC CD disc drive.
- 2. Click **My Computer**, and then double-click the **AD9523-1EV CD** icon.

A window opens showing the contents of the CD divided into four sections: data sheet, layout, schematic, and software. The **readme.txt** file contains a description of the CD-ROM contents, as well as any last minute instructions or information.

3. Double-click the **Software** folder, and then double-click **AD9523-1Eval\_Setup1.1.0.exe**. Follow the installation instructions.

The default location for the evaluation software is C:\Program Files\Analog Devices\AD9523-1 Eval Software\.

4. If there are any updates to the evaluation software on a supplemental CD or in the **\Software\Updates** folder, be sure to copy the new .exe file, as well as any setup files, to the default location.

### **USING THE SOFTWARE**

After the evaluation software has been installed, you can run the software as follows:

- 1. Power up and connect the evaluation board to the PC.
- 2. Double-click **AD9523-1 Eval Software** to run the AD9523-1 evaluation software.

A hardware installation window appears. Depending on whether the evaluation board was found by the software, the text in this window is either light blue, indicating that the evaluation board was found, or red, indicating that the evaluation board was not found.

3. If the evaluation board was found, click in the window when the **Evaluation Software Ready** message appears.

The main window of the evaluation board software appears. Proceed to the Evaluation Board Software Operation section for more details about using the software.

- 4. If the evaluation board was not found, a dialog box appears that allows you to select an evaluation board to use while the software runs in standalone mode. Standalone mode is useful for viewing and generating register setup files.
  - a. If the evaluation board was not automatically detected when it was connected, choose Select Evaluation Board from the I/O menu, and then select Ezssp-0, Ezssp-1, or Ezssp-2 (see Figure 4).

Device	Firmware Rev. Host	
Ezssp-0	1.4 Usin	g

Figure 4. Select USB Device Window

5. If you connect the evaluation board while the evaluation board software is running, the window shown in Figure 5 usually appears to prompt you to load the evaluation board with the evaluation board software settings or to read the current evaluation board settings into the software.

SYNC Evaluation Software
Communication with the evaluation board has been restored!
The current state of the AD9523 is unknown! Click the SYNC button to synchronize the evaluation board and software.
Options
$\ensuremath{\mathfrak{C}}$ Load the evaluation board with the current software settings.
C Read the current evaluation board settings into the software.
SYNC Cancel

Figure 5. SYNC Evaluation Software Window

## EVALUATION BOARD SOFTWARE OPERATION

The main window of the AD9523-1 evaluation board software comprises subsections that correspond to the major functional blocks of the AD9523-1 (see Figure 6). These subsections, most of which have their own window, are outlined in this section. From the main window, the window for each functional block can be accessed by clicking the appropriate box.

When a subsection window closes after clicking OK, the WRITE button under REGISTER W/R on the main window may start blinking. This indicates that there are settings that have not been loaded to the AD9523-1 evaluation board. Click WRITE to load these settings to the evaluation board.

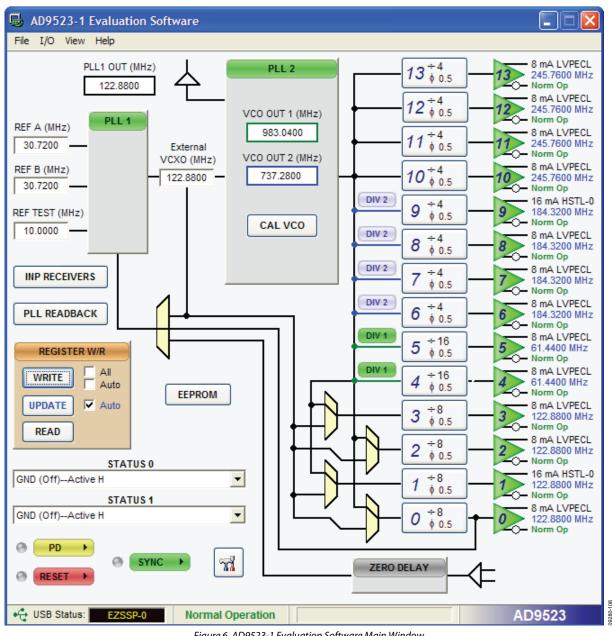


Figure 6. AD9523-1 Evaluation Software Main Window

#### MENU BAR OF MAIN WINDOW

#### File Menu

The **File** menu allows you to load a previously saved AD9523-1 setup file or to save a new AD9523-1 setup file. A setup file (.stp) is a text file that contains the AD9523-1 register setup file, plus any evaluation board settings.

To load a previously saved setup file, select **Load Setup** from the **File** menu. Note that you must still perform a VCO calibration. Alternatively, to save a new setup file, select **Save Setup** from the **File** menu.

To exit the evaluation software, select **Exit** from the **File** menu. However, note that you must save your setup before exiting; no checking is performed to ensure that the existing setup is saved.

#### I/O Menu

The AD9523-1 evaluation system allows one PC to control multiple evaluation boards. The **Select USB Device** window, accessed by choosing **Select Evaluation Board** from the **I/O** menu, allows you to select which evaluation board the software controls (see Figure 7). Click **Refresh List** to detect a recently connected evaluation board.

Selec	t the Evaluation Board to use:
Device	Firmware Rev. HostID
Ezssp-0	1.4 Using

Figure 7. Select USB Device Window

Selecting **Configure Serial Port** from the **I/O** menu allows you to control how the USB controller interacts with the AD9523-1 serial port (see Figure 8) by configuring Register 0x0000 (shown as **0000h** in Figure 10).

The serial port configuration window allows you to control how the USB controller interacts with the AD9523-1 serial port. If you are using I<sup>2</sup>C mode, this window allows you to select which address to use. Note that it needs to correspond to the settings of Jumpers P5 and P6 on the evaluation board. You can also click the **Detect Current Configuration** button to have the evaluation software discover which I<sup>2</sup>C address is active.



Figure 8. Serial Port Configuration Window

#### View Menu

The **Debug** window, accessed by selecting **Debug Window** from the **View** menu, allows you to write and read registers directly and to force the various configuration pins high or low (see Figure 9).

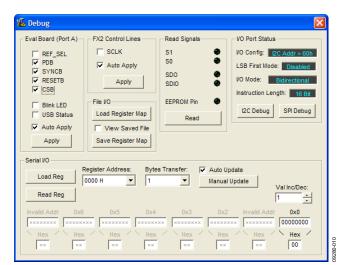


Figure 9. Debug Window

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The **Register Map Values** window, accessed by selecting **Register Map Window** from the **View** menu, allows you to read registers (see Figure 10).

🖃 Reg	ister Map	Values							X
Addr:	Binary Val:	Addr:	Binary Val:	Addr:	Binary Val:	Addr:	Binary Val:	Addr:	Binary Val:
0000h	00000000	00F9h	00000000	01AEh	00000000	0A09h	00001110	100Dh	00000000
0002h	00000000	00FAh	00000000	01AFh	00011111	QAQAh	00000000	100Eh	00000000
0003h	00000000	0190h	00000000	01B0h	00000000	0A0Bh	11110000	100Fh	00000000
0004h	00000000	0191h	00011111	01B1h	00010000	0A0Ch	00001011	1010h	00000000
0005h	00000000	0192h	00000000	01B2h	00011111	QAODh	00000001		
0006h	00000000	0193h	00010000	01B3h	00000000	0A0Eh	10010000	Regma	ap Buffer:
0010h	00000000	0194h	000111111	01B4h	00000000	0A0Fh	00000001	Net	w Values
0011h	00000000	0195h	00000000	01B5h	00011111	0A10h	00000001		rent Values
0012h	00000000	0196h	00000000	01B6h	00000000	0A11h	11100000	, o cu	Territ Values
0013h	00000000	0197h	00011111	01B7h	00010000	0A12h	00000001	Data F	
0014h	00000000	0198h	00000000	01B8h	00011111	0A13h	00000010		
0015h	00000000	0199h	00010000	01B9h	00000000	0A14h	00110000	💿 Bin	ary
0016h	00000000	019Ah	00011111	01BAh	00000000	0A15h	10000000	C He	
0017h	00000000	019Bh	00000000	01BBh	10000000	0A16h	111111111		
0018h	00001100	019Ch	00000000	022Ch	00000000	OBOOh	00000000	🔽 Au	to Refresh
0019h	00000000	019Dh	00011111	022Dh	00000000	0B01h	00000000	J¥ Au	to nellesh
001Ah	00000000	019Eh	00000000	022Eh	00000000	0B02h	00000000		1
001Bh	00000000	019Fh	00010000	022Fh	00000000	0B03h	00000000	Re	efresh
001Ch	00000000	01A0h	00011111	0230h	00000000	OFFFh	00000000		
001Dh	00000000	01A1h	00000000	0231h	00000000	1000h	00010000		
001Eh	00000000	01A2h	00000000	0232h	00000000	1001h	00100000		
001Fh	00000000	01A3h	000111111	0233h	00000000	1002h	01000000		
0020h	00000000	01A4h	00000000	0234h	00000000	1003h	00000000		
00F0h	00000000	01A5h	00010000	0400h	00000000	1004h	00000000		
00F1h	00000100	01A6h	00011111 00000000	0A01h 0A02h	00000000 00000000	1005h	00000000		
00F2h 00F3h	00000011	01A7h 01A8h		0A03h	000000000	1006h 1007h	00000000 00000000		
	00000000		000000000		00000010				
00F4h 00F5h	00000000 00000000	01A9h 01AAh	000111111 00000000	0A04h 0A05h	000000000	1008h 1009h	00000000 00000000		
00F5h	00000000	01AAN 01ABh	00010000	0A06h	00000100	1009n 100Ah	000000000		
00F6h 00F7h	00000000	01ABh 01ACh	00010000	0405h	000001110	1008h	000000000		
00F7h 00F8h	00000000	01ADh	000000000	0408h	00010000	1006h	000000000		
ooran	000000000	UIAUN	00000000	uquan	00010000	rooun	000000000		



#### Help Menu

Selecting **Help** from the **Help** menu opens the **About AD9523-1** window, which contains information such as revision number, region information, and contact information.

### USING THE SOFTWARE TO CONTROL THE FUNCTIONAL BLOCKS OF AD9523-1 REGISTER W/R

The **REGISTER W/R** (write/read) section in Figure 6 has three buttons and three check boxes.

The **WRITE** button transfers the values stored in the evaluation software to the evaluation board. It blinks red when register values have changed.

The **READ** button transfers the values stored in the evaluation board to the evaluation software.

The **UPDATE** button issues an I/O update command by writing to the I/O update register.

Selecting the **All** check box transfers all of the registers when the **WRITE** button is clicked. When this box is not selected, only the registers whose value has changed are written.

Selecting the **Auto** check box adjacent to the **WRITE** button forces the evaluation software to write the register changes to the evaluation board automatically when they occur.

Selecting the **Auto** check box adjacent to the **UPDATE** box forces the evaluation software to issue an I/O update command whenever registers are written to the AD9523-1.

#### SYNC, PD (Power Down), and RESET

The SYNC, PD, and RESET buttons allow you to control the SYNC, PD, and RESET pins on the AD9523-1.

Each button has three options: **Strobe**, **Latch**, and **Release**. **Strobe** activates the pin and then releases it. **Latch** holds the pin active until the **Release** command is issued.

### **PLL 1 CONTROLS**

The **PLL 1** box in the main window (see Figure 6) allows you to configure the PLL1 parameters. Clicking the **PLL 1** box in the main window, shown in Figure 11, opens a window to allow configuration of PLL1 (see Figure 12).

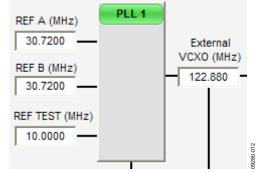


Figure 11. PLL1 Box (in Main Window)

Clicking each individual box in the **PLL 1 Controls** window opens a new window to allow configuration of that block (see Figure 13 for an example for the **REF A Divider** window).

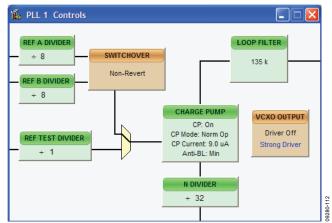


Figure 12. PLL1 Controls Window

#### Reference (REF) Divider Window

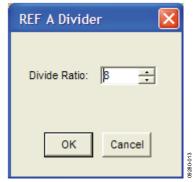


Figure 13. Reference A or Reference B Divider Window

The reference divider window shown in Figure 13 is accessed by clicking the **REF A Divider** box in Figure 12. It allows you to set the reference divider. There is a corresponding window for both REF A and REF B dividers.

#### Feedback (N) Divider Window

N Divider	
Divide Ratio:	32 🕂
ОК	Cancel

Figure 14. N Divider Window

The feedback divider window shown in Figure 14 is accessed by clicking the **N DIVIDER** box in Figure 12. It allows you to set the feedback divider.

#### **Charge Pump Window**

Charge Pump Setup					
Tri-State Charg	ge Pump				
CP Mode: Tri-State Pump Down Pump Up Normal Operation	CP Current (uA): 3.0 3.5 4.0 4.5 5.0				
Enable Anti-Backlash Period Anti-Backlash:					
Minimum Low High Maximum					
Са	ancel				

Figure 15. Charge Pump Window

The **Charge Pump Setup** window shown in Figure 15 is accessed by clicking the **CHARGE PUMP** box in Figure 12.

This window is most often used to vary the charge pump current.

### **PLL 2 CONTROLS**

Clicking the **PLL 2** box from the main window (see Figure 16) opens a window to allow configuration of PLL 2 (see Figure 17).

-	D OUT		Hz)
L	983.0	400	
-	D OUT		Hz)
L	737.2	800	
_			-
	CAL	/CO	

Figure 16. PLL 2 Box (in Main Window)

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Clicking each individual box in the **PLL 2 Controls** window opens a new window to allow configuration of that block.

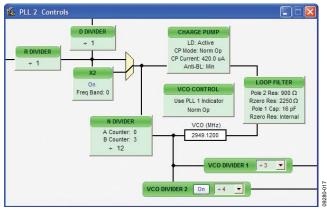


Figure 17. PLL 2 Controls Window

#### Feedback (N) Divider Window

N Divider	
Divide Ratio: 12 (N = 4B + A)	
A Counter: 0 + B Counter: 3 +	
OK Cancel	
Eigure 18 N Divider Winde	2144

Figure 18. N Divider Window

The **N Divider** window shown in Figure 18 is accessed by clicking the **N DIVIDER** box in Figure 17. It allows you to set the feedback divider.

#### VCO Divider 1 and Divider 2

The VCO dividers controls are located in the **PLL 2 Controls** window shown in Figure 17. They allow you to set the frequency feeding the channels. Channel OUT4 through Channel OUT9 can be configured for either Divider 1 or Divider 2. If Divider 2 is not required, it is recommended that it be turned off for best spurious performance.

#### **Charge Pump Window**

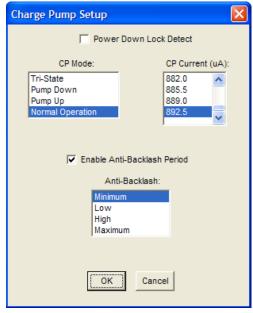


Figure 19. Charge Pump Window

The **Charge Pump Setup** window shown in Figure 19 is accessed by clicking the **CHARGE PUMP** box in Figure 17.

This window is most often used to vary the charge pump current.

### **CHANNEL DIVIDER WINDOW**

Divider 13 Settings	
Divide Ratio:	32 <b>*</b>
Divider Phase:	0.0 💌
ок	[Cance]

Figure 20. Channel Divider Window

The channel divider window shown in Figure 20 is accessed by clicking the appropriate channel divider (see Figure 21) in the main window shown in Figure 6. It is usually sufficient to change only the divide ratio, because the evaluation software and the AD9523-1 duty cycle correction feature ensure that the output duty cycle remains very close to 50%.

Figure 21. Channel Divider

You can also vary the phase offset by changing the phase offset bits setting under the **Divider Phase** box in Figure 20. However, for the new phase to take effect, the  $\overline{SYNC}$  signal must be toggled, by clicking the SYNC button shown in Figure 22 and selecting **Strobe SyncB**.



Figure 22. Toggling SYNC Signal

### **OUTPUT DRIVER WINDOW**

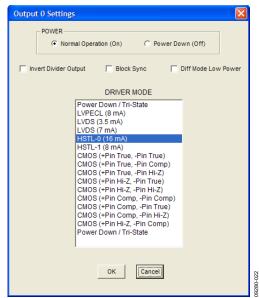


Figure 23. Output Driver Window

The output driver window shown in Figure 23 is accessed by clicking any of the triangular output driver symbols on the right side of the main window (see Figure 24).

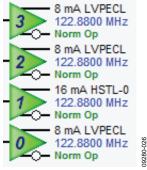


Figure 24. Output Drivers

It is important to power down unused outputs on the evaluation board because they can be a major source of unwanted spurs.

The outputs are ac-coupled with 100  $\Omega$  differential resistors on each output. This termination scheme is ideal for LVPECL drivers. However, this scheme degrades the CMOS driver performance. Improved CMOS driver performance is achieved by removing the 100  $\Omega$  resistors.

#### **EEPROM CONTROL**

	EEPROM Status Registers	
EEPROM Status	Data Transfer Status:	Finished
Program EEPROM	Error Checking:	Correct

Figure 25. EEPROM Control Window

The **EEPROM Control** window shown in Figure 25 is accessed by clicking the **EEPROM** button near the lower left quadrant of the main window.

To store the current register settings of the AD9523-1 to the EEPROM, click the **Program EEPROM** button. Visually confirm the **EEPROM Status Registers** section on the right side of the window to verify that the operation is successful.

To load the values stored in the EEPROM,

- 1. Disconnect the 6 V power connector to power down the AD9523-1.
- 2. Ensure that the EEPROM pin is pulled high by placing the P4 EEPROM\_SEL jumper of the evaluation board across the center and left (high) pin (see Figure 3).
- 3. Reconnect the 6 V power supply. This automatically loads the EEPROM settings into the AD9523-1. The programmed settings can be observed at the outputs. In addition, a window opens (see Figure 26). Click the second option to read from the AD9523-1. This loads the control software with the current register settings that were programmed by the EEPROM.

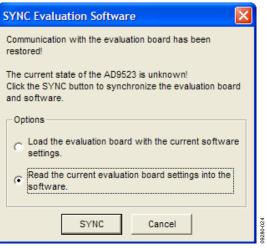


Figure 26. SYNC Evaluation Software Window

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## **USING THE EVALUATION BOARD TO PROGRAM AN AD9523-1 ON A CUSTOMER BOARD**

This guide explains how to use an AD9523-1 evaluation board to program an AD9523-1 on a customer board via the I<sup>2</sup>C interface. It assumes that the user has access to the I<sup>2</sup>C pins via a header on the target board, and knows the assigned address of the target I<sup>2</sup>C device.

- 1. Move Jumpers P13 and P11 to the I2C position.
- Select the desired I<sup>2</sup>C address for the AD9523-1 evaluation board using Jumper P5 and Jumper P6. Note that the P5 = P6 = low setting is reserved for SPI mode. Also, this I<sup>2</sup>C address should not conflict with the I<sup>2</sup>C address of the target AD9523-1.
- 3. Attach a jumper cable from the SDIO\_SDA pin of Header P2 of the evaluation board to the SDA pin on the target board.
- 4. Repeat Step 3 for both the SCLK\_SCL pin and the GND pin of the AD9523-1 evaluation board, attaching jumper cables to the SCL pin and ground pin of the target board, respectively.
- 5. On the evaluation software, select **Configure Serial Port** from the **I/O** menu. This window is shown in Figure 27.

I/O Interface			×
Serial Port Confi	guration:		- Serial Port
I2C Address	S1 Pin Value	S0 Pin Value	
Use SPI	Low	Low	Soft Reset
60 Hex	Low	High	LSB First Mode
61 Hex 62 Hex	High High	Low High	Instruction Length:
			8 Bits 16 Bits
			Serial VO Mode:
Detect Current Configuration		Bidirectional Unidirectional	
Communication Speed: 100 kHz		Reset Serial Port	
ОК	Cancel		

Figure 27. Evaluation Software Serial Port Configuration

- 6. Click Reset Serial Port and then click Detect Current Configuration. A dialog box appears and acknowledges the I<sup>2</sup>C mode and address. The evaluation software starts at I<sup>2</sup>C Address 0x060 and stops at the first valid I<sup>2</sup>C address that it finds. If the target I<sup>2</sup>C address is different from the one automatically selected, select the I<sup>2</sup>C address of the target AD9523-1 from the list, and click OK.
- From the View menu on the menu bar, select Debug Window. From the Debug window (see Figure 9), click the I2C Debug button under the I/O Port Status section. The window shown in Figure 28 appears.



Figure 28. Evaluation Software I<sup>2</sup>C Debug Window

8. Enter the I<sup>2</sup>C address set by Jumper P5 and Jumper P6 on the AD9523-1 evaluation board, and click **Ping**. The user should see a green **ACK** message as shown in Figure 28. Repeat this step for the I<sup>2</sup>C address of the target AD9523-1. If **ACK** is returned for both addresses, the remote AD9523-1 is ready to be programmed.

If the ping test fails, double-check the cabling between the boards, as well as the I<sup>2</sup>C address of the target AD9523-1. Ensure that the I<sup>2</sup>C address of the AD9523-1 on the evaluation board is different from the target AD9523-1. Also, disconnect the jumper cable, and make sure that I<sup>2</sup>C mode is working properly on the AD9523-1 evaluation board.

- 9. Proceed to program the target AD9523-1 with the desired settings.
  - a. When finished, click the **EEPROM** button on the main window to access the EEPROM window.
  - b. Click **Program EEPROM** to write the settings to the EEPROM.

## QUICK START GUIDE TO THE AD9523-1

The AD9523-1 can be initialized at startup from either the EEPROM or from SPI settings. The AD9523-1 evaluation board ships with initial settings programmed in the EEPROM. It is advised that the user first use the preprogrammed EEPROM settings before proceeding onto software control.

To load the values stored in the EEPROM:

- 1. Ensure that the EEPROM pin is pulled high by placing the P4 EEPROM\_SEL jumper of the evaluation board across the center and left (high) pin (see Figure 3).
- 2. Connect a signal generator to REF A SMA Connector J9. By default, the reference inputs on this evaluation board are ac-coupled and terminated with 50  $\Omega$  to ground. An amplitude setting of 6 dBm is sufficient and the frequency should be 30.72 MHz.
- 3. Connect an oscilloscope, spectrum analyzer, or other lab equipment to the OUT1 SMA connector on the right side of the board. This output connector is a single-ended output of a differential pair.
- 4. Connect the 6 V power supply. This automatically loads the EEPROM settings into the AD9523-1 (the EEPROM configurations are similar as shown in Figure 6).

To load the provided setup file:

- 1. Follow the instructions provided in the Evaluation Board Software Setup section.
- 2. Ensure that the EEPROM pin is pulled low by placing the P4 EEPROM\_SEL jumper of the evaluation board across the center and right (low) pin (see Figure 3).
- 3. Connect a signal generator to REF A SMA Connector J9. By default, the reference inputs on this evaluation board are ac-coupled and terminated with 50  $\Omega$  to ground. An amplitude setting of 6 dBm is sufficient and the frequency should be 30.72 MHz.
- 4. Connect the 6 V power supply.
- Provided on the CD is a setup file named AD9523-1\_983plan\_122p88MHz\_VCXO\_DoublerON.stp located in the Setup Files directory. Load this setup file using the File menu from the main software window. The main window should appear as shown in Figure 6.
- 6. Click the **CAL VCO** button located in the **PLL 2** box of Figure 6.
- 7. Connect an oscilloscope, spectrum analyzer, or other lab equipment to the OUT1 SMA connector on the right side of the board. This output connector is a single-ended output of a differential pair. A picture of phase noise profile is located in the same directory as the setup file with the same file name (with the .png extension).

## NOTES

## NOTES

## NOTES



#### ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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