74LVC16374A; 74LVCH16374A

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Rev. 11 — 16 January 2013 Product data sheet

1. General description

The 74LVC16374A and 74LVCH16374A are 16-bit edge-triggered flip-flops featuring separate D-type inputs with bus hold (74LVCH16374A only) for each flip-flop and 3-state outputs for bus-oriented applications. It consists of two sections of eight positive edge-triggered flip-flops. A clock input (nCP) and an output enable ($n\overline{OE}$) are provided for each octal.

The flip-flops store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition.

When pin $n\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When pin $n\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of input $n\overline{OE}$ does not affect the state of the flip-flops.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

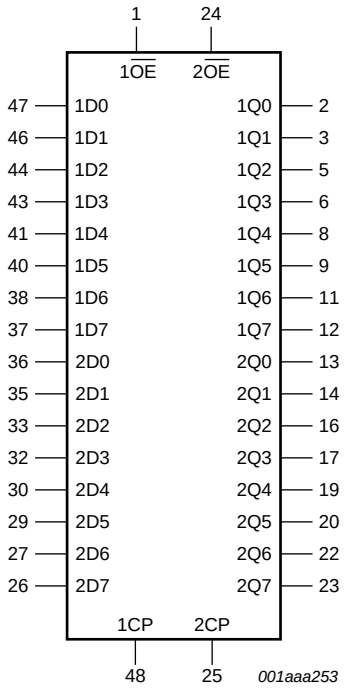
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Low inductance multiple supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16374A only)
- High-impedance outputs when V_{CC} = 0 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

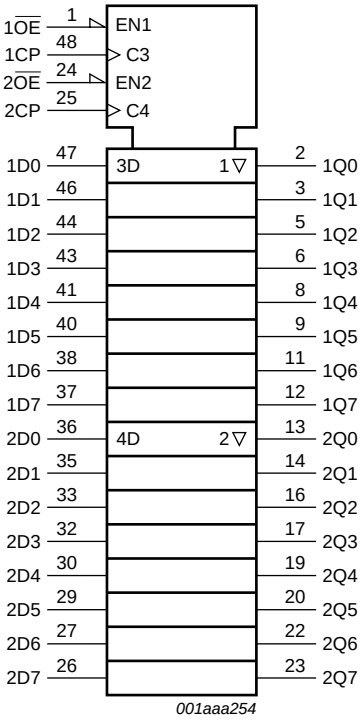
Type number	Package			
	Temperature range	Name	Description	Version
74LVC16374ADL	–40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVCH16374ADL				
74LVC16374ADGG	–40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16374ADGG				
74LVC16374ABX	–40 °C to +125 °C	HXQFN60U	plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 × 6 × 0.5 mm	SOT1134-1
74LVCH16374ABX				

4. Functional diagram



Pin numbers are shown for SSOP48 and TSSOP48 packages only.

Fig 1. Logic symbol



Pin numbers are shown for SSOP48 and TSSOP48 packages only.

Fig 2. IEC logic symbol

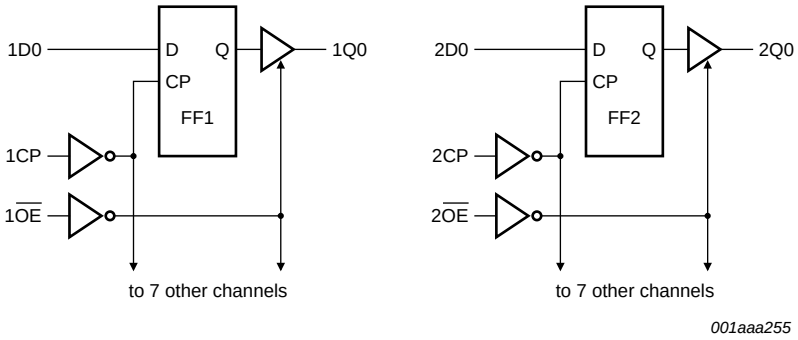


Fig 3. Logic diagram

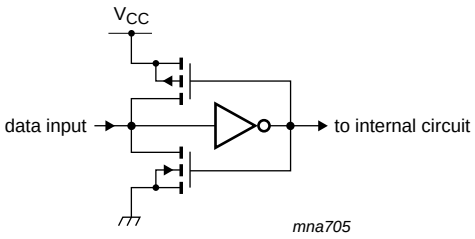


Fig 4. Bus hold circuit

5. Pinning information

5.1 Pinning

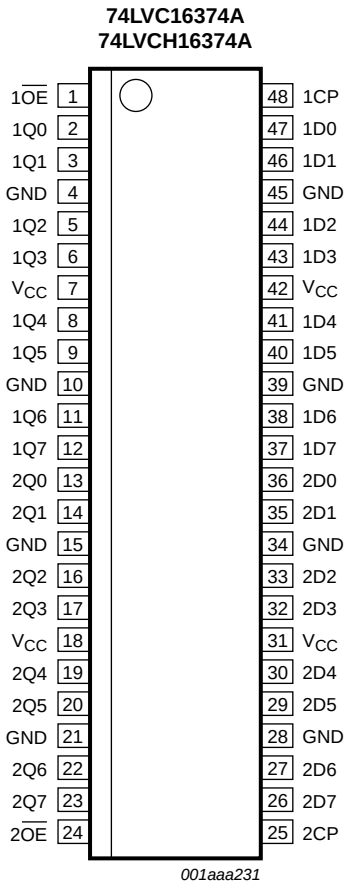
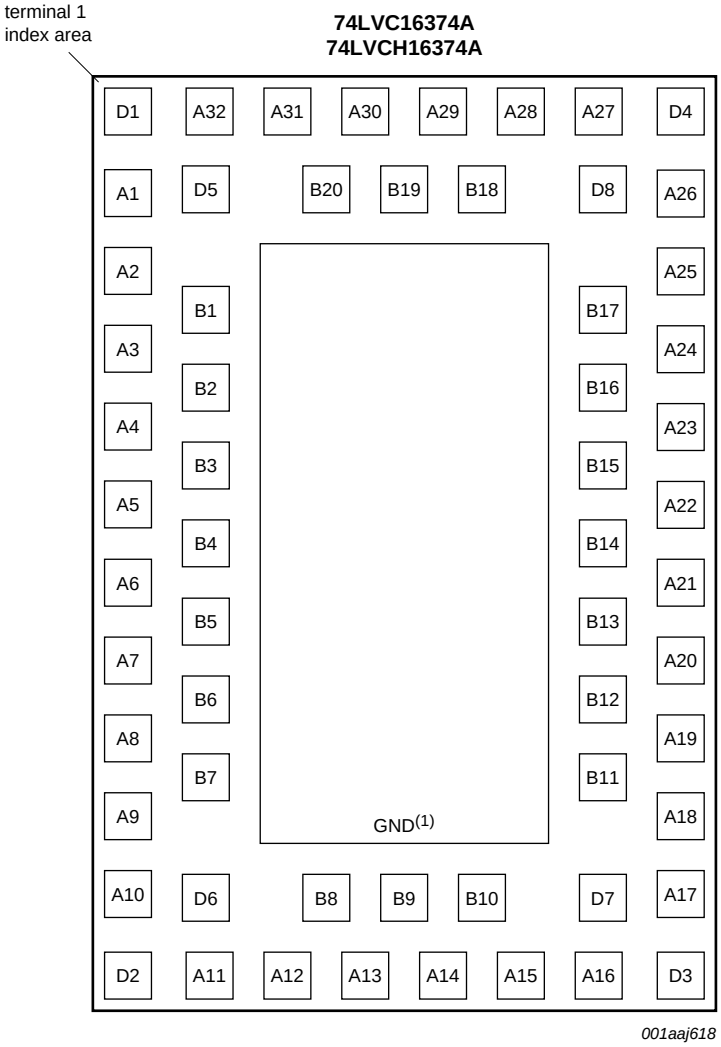


Fig 5. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 6. Pin configuration SOT1134-1 (HXQFN60U)

5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT370-1 and SOT362-1	SOT1134-1	
$1\overline{OE}$, $2\overline{OE}$	1, 24	A30, A13	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V_{CC}	7, 18, 31, 42	A1, A10, A17, A26	supply voltage
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	B20, A31, D5, D1, A2, B2, B3, A5	data output
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	A6, B5, B6, A9, D2, D6, A12, B8	data output
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	B18, A28, D8, D4, A25, B16, B15, A22	data input
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	A21, B13, B12, A18, D3, D7, A15, B10	data input
1CP, 2CP	48, 25	A29, A14	clock input

6. Functional description

Table 3. Function selection[1]

Operating mode	Input			Internal flip-flop	Output nQ0 to nQ7
	$n\overline{OE}$	nCP	nDn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;
↑ = LOW-to-HIGH transition;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH-or LOW-state	[2]	–0.5	V_{CC} + 0.5	V
		output 3-state	[2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C

Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C				
		(T)SSOP48 package	[3]	-	500	mW
		HXQFN60U package	[4]	-	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

[4] Above 70 °C, the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V

Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = –100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	V_{CC}	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	0	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND [2]	-	±0.1	±5	-	±20	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND [2]	-	±0.1	±5	-	±20	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±10	-	±20	μA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	20	-	80	μA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0 A	-	5	500	-	5000	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF
I_{BHL}	bus hold LOW current	V_{CC} = 1.65; V_I = 0.58 V [3][4]	10	-	-	10	-	μA
		V_{CC} = 2.3; V_I = 0.7 V	30	-	-	25	-	μA
		V_{CC} = 3.0; V_I = 0.8 V	75	-	-	60	-	μA
I_{BHH}	bus hold HIGH current	V_{CC} = 1.65; V_I = 1.07 V [3][4]	–10	-	-	–10	-	μA
		V_{CC} = 2.3; V_I = 1.7 V	–30	-	-	–25	-	μA
		V_{CC} = 3.0; V_I = 2.0 V	–75	-	-	–60	-	μA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 1.95 V [3][5]	200	-	-	200	-	μA
		V_{CC} = 2.7 V	300	-	-	300	-	μA
		V_{CC} = 3.6 V	500	-	-	500	-	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 1.95 V [3][5]	–200	-	-	–200	-	µA
		V_{CC} = 2.7 V	–300	-	-	–300	-	µA
		V_{CC} = 3.6 V	–500	-	-	–500	-	µA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input pin.

[3] Valid for data inputs (74LVCH16374A) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQn; see Figure 7 [2]						
		V_{CC} = 1.2 V	-	14	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.1	6.9	13.5	2.1	15.6	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.7	6.7	1.5	7.7	ns
		V_{CC} = 2.7 V	1.5	3.4	6.0	1.5	7.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.1	5.4	1.5	7.0	ns
t_{en}	enable time	$n\overline{OE}$ to nQn; see Figure 9 [2]						
		V_{CC} = 1.2 V	-	20	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	5.9	13.1	1.5	15.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.4	6.9	1.5	8.0	ns
		V_{CC} = 2.7 V	1.5	3.6	6.0	1.5	7.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.7	5.2	1.0	6.5	ns
t_{dis}	disable time	$n\overline{OE}$ to nQn; see Figure 7 [2]						
		V_{CC} = 1.2 V	-	12	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.8	4.6	9.1	2.8	10.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.5	4.9	1.0	5.7	ns
		V_{CC} = 2.7 V	1.5	3.4	5.1	1.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.1	4.9	1.5	6.5	ns
t_W	pulse width	nCP HIGH; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V_{CC} = 2.7 V	3.0	-	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.0	1.5	-	3.0	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	nDn to nCP; see Figure 8							
		V_{CC} = 1.65 V to 1.95 V		4.0	-	-	4.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		3.0	-	-	3.0	-	ns
		V_{CC} = 2.7 V		1.9	-	-	1.9	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.9	0.3	-	1.9	-	ns
t_h	hold time	nDn to nCP; see Figure 8							
		V_{CC} = 1.65 V to 1.95 V		3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.5	-	-	2.5	-	ns
		V_{CC} = 2.7 V		1.1	-	-	1.1	-	ns
		V_{CC} = 3.0 V to 3.6 V		+1.5	–0.3	-	1.5	-	ns
f_{max}	maximum frequency	see Figure 7							
		V_{CC} = 1.65 V to 1.95 V		100	-	-	80	-	ns
		V_{CC} = 2.3 V to 2.7 V		125	-	-	100	-	ns
		V_{CC} = 2.7 V		150	-	-	120	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	300	-	120	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	14.1	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	16.4	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	18.5	-	-	-	pF

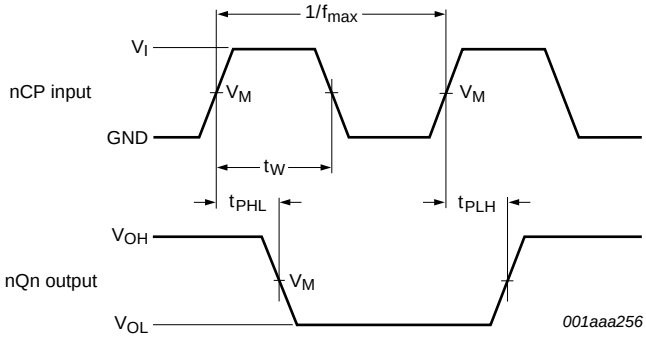
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

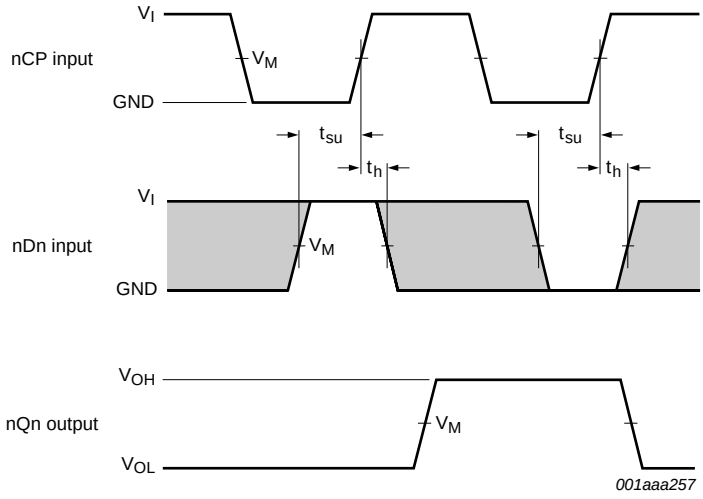
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 7. Clock (nCP) to output (nQn) propagation delays, clock pulse width, and the maximum frequency

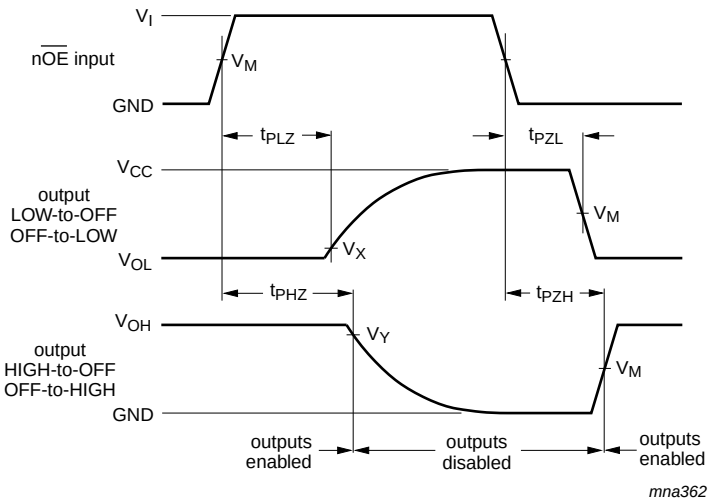


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable performance.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 8. Data set-up and hold times for the nDn input to the nCP input



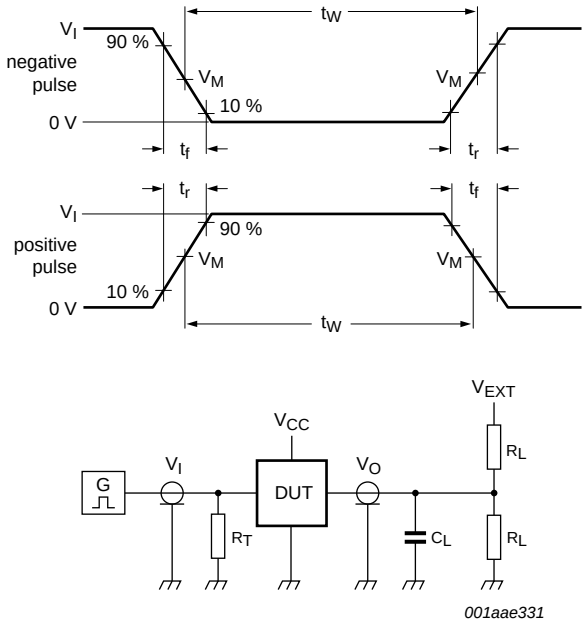
Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 9. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

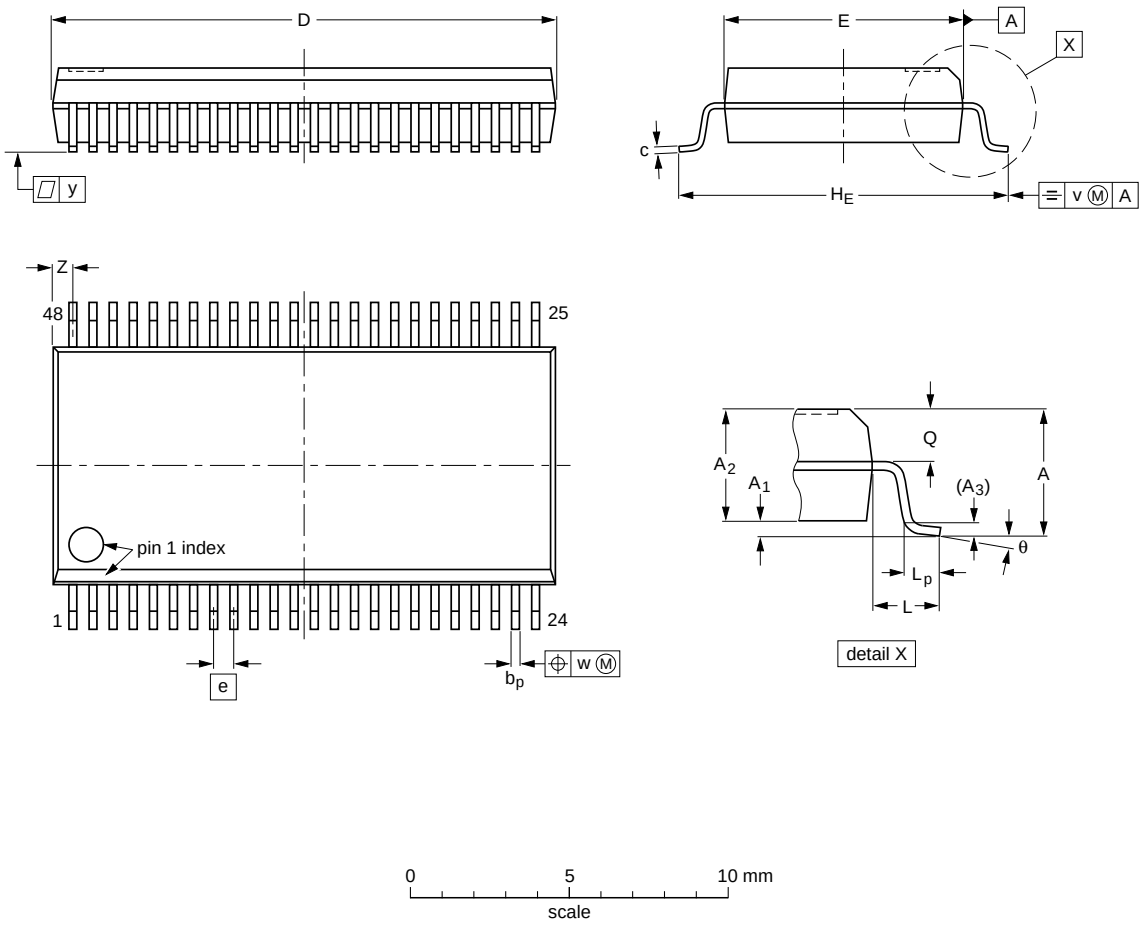
Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

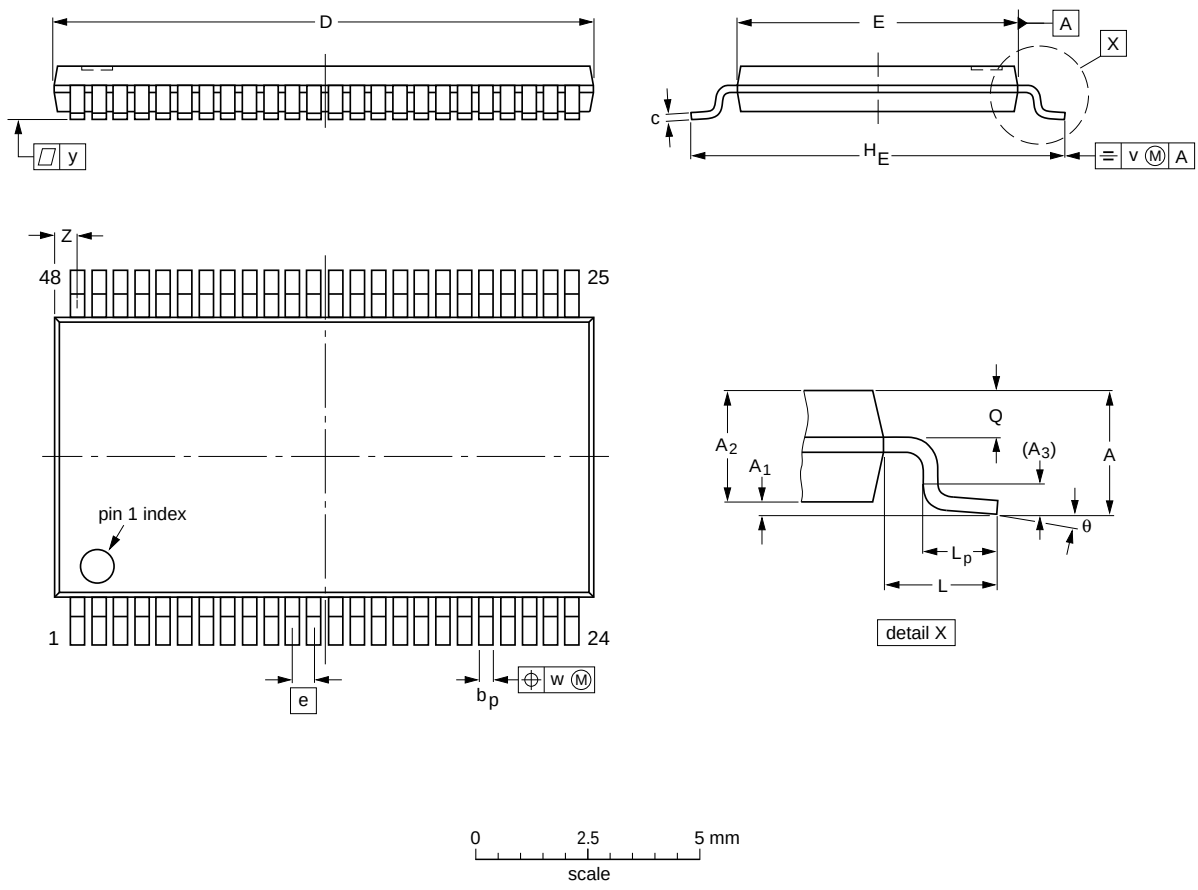
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

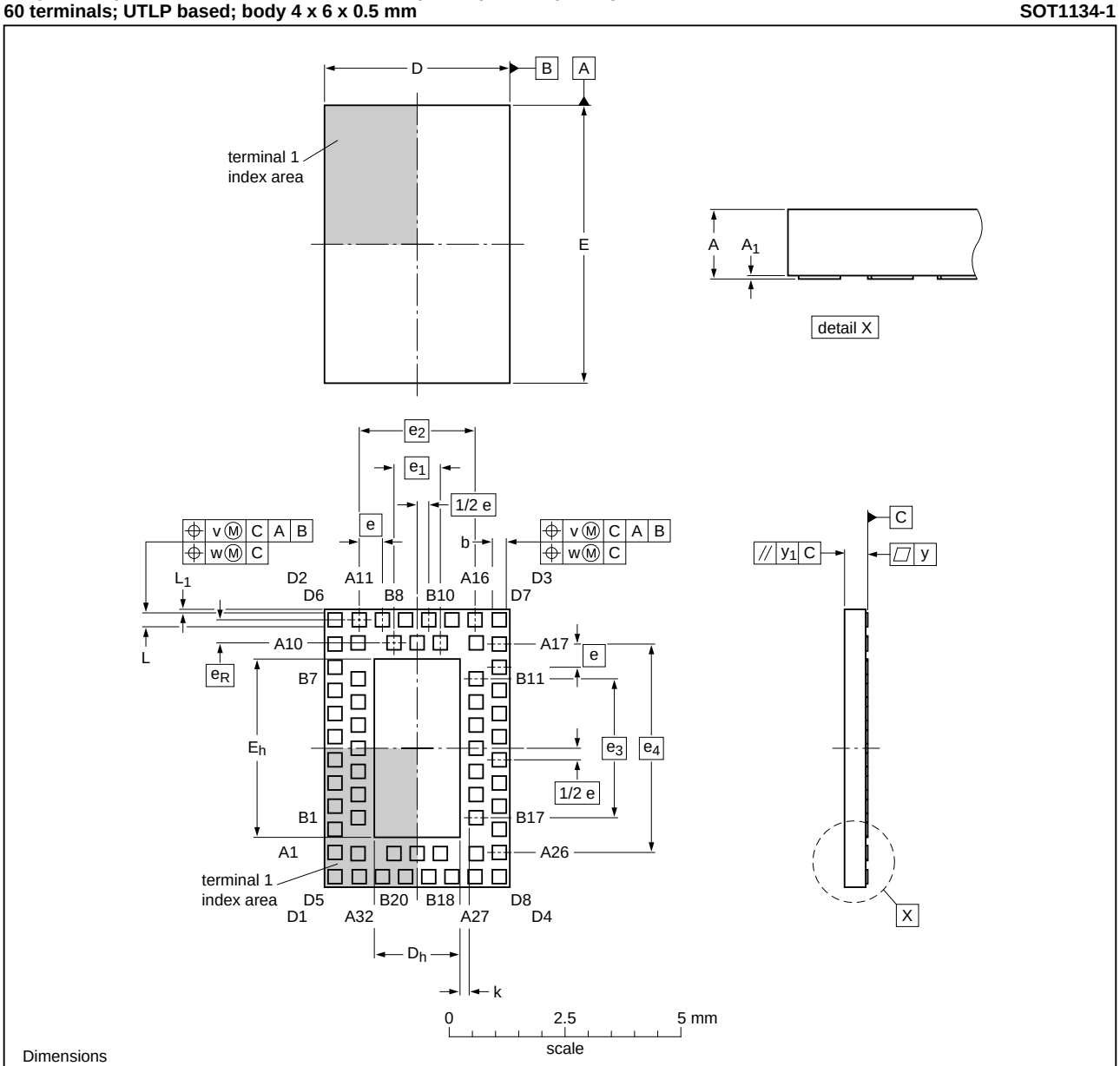
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT362-1 (TSSOP48)

HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 x 6 x 0.5 mm **SOT1134-1**



Dimensions

Unit		A	A_1	b	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	eR	k	L	L_1	v	w	y	y_1
	max	0.50	0.05	0.35	4.1	1.90	6.1	3.90							0.25	0.35	0.125				
mm	nom	0.48	0.02	0.30	4.0	1.85	6.0	3.85	0.5	1	2.5	3	4.5	0.5	0.20	0.30	0.075	0.07	0.05	0.08	0.1
	min	0.46	0.00	0.25	3.9	1.80	5.9	3.80							0.15	0.25	0.025				

sot1134-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1134-1	- - -	- - -	- - -			~~08-12-17~~ 09-01-22

Fig 13. Package outline SOT1134-1 (HXQFN60U)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16374A v.11	20130116	Product data sheet	-	74LVC_LVCH16374A v.10
Modifications:	• Minor non-technical text changes and corrections • Document revision history correction			
74LVC_LVCH16374A v.10	20120301	Product data sheet	-	74LVC_LVCH16374A v.9
74LVC_LVCH16374A v.9	20111219	Product data sheet	-	74LVC_LVCH16374A v.8
74LVC_LVCH16374A v.8	20110621	Product data sheet	-	74LVC_LVCH16374A v.7
74LVC_LVCH16374A v.7	20100323	Product data sheet	-	74LVC_LVCH16374A v.6
74LVC_LVCH16374A v.6	20090212	Product data sheet	-	74LVC_LVCH16374A v.5
74LVC_LVCH16374A v.5	20031212	Product specification	-	74LVC_H16374A v.4
74LVC_H16374A v.4	19980317	Product specification	-	74LVC16374A_ 74LVCH16374A v.3
74LVC16374A_ 74LVCH16374A v.3	19980317	Product specification	-	74LVC16374A v.2
74LVC16374A v.2	19970822	Product specification	-	74LVC16374A v.1
74LVC16374A v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 January 2013
Document identifier: 74LVC_LVCH16374A