Evaluation Board User Guide
UG-071

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Setting Up the Evaluation Board for the ADCLK846

PACKAGE LIST

Evaluation board with components installed
Applicable documents (schematic and layout)

GENERAL DESCRIPTION

This user guide describes how to set up and use the evaluation board for ADCLK846. The ADCLK846 data sheet contains full technical details about the specifications and operation of this device and should be consulted when using the evaluation board.

The ADCLK846 is a high performance clock fanout buffer. The evaluation board is fabricated using a high quality Rogers® dielectric material. Transmission line paths are kept as close to 100 Ω differentially as possible.

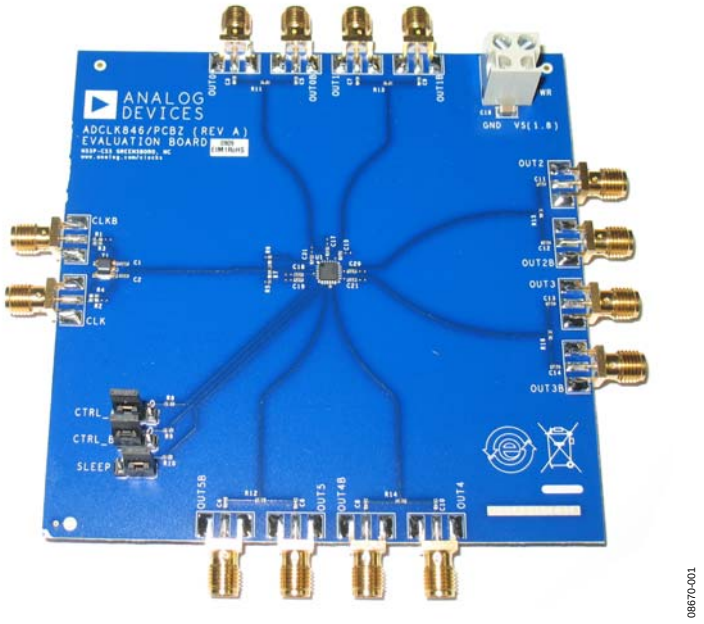

Figure 1. Evaluation Board

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REVISION HISTORY

12/09—Revision 0: Initial Version

RECOMMENDED BOARD SETUP

The recommended setup for the ADCLK846 evaluation board is shown in Figure 2. V_S is set to 1.8 V.

The CLK input is set up for single-ended-to-differential operation via the balun on the evaluation board. In addition, series capacitors (C3 and C4) in the path provide ac-coupled inputs to the ADCLK846.

The range of the peak-to-peak input voltage swing at CLK is 0.15 V to 1.8 V. Output jitter performance is degraded by input slew rate, as shown in the ADCLK846 data sheet.

Table 1. Basic Equipment Required

Quantity	Description
1	Single power supply
1	Signal source
1	High bandwidth oscilloscope
1	High bandwidth differential probe
2	Matched high speed cables

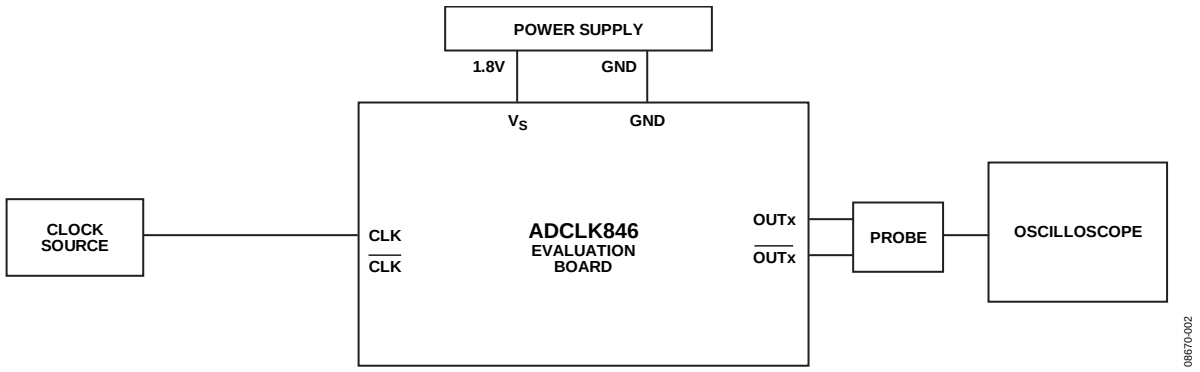

Figure 2. Recommended Setup for ADCLK846 Evaluation

CLOCK OUTPUTS

The ADCLK846 outputs are pin programmable up to 6 differential LVDS outputs or 12 single-ended 1.8 V CMOS outputs. Jumpers CTRL_A, CTRL_B, and SLEEP are used to configure the outputs. See Table 2 and Figure 3 for jumper assignments.

For high precision measurements, it is recommended to evaluate the nonlaunched outputs on the evaluation board. The nonlaunched outputs do not go to the SMA connectors. In this case, the ADCLK846 is physically close to the output load and avoids the issues of driving a 50 Ω cable. CMOS is not designed to operate in a 50 Ω environment.

The nonlaunched outputs have a full output swing with 100 Ω differential trace impedance into a 100 Ω resistor to minimize reflections. These outputs are set up to evaluate using a high bandwidth differential probe and oscilloscope. See the evaluation board schematic in Figure 4 for more details.

Outputs that go to a SMA connector may not have a full output swing, and reflections may be observed.

Table 2. Output Pin Assignment

Jumper Name	Jumper Setting	Affected Outputs
CTRL_A	Logic 0 = LVDS; Logic 1 = CMOS	Output 0 to Output 1
CTRL_B	Logic 0 = LVDS; Logic 1 = CMOS	Output 2 to Output 5
SLEEP	Logic 1 = sleep	Output 0 to Output 5

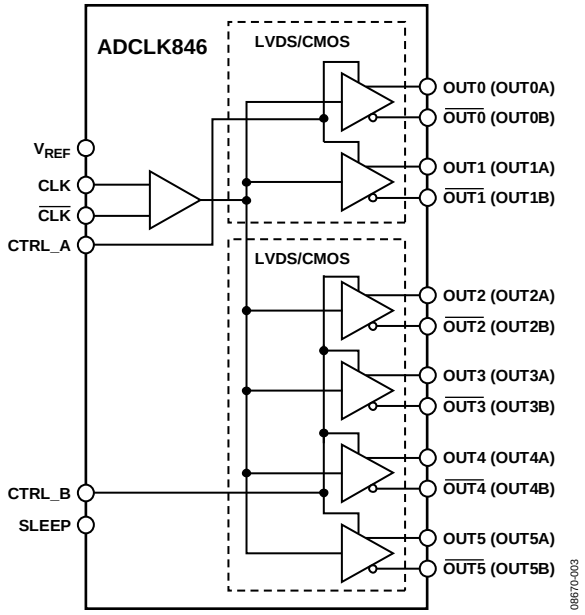

Figure 3. 1:6 Clock/Data Buffer Block Diagram

EVALUATION BOARD SCHEMATICS AND ARTWORK

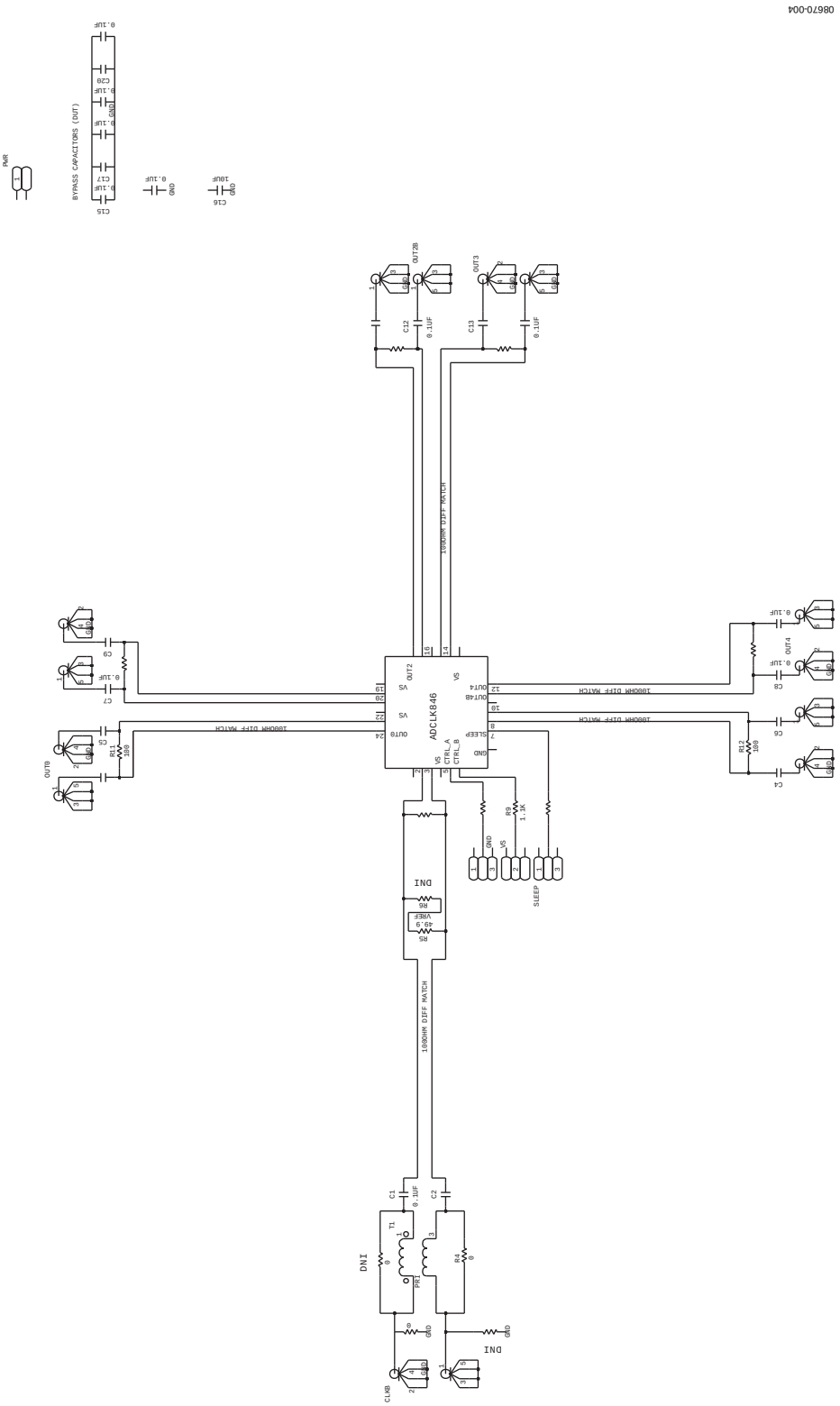

Figure 4. Evaluation Board Schematic

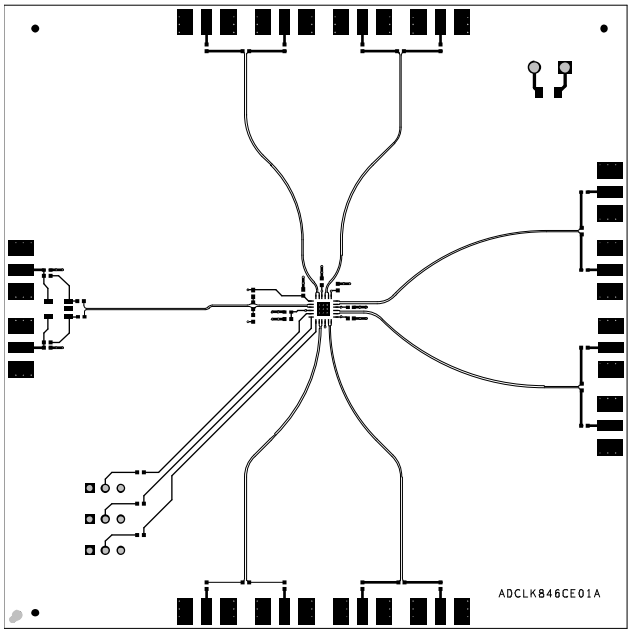

Figure 5. Top Trace Layer

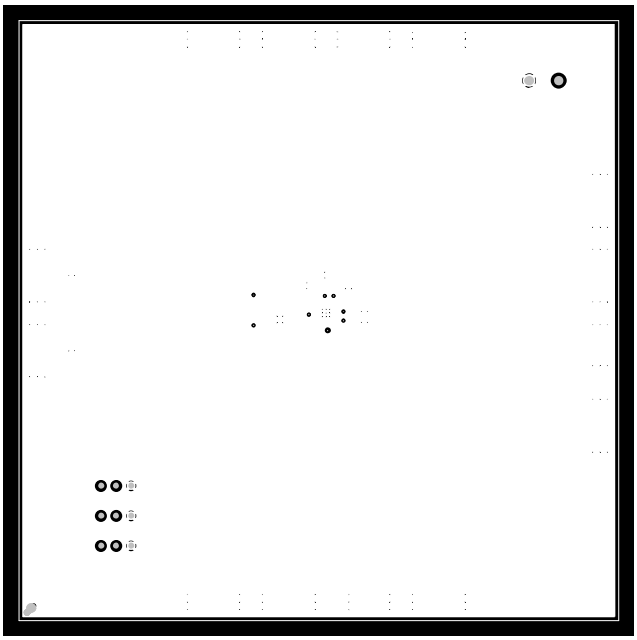

Figure 6. Ground Plane Layer

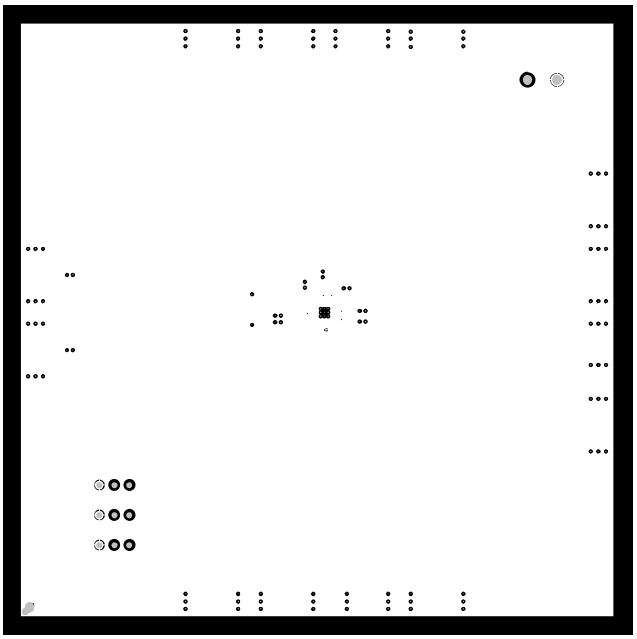

Figure 7. V_S Power Plane Layer

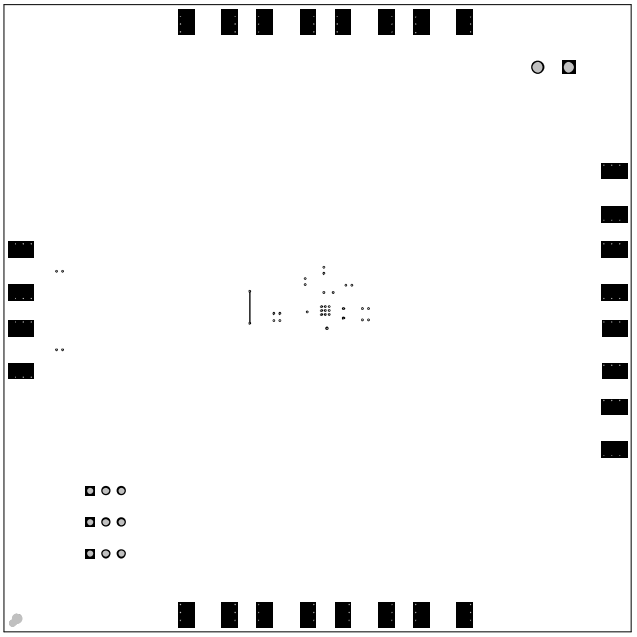

Figure 8. Bottom Trace Layer

NOTES

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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