LTC4263CS/LTC4263CDE

DESCRIPTION

Demonstration circuits 981A and 981B features the LTC4263 in single port Power Over Ethernet (PoE) Power Sourcing Equipment (PSE) Midspan and Endpoint solutions. The LTC4263 is an autonomous single-channel PSE controller for use in IEEE802.3af compliant PoE systems. It includes an on-board planar power MOSFET, internal inrush, current limit, and short circuit control, Powered Device (PD) detection and classification circuitry, and selectable AC or DC disconnect sensing. On-board control algorithms provide complete PSE Control operation without the need of a microcontroller. The LTC4263 simplifies

PSE implementation, needing only a single 48V supply and a small number of passive support components. Other options shown on the DC981A include Legacy PD detection enable, Midspan back off timer enable, power class enforce mode, power management enable. An LED for each port is driven by the respective LTC4263 to indicate the state of the port.

Design files for this circuit board are available. Call the LTC factory.

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PARAMETER	CONDITION VALUE		
Supply Voltage	Voltage for IEEE802.3af Compliance at Port Output	46V to 57V	
Midspan Mode Detection Backoff	Midspan Enabled, Failed Detection 3.2 seconds		
Detection Range	Valid IEEE802.3af PD Detection	17k to 29.7k	
Set Maximum Allocated Power	Power Management Enabled 17W		
Ethernet Powered Pairs Pinout	Endpoint PSE, Alternative A (MDI)	1/2(+), 3/6(-)	
	Midspan PSE, Alternative B	4/5(+) , 7/8 (-)	

Table 1. Typical DC981 Performance Summary $(T_A = 25^{\circ}C)$

QUICK START PROCEDURE

Demonstration circuit 981 is easy to set up to evaluate the performance of the LTC4263. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

- **1**. Place jumpers in the following positions:
 - JP1 EN
 - JP2 EN
 - JP3 DIS
 - JP4 AC
 - JP5 AC
 - JP6 EN

- 2. Insert daughter card (DC981B) to main board (DC981A) at polarized connector J3.
- 3. Apply 48V across VDD48 and VSS.
- 4. Connect a scope probe at VOUT_MD and VOUT_EP both referenced to positive rail VDD48.
- **5.** Connect a valid PD to either Midspan PSE or Endpoint PSE.
- 6. Connect a second PD to the open port.



Figure 1. Basic DC981A/B Equipment Setup

OPERATING PRINCIPLES

DC981 provides two implementations of a PSE controlled by the LTC4263, a Midspan PSE and an Endpoint PSE. A single 48V supply is all that is required to power the board. This in turn provides power to the Midspan PSE and Endpoint PSE outputs. On each solution, an LTC4263 provides detection of a PD, classification, power management, safe power on of the PD, port current limit, and disconnect detection.

Midspan PSE and Midspan Mode

In the Midspan solution, a device (router, switch, etc.) that does not have PoE is connected to MIDSPAN IN. Data is passed through to MIDSPAN OUT along with PoE which goes out to a PD. Power is applied directly to Ethernet pairs 4/5 and 7/8. The LTC4263 circuitry sits in a small layout area behind the RJ45 connector and switches power on the negative rail. To show the different functions of the LTC4263. jumpers allow for the user to select the options of AC or DC disconnect, legacy detection, Midspan backoff timing, and class enforcement. An LED that shows the status of the port is driven by a switcher in the LTC4263 to improve efficiency when VDD5 is provided internally. Push button switch SW1 ties the shutdown pin to ground to disable the LTC4263 in the Midspan solution.

A PSE implementing Alternative B pin out must back off from detection for at least 2 seconds after a failed attempt. This is to avoid conflict of Detection, for example, should a potential Endpoint PSE and Midspan PSE be connected to the same PD. To enable this feature, set JP2 to DIS. JP2 ties the MIDSPAN pin to VDD5 to enable the LTC4263 backoff timer or to VSS to disable. A 3.2 second delay occurs after every failed detect cycle unless the result is open circuit. If held at VSS, no delay occurs after failed detect cycles.

Endpoint PSE

The Endpoint solution is primarily shown on a small daughter card (DC981B). This card is the same height and width as the integrated RJ45 connector that it slides behind on the main board (DC981A). The RJ45 includes Ethernet magnetics and common mode termination. A layout option shows the same components can be placed under the same RJ45 connector. The minimum connections to the daughter card are VSS, VDD48 and VOUT. Power is switched over from the daughter card out to the Ethernet data pairs (1/2 and 7/8). A PHY can be connected to the "TO PHY" to pass data through to the data pairs along with PoE. LED drive and power management pins are also brought out for additional board functions. The board is set up for AC disconnect, but can be reworked for DC disconnect by removing components and replacing with shorts in certain locations. Two solder jumpers also provide selectable options for legacy detection and class enforce.

Power Management

The Midspan and Endpoint PSE, although separate solutions on the DC981, are tied together at the PWRMGT pin for demonstration of the LTC4263 power management capability. Programmable on-board power management circuitry allows multiple LTC4263s to allocate and share power in multi-port systems, allowing maximum utilization of the 48V power supply – all without the intervention of a host processor.

The LTC4263 sources current at the PWRMGT pin proportional to the class of the PD that it is powering. The voltage of this pin is checked before powering the port. The port will not turn on if this pin is more than 1V above VSS. The PWRMGT pins of the LTC4263s are tied together and connect to a resistor (RPM) and capacitor (CPM) in parallel to VSS to implement power management among multiple ports. This resistor is selected with the following equation:

$R_{_{PM}} = 213k * W / P_{_{FULL_LOAD}}$

On the DC981A, the default $R_{_{PM}}$ is 12.4k for a full load power of 17W.



PD CLASS	POWER REQUEST	IPM (TYP)	VPM*	
Class 1	4W	19µA	236mV	
Class 2	7W	33µA	409mV	
Class 0, 3, or 4	15.4W	73µA	905mV	

Table 2. Power Management Voltage

 $R_{PM} = 12.4k$

Table 3. Powered Device Combinations

PD COMBINATION	1 ^{s⊤} PD	2 [™] PD
Class 1 / Class 1	Powered	Powered
Class 1 / Class 2	Powered	Powered
Class 1 / Class 3**	Powered	Power Denied
Class 2 / Class 2	Powered	Powered
Class 2 / Class 3**	Powered	Power Denied
Class 3 **/ Class 3**	Powered	Power Denied

**Class 3 substitutable with Class 0 or 4.

If power management is not used, move JP6 to DIS to tie the PWRMGT pins to VSS and disable this feature.

Class Enforce Mode

ENFORCE CLASS jumper JP1 ties the ENFCLS pin of the LTC4263 to either VDD5 or VSS to respectively enable or disable class enforce current limits. If held at VDD5, the LTC4263 will reduce the ICUT threshold for Class 1 or Class 2 PDs. If ENFCLS is held at VSS, ICUT remains at 375mA (typical) for all classes.

Table 4.	Port	Current	Limit	Accordina	to	Class
14810 11		• • • • • • • • •			•••	0.000

PD CLASS	CUBBENT THRESHOLD (TYPICAL)
Class 1	100mA
Class 2	175mA
Class 0, 3, 4, or Class En- force Disabled	375mA

LED Drive

An LED pin indicates the state of the port controlled by the LTC4263. When the port is powered, the LED is on; when disconnected or detecting, the LED is off. If an invalid signature is detected or a fault occurs, the LED will flash a pattern that the user or host system can read to indicate the nature of the problem. When run from a single 48V supply, the LED pin can operate as a simple switching current source to reduce power dissipation in the LED drive circuitry.

VDD5 Option

The logic 5V power supply can be supplied from the internal LTC4263 5V supply or an external 5V supply when above the internal supply. If the internal regulator is used, this pin should only be connected to the bypass capacitor and to any logic pins of the LTC4263 that are being held at VDD5.

AC and DC Disconnect

AC and DC disconnect are two different methods of detecting whether a valid PD is present and requires power. AC disconnect is the default method for the DC981 but can be converted to DC disconnect in the Midspan solution through two jumpers. Moving DISCON (JP4) to DC will short the ACCOUT pin to VSS and configure the LTC4263 to DC disconnect. Moving jumper setting for ACCOMP (JP5) to DC by-passes the AC blocking diode and removes the RC used for AC disconnect from the main circuit.

Legacy Detection

LEGACY jumper JP3 controls whether legacy detect is enabled. If the LEGACY pin is held at VDD5 (EN selected), legacy detect is enabled and testing for a large capacitor is performed to detect the presence of a legacy PD on the port. If held at VSS (DIS selected), only IEEE 802.3af compliant PDs are detected. If left floating (no jumper), the LTC4263 enters force-power-on mode and any PD that generates between 1V and 10V when biased with 270µA of detection current will be powered as a legacy device. This mode is useful if the system uses a differential detection scheme to detect legacy devices. Warning: Legacy modes are not IEEE 802.3af compliant.











