

Introduction

The ISL59446EVAL1 evaluation board contains all the circuitry needed to characterize critical performance parameters of the ISL59446 500MHz triple 4:1 MUX-amplifiers over a variety of applications.

The ISL59446 contains 3 separate 4:1 high impedance input multiplexers, each followed by a non-inverting output current-feed amplifier set to a fixed gain of 2. A common set of logic inputs is provided (Figure 1, Table 1). Control features include a high speed (20ns) HIZ output control for individual selection of MUX amps that share a common video output line. The ENABLE control can be used to save power by powering the device down.

The evaluation board circuit and layout is optimized for either 50Ω or 75Ω terminations, and implements a basic R-G-B video 4 input MUX-amp. The board is supplied with 75Ω input signal terminations and a 75Ω back-termination resistor on each of the 3 outputs. The internally set gain of 2 compensates for the output termination gain reduction when terminated into a 75Ω load. The user has the option of replacing the 75Ω resistors with 50Ω resistors for other applications. The control lines contain 50Ω resistors to match the 50Ω output impedance of high speed pulse generators. Control line termination resistors are recommended for rise and fall times under 10ns to minimize unwanted transients. If DC is used for the control logic, the resistors may be removed; or the applied DC voltage can be reduced to 2.5V to reduce the dissipation in the termination resistor.

The layout contains component options to include an output series resistor (R_S) followed by a parallel resistor (R_L) capacitor (C_L) network to ground. This option allows the user to select several different output configurations. Examples are shown in Figures 2A, 2B, and 2C. The evaluation board is supplied with the 75Ω back termination resistors shown in Figure 2C.

Amplifier Performance and Output Configurations

The EL4342 output amplifiers are designed for maximum gain-bandwidth performance when loaded with ~500Ω (R_L) in parallel with ~5pF (C_L) to ground, directly at the output pin (Figure 2A). They are ideally suited for driving high impedance high speed selectable-gain buffers when gain compensation is needed. In these applications, output trace capacitance to 5pF actually optimizes AC performance. For trace capacitance below 5pF, an additional capacitor between the output pin to ground may be added to achieve the 5pF optimum. GBW decreases slightly at the lower output load impedances typical of back-terminated cable driving applications. Additional performance data can be found in the data sheet references.

High Frequency Layout Considerations

At frequencies of 500MHz and higher, circuit board layout may limit performance. The following layout guidelines are implemented on the evaluation board:

- Signal I/O lines are the same lengths and widths to match propagation delay and trace parasitics.
- No series connected vias are used in signal I/O lines, as they can add unwanted inductance.
- Signal trace lengths are minimized to reduce transmission line effects and the need for strip-line tuning of the signal traces.
- High frequency decoupling caps are placed as close to the device power supply pin as possible - without series vias between the capacitor and the device pin.

Power Sequencing

Proper power supply sequencing is -V first, then +V. In addition, the +V and -V supply pin voltage rate-of-rise must be limited to $\pm 1V/\mu s$ or less. The evaluation board contains parallel-connected low Von Schottky diodes on each supply terminal to minimize the risk of latch up due to incorrect sequencing. In addition, extra 10μF decoupling capacitors are added to each supply to aid in reducing the applied voltage rate-of-rise.

Reference Documents

1. ISL59446 Data Sheet, FN6261

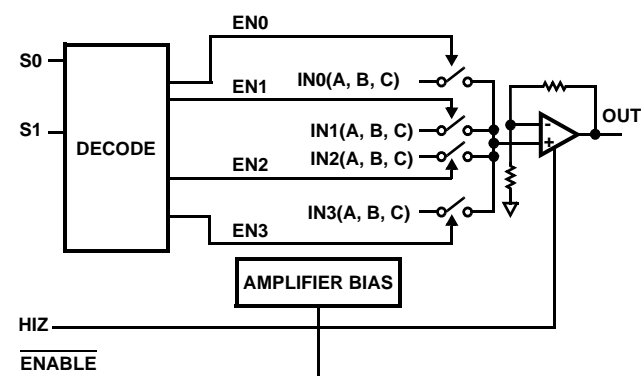
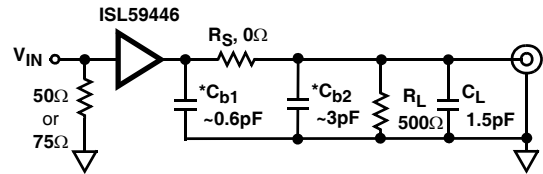


FIGURE 1. ISL59446 FUNCTIONAL BLOCK DIAGRAM
(1 OF 3 CHANNELS)

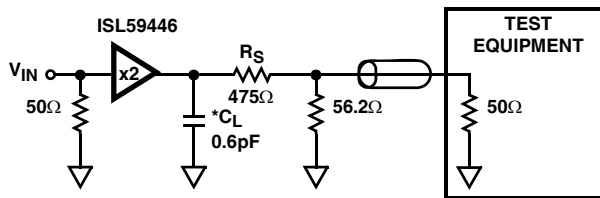
TABLE 1. LOGIC TABLE

S0	S1	HIZ	ENABLE	OUTA, B, C
0	0	0	0	IN0A, B, C
1	0	0	0	IN1A, B, C
0	1	0	0	IN2A, B, C
1	1	0	0	IN3A, B, C
-	-	1	0	HIZ
-	-	-	1	Power-Down



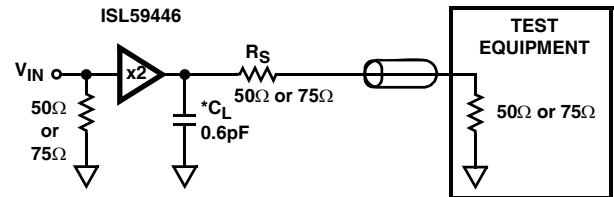
* Cb1, Cb2 are approximate PCB trace capacitances

FIGURE 2A. TEST CIRCUIT FOR INTER-STAGE APPLICATION WITH OPTIMAL OUTPUT LOAD



*CL Includes PCB trace capacitance

FIGURE 2B. TEST CIRCUIT FOR 500Ω LOAD USING 50Ω TERMINATIONS

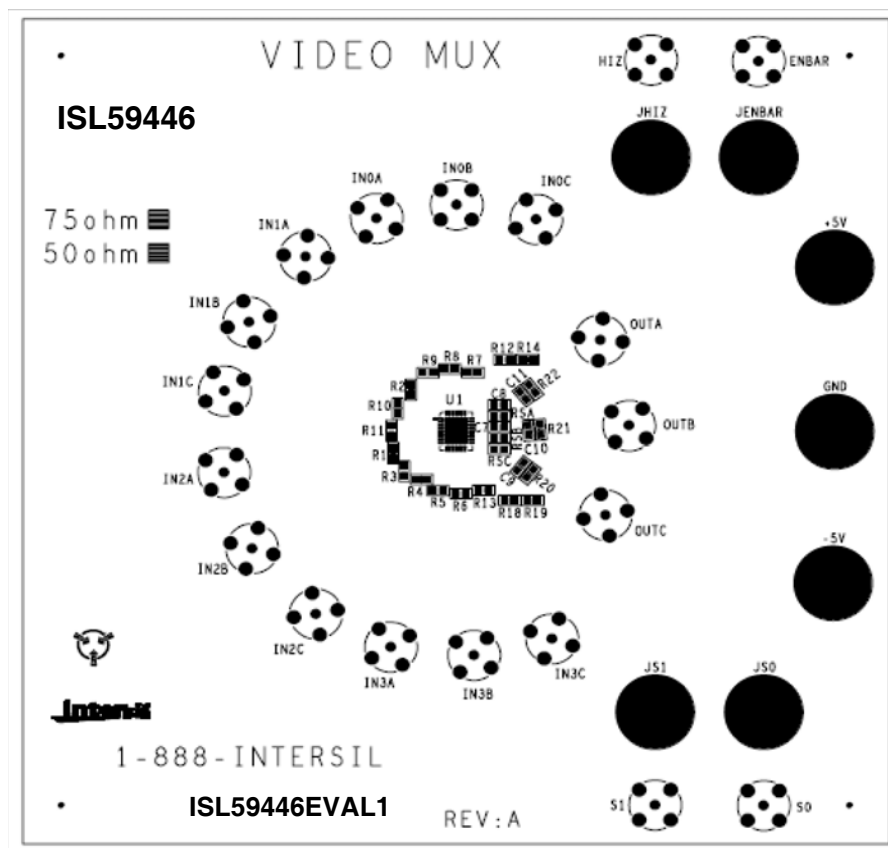


*CL is approximate PCB trace capacitance

FIGURE 2C. BACK-TERMINATED TEST CIRCUIT FOR CABLE APPLICATION

ISL59446EVAL1

TOP VIEW



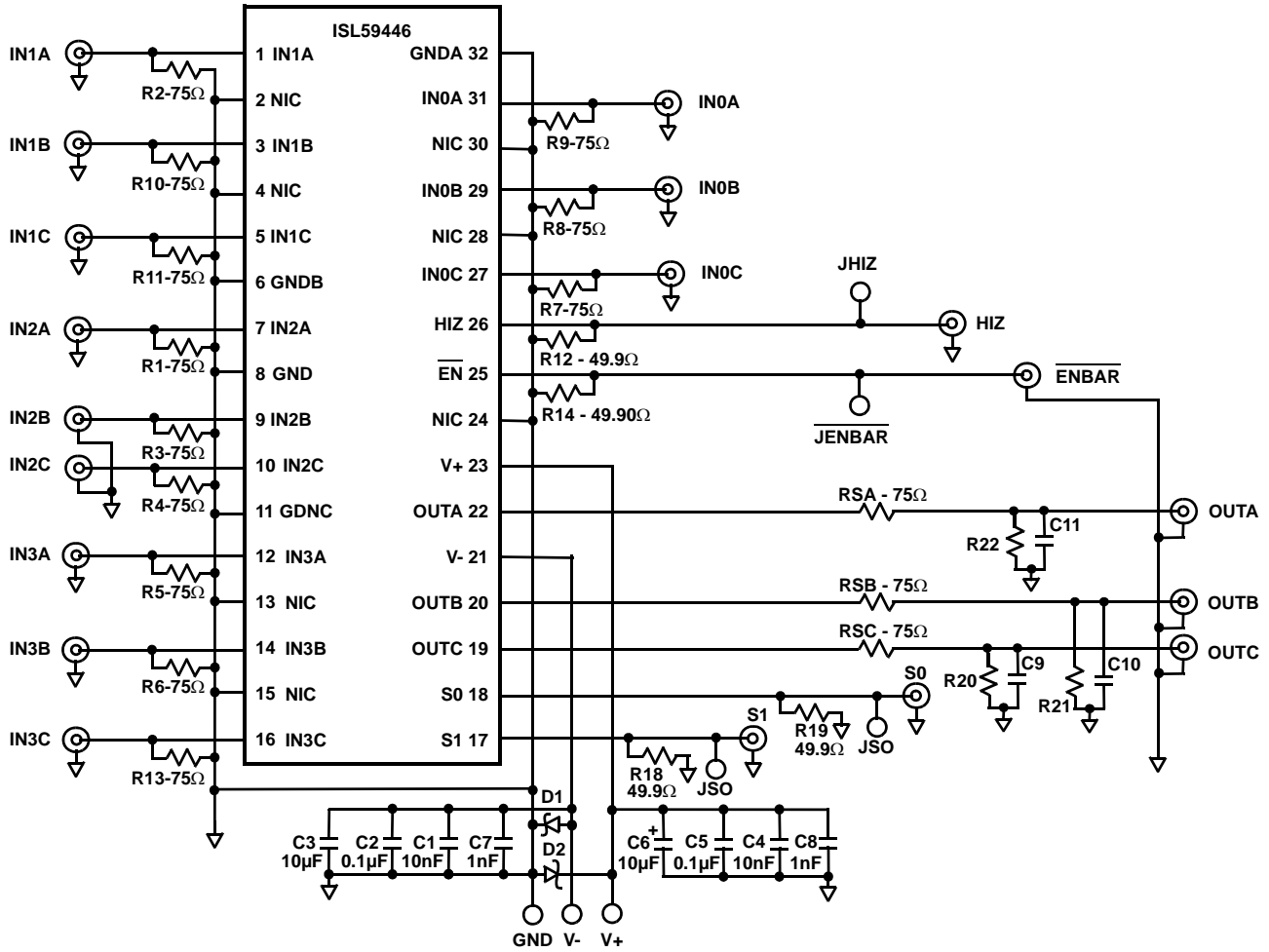


FIGURE 3. ISL59446EVAL1 SCHEMATIC DIAGRAM

TABLE 2. COMPONENTS PARTS LIST

DEVICE #	DESCRIPTION	COMMENTS
C7, C8	Cap, SMD, 0603, 1000pF, 25V, 10%, X7R	Power Supply Decoupling
C1, C4	Cap, SMD, 0603, 0.01μF, 25V, 10%, X7R	Power Supply Decoupling
C2, C5	Cap, SMD, 0603, 0.1μF, 25V, 10%, X7R	Power Supply Decoupling
C3, C6	Cap, SMD, 0805, 10μF, 6.3V, 10%, X5R	Power Supply Decoupling
D1, D2	Diode-Schottky, 2 Pin, 45V, 7.5A	MBR0550T (Motorola) reverse polarity protection
R1-R11, R13, RSA, RSB, RSC	Resistor, SMD, 0603, 75Ω, 1/10W, 1%	Signal input/output termination
R12, R14, R18, R19	Resistor, SMD, 0603, 49.9Ω, 1/16W, 1%	Logic input termination
C9, C10, C11	Capacitor, SMD, 0603	Optional, not populated
R20, R21, R22	Resistor, SMD, 0603	Optional, not populated
U1	ISL59446IR -500MHz Multiplexing Amplifier, 32P, QFN	Device under test

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

For information regarding Intersil Corporation and its products, see www.intersil.com