Freescale Semiconductor
Technical Data

Document Number: MC33810
Rev. 10.0, 4/2011

RoHS

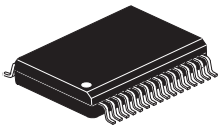
Automotive Engine Control IC

33810

ENGINE CONTROL

The 33810 is an eight channel output driver IC intended for automotive engine control applications. The IC consists of four integrated low side drivers and four low side gate pre-drivers. The low side drivers are suitable for driving fuel injectors, solenoids, lamps, and relays. The four gate pre-drivers can function either as ignition IGBT gate pre-drivers or as general purpose MOSFET gate pre-drivers.

When configured as ignition IGBT gate pre-drivers, additional features are enabled such as spark duration, dwell time, and ignition coil current sense. When configured as a general purpose gate pre-driver, the 33810 provides external MOSFETs with short circuit protection, inductive flyback protection and diagnostics. The device is packaged in a 32 pin (0.65mm pitch) exposed pad SOIC.



EK SUFFIX (Pb-FREE)
98ASA10556D
32 PIN SOICW EP

Features

- Designed to operate over the range of 4.5V ≤ VPWR ≤ 36V
- Quad ignition IGBT or MOSFET gate pre-driver with Parallel/SPI and/or PWM control
- Quad injector driver with Parallel/SPI control
- Interfaces directly to MCU using 3.3V/5.0V SPI protocol
- Injector driver current limit - 4.5A max.
- Independent fault protection and diagnostics
- VPWR standby current 10μA max.
- Pb-free packaging designated by suffix code EK

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33810EK/R2	-40°C to 125°C	32 SOICW-EP

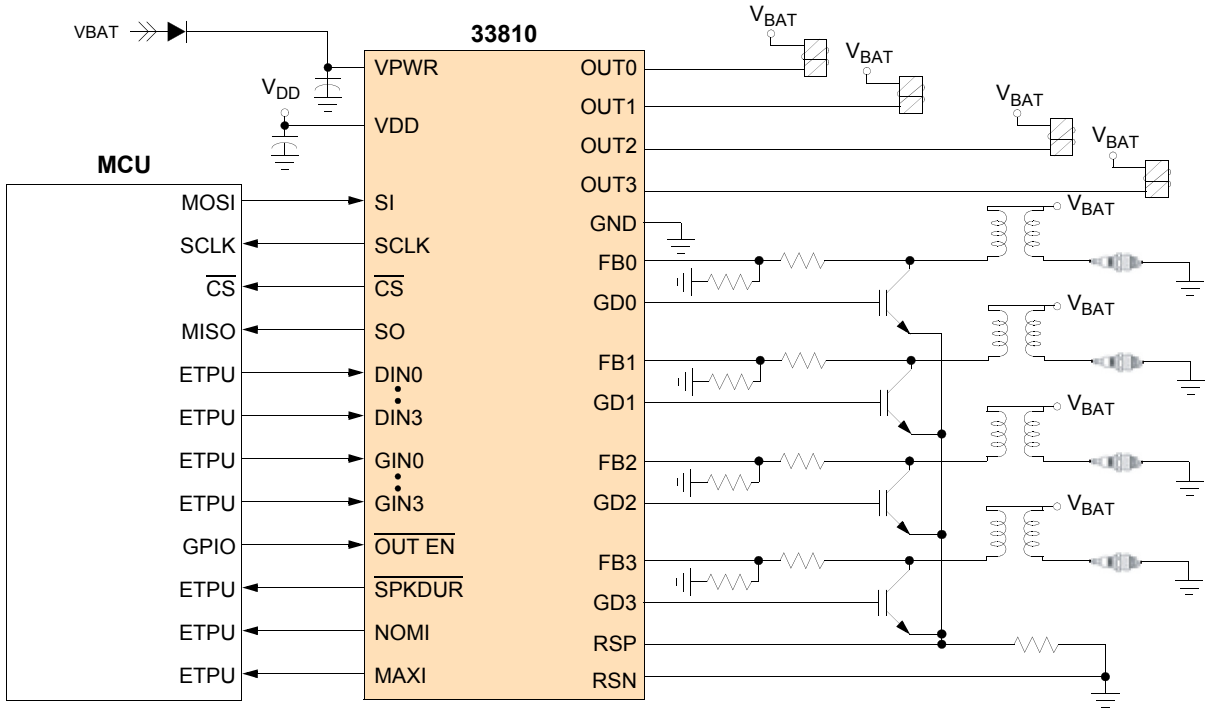


Figure 1. MC33810 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

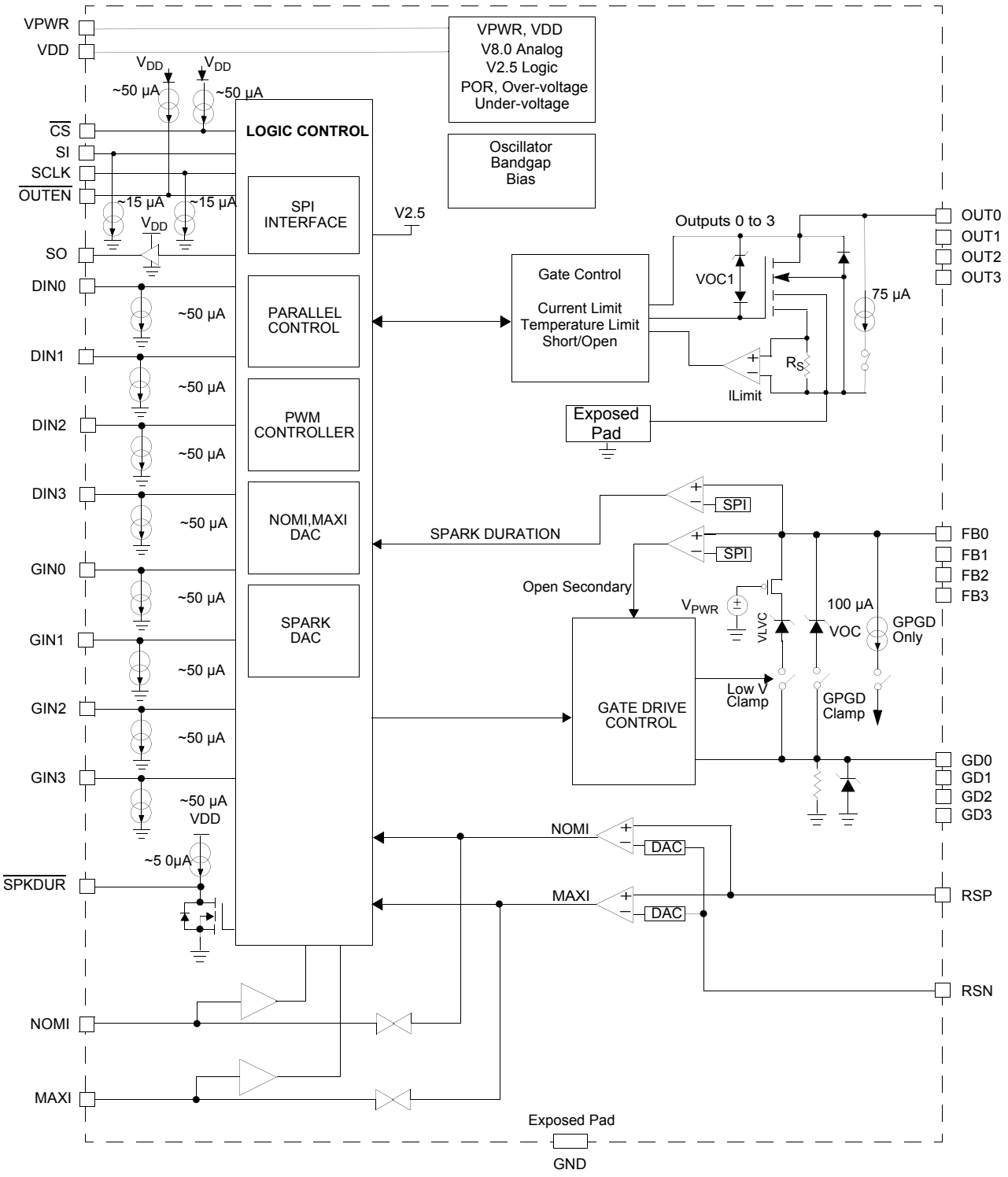


Figure 2. 33810 Simplified Internal Block Diagram

PIN CONNECTIONS

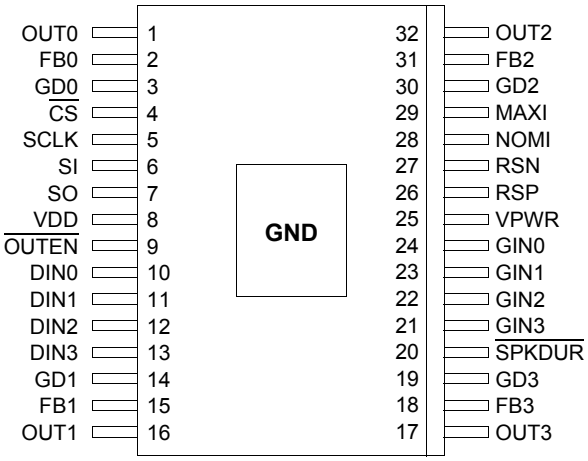


Figure 3. 33810 Pin Connections

Table 1. 33810 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
8	VDD	Input	Digital Logic Supply Voltage	The VDD input supply voltage determines the interface voltage levels between the device and the MCU, and is used to supply power to the Serial Out buffer (SO), SPKDUR buffer, MAXI, NOMI, and pull-up current source for the Chip Select (CS).
6	SI	Input	Serial Input Data	The SI input pin is used to receive serial data from the MCU.
5	SCLK	Input	Serial Clock Input	The SCLK input pin is used to clock in and out the serial data on the SI and SO pins, while being addressed by the CS.
4	CS	Input	Chip Select	The Chip Select input pin is an active low signal sent by the MCU to indicate that the device is being addressed. This input requires CMOS logic levels and has an internal active pull-up current source.
7	SO	Output	Serial Output Data	The SO output pin is used to transmit serial data from the device to the MCU.
10, 11, 12, 13	DIN0,DIN1, DIN2,DIN3	Input	Driver Input 0, Driver Input 1, Driver Input 2, Driver Input 3	Active HIGH input control for injector outputs OUT0 - 3. The parallel input data is logically OR'd with the corresponding SPI input data register contents.
24, 23, 22, 21	GIN0,GIN1, GIN2,GIN3	Input	Gate Driver Input 0 Gate Driver Input 1 Gate Driver Input 2 Gate Driver Input 3	These pins are the active HIGH input control for IGBT/General Purpose Gate Driver outputs 0 - 3. The parallel input data is logically OR'd with the corresponding SPI input data register contents in General Purpose Mode Only.
20	SPKDUR	Output	Spark Duration Output	This pin is the Spark Duration Output. This open drain output is low while feedback inputs FB0 through FB3 are above the programmed spark detection threshold.
25	VPWR	Input	Analog Supply Voltage	VPWR is the main voltage input for all internal analog bias circuitry.
Exposed Pad (bottom of package)	GND	Ground	Ground	The exposed pad is the only ground reference for analog, digital and power ground connections. As such, it must be soldered directly to a low impedance ground plane for both electrical and thermal considerations. For more information about this package, please see application note AN2409 on the Freescale Web site, www.freescale.com

Table 1. 33810 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
9	$\overline{\text{OUTEN}}$	Input	Output Enable	The Output Enable pin ($\overline{\text{OUTEN}}$) is an active low input. When the $\overline{\text{OUTEN}}$ pin is low, the device outputs are active. The outputs are disabled when $\overline{\text{OUTEN}}$ is high.
29	MAXI	Output	Maximum Ignition Coil Current	This pin is the Maximum Ignition Coil Current output flag. This output is asserted when the IGBT Collector-Emitter current exceeds the selected level of the DAC. This signal also latches off the gate pre-drive outputs when configured as a General Purpose Gate pre-Driver. The MAXI current level is determined by the voltage drop across an external sense resistor connected to pins RSP and RSN.
28	NOMI	Output	Nominal Ignition Coil Current	This pin is the Nominal Ignition Coil Current output flag. This output is asserted when the IGBT Collector-Emitter current exceeds the level selected by the DAC.
2, 15, 31, 18	FB0 - FB3	Input	Feedback Voltage Sense	In IGBT ignition gate pre-driver mode, these feedback inputs monitor the IGBT's collector voltage to provide the spark duration timer control signal.
3, 14, 30,19	GD0 -GD3	Output	Gate Drive Output	IGBT/General Purpose Gate pre-driver outputs are controlled by $\overline{\text{GIN0}}$ - $\overline{\text{GIN3}}$. Pull-up and pull-down current sources are used to provide a controlled slew rate to an external IGBT or MOSFET connected as a low side driver.
26	RSP	Input	Resistor Sense Positive	This pin is the Positive input of a current sense amplifier.
27	RSN	Input	Resistor Sense Negative	This pin is the Negative input of a current sense amplifier.
1, 16, 32, 17	OUT0 -OUT3	Output	Low Side Injector Driver Output	These pin are the Open drain low side injector driver outputs.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
VPWR Supply Voltage[1]	V_{PWR}	-1.5 to 45	V_{DC}
VDD Supply Voltage[1]	V_{DD}	-0.3 to 7.0	V_{DC}
SPI Interface and Logic Input Voltage ($\overline{CS}$, SI, SO, SCLK, $\overline{OUTEN}$, DIN0 - DIN3, GIN0 - GIN3, $\overline{SPKDUR}$, NOMI, MAXI, RSP,RSN)	V_{IL} V_{IH}	-0.3 to VDD	V_{DC}
IGBT/General Purpose Gate Pre-driver Drain Voltage (V_{FB0} to V_{FB3})	V_{FB}	-1.5 to 60	V_{DC}
Injector Output Voltage (OUTx)	V_{OUTX}	-1.5 to 60	V_{DC}
General Purpose Gate Pre-driver Output Voltage (GDx)	V_{GDx}	-0.3 to 10	V_{DC}
Output Clamp Energy (OUT0 to OUT3)(Single Pulse) $T_{JUNCTION}$ = 150°C, I_{OUT} = 1.5 A	E_{CLAMP}	100	mJ
Output Clamp Energy (OUT0 to OUT3)(Continuous Pulse) $T_{JUNCTION}$ = 125°C, I_{OUT} = 1.0 A (Max Injector frequency is 70 Hz)	E_{CLAMP}	100	mJ
Output Continuous Current (OUT0 to OUT3) $T_{JUNCTION}$ = 150°C	I_{OSSSS}	2.0	A
Maximum Voltage for RSN and RSP inputs	V_{RSX}	-0.3 - VDD	V_{DC}
Frequency of SPI Operation (VDD = 5.0 V)	–	6.0	MHz
ESD Voltage[2], [3] Human Body Model (HBM) Machine Model (MM) Charge Device Model (CDM)	 V_{ESD1} V_{ESD2} V_{ESD3}	 ±2000 ±200 ±750	V
THERMAL RATINGS			
Operating Temperature Ambient Junction2 Case	 T_A T_J T_C	 -40 to 125 -40 to 150 -40 to 125	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Power Dissipation (T_A = 25°C)	P_D	1.7	W
Peak Package flow Temperature During Solder Mounting DWB Suffix EW Suffix	T_{SOLDER}	 240 245	°C
Thermal Resistance Junction-to-Ambient Junction- to-Lead Junction-to-Flag	 $R_{\theta JA}$ $R_{\theta JL}$ $R_{\theta JC}$	 75 8.0 1.2	°C/W

Table 2. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted.

Ratings	Symbol	Value	Unit

Notes
1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD testing is performed in accordance with the Human Body Model (HBM) (AEC-Q100-002), the Machine Model (MM) (AEC-Q100-003), and the Charge Device Model (CDM), Robotic (AEC-Q100-011).

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where typical values reflect the parameter's approx. average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VDD, VPWR)					
Supply Voltage[4] Fully Operational Full Parameter Specification	$V_{PWR(FO)}$	 4.5 6.0	 –	 36 32	V
Supply Current All Outputs Disabled (Normal Mode)	$I_{VPWR(ON)}$	 –	 10.0	 14.0	mA
Sleep State Supply Current (Must have V_{DD} ≤ 0.8 V for sleep state), V_{PWR} = 32 V	$I_{VPWR(SS)}$	 –	 15	 30	μA
V_{PWR} Over-voltage Shutdown Threshold Voltage[5]	$V_{PWR(OV)}$	36.5	39	42	V
V_{PWR} Over-voltage Shutdown Hysteresis Voltage	$V_{PWR(OV-HYS)}$	0.5	1.5	3.0	V
V_{PWR} Under-voltage Shutdown Threshold Voltage[6]	$V_{PWR(UV)}$	3.0	4.0	4.4	V
V_{PWR} Under-voltage Shutdown Hysteresis Voltage	$V_{PWR(UV-HYS)}$	100	200	300	mV
V_{PWR} Low Operating Voltage (Low-voltage reported via the SPI)[7]	$V_{PWR(LOV)}$	5.3	–	8.99	V
VDD Supply Voltage	V_{DD}	3.0	–	5.5	V
VDD Supply Current Static Condition and does not include VDD current out of device	I_{VDD}	 –	 –	 1.0	mA
VDD Supply Under-voltage (Sleep State) Threshold Voltage[8]	$V_{DD(UV)}$	0.8	2.5	2.8	V
INJECTOR DRIVER OUTPUTS (OUT 0:3)					
Drain-to-Source ON Resistance I_{OUT} = 1.0 A, T_J = 125°C, VPWR = 13 V I_{OUT} = 1.0 A, T_J = 25°C, VPWR = 13 V I_{OUT} = 1.0 A, T_J = -40°C, VPWR = 13 V	$R_{DS(ON)}$	 – – –	 – 0.2 –	 0.3 – –	Ω
Output Self Limiting Current	$I_{OUT(LIM)}$	3.0	–	6.0	A
Output Fault Detection Voltage Threshold[9] Outputs Programmed OFF (Open Load) Outputs Programmed ON (Short to Battery)	$V_{OUT(FLT-TH)}$	 2.0	 2.5	 3.0	V
Output OFF Open Load Detection Current V_{DRAIN} = 18 V, Outputs Programmed OFF V_{DRAIN} = 32 V, Outputs Programmed OFF (-40°C)	$I_{(OFF)OCO}$	 40	 75	 115 115	μA
Output ON Open Load Detection Current Current less then specification value considered open	$I_{(ON)OCO}$	 20	 100	 200	mA

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where typical values reflect the parameter's approx. average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit

Notes

4. These parameters are guaranteed by design, but not production tested. Fully operational means driver outputs will toggle as expected with input toggling. SPI is guaranteed to be operational when VPWR > 4.5 V. SPI may not report correctly when VPWR < 4.5 V.
5. Over-voltage thresholds minimum and maximum include hysteresis.
6. Under-voltage thresholds minimum and maximum include hysteresis.
7. Device is functional provided T_J is less than 150°C. Some table parameters may be out of specification.
8. Device in Sleep State, returns from sleep state with power on reset.
9. Output fault detection thresholds with outputs programmed OFF. Output fault detect thresholds are the same for output open and shorts.

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where typical values reflect the parameter's approx. average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
INJECTOR DRIVER OUTPUTS (OUT 0:3) (Continued)					
Output Clamp Voltage 1 I_D = 20 mA	V_{OC1}	48	53	58	V
Output Leakage Current VDD = 5.0 V, V_{DRAIN} = 24 V, Open Load Detection Current Disabled VDD = 5.0 V, V_{DRAIN} = V_{OC} - 1.0 V, Open Load Detection Current Disabled VDD = 0 V, V_{DRAIN} = 24 V, Sleep State	$I_{OUT(LKG)}$	 – – –	 – – –	 20 3000 10	µA
Over-temperature Shutdown[10]	T_{LIM}	155	–	185	°C
Over-temperature Shutdown Hysteresis[10]	$T_{LIM(HYS)}$	5.0	10	15	°C
IGNITION (IGBT) GATE DRIVER PARAMETERS (GD 0:3 FB0:3)					
Gate Driver Output Voltage I_{GD} = 500 µA I_{GD} = -500 µA	 $V_{GS(ON)}$ $V_{GS(OFF)}$	 4.8 0	 7.0 0.375	 9.0 0.5	V
Sleep Mode Gate to Source Resistor	$R_{GS(PULLDOWN)}$	100	200	300	KΩ
Sleep Mode FBx pin Leakage Current VDD = 0 V, V_{FBx} = 24 V,	$I_{FBX(LKG)}$	–	–	1.0	µA
Feedback Sense Current (FBx Input Current) FBx = 32 V, Outputs Programmed OFF	$I_{FBX(FLT-SNS)}$			1.0	µA
Gate Drive Source Current (1 ≤ V_{GD} ≤ 3)	$I_{GATEDRIVE}$	650	780	950	µA
Gate Drive Turn Off Resistance	$R_{DS(ON)}$	500	–	1000	Ω
SOFT SHUTDOWN FUNCTION (VOLTAGES REFERENCED TO IGBT COLLECTOR)					
Low Voltage Flyback Clamp Driver Command Off, Soft Shutdown Enabled, GDx = 2.0 V	V_{LVC}	VPWR +9.0	VPWR +11	VPWR + 13	V
Spark Duration Comparator Threshold (referenced to IC Ground Tab) Rising Edge Relative to VPWR	$V_{TH-RISE}$	18	21	24	V
Spark Duration Comparator Threshold (referenced to IC Ground Tab)[11] Falling Edge Relative to VPWR, Default = 5.5 V Assuming ideal external 10:1 voltage divider. Voltage measured at high end of divider, not at pin. Tolerance of divider not included	$V_{TH-FALL}$	1.2 4.9 7.4 9.9	2.75 5.5 8.2 11.00	3.6 6.1 9.1 12.1	V
Open Secondary Comparator Threshold (referenced from primary to Rising Edge Relative to GND. No hysteresis with 10:1 voltage divider.	$V_{TH-RISE}$	11.5	–	15.5	V
CURRENT SENSE COMPARATOR (RSP, RSN)					
NOMI Trip Threshold Accuracy - Steady State Condition 3.0 A across 0.02 Ω (RSP - RSN = 60 mV) 10.75 A across 0.04 Ω (RSP - RSN = 430 mV)	$NOMI_{TRIPTA}$	-10	–	10	%

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where typical values reflect the parameter's approx. average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit

Notes

10. This parameter is guaranteed by design, however is not production tested.
11. Assuming Ideal external 10:1 Voltage Divider. Tolerance of 10:1 Voltage Divider is not included. Voltage is measured on the High End of Divider - not at the pin. 10:1 N.3.A 10:1 Voltage Divider is produced using two resistors with a 9:1 resistance ratio by the basic formula:

$$\frac{VOUT}{VIN} = \frac{R1}{R1 + R2} \quad \text{Where R2 = 9XR1}$$

CURRENT SENSE COMPARATOR (RSP, RSN) (CONTINUED)					
MAXI Trip Threshold Accuracy Steady State Condition 6.0 A across 0.02 Ω (RSP - RSN = 120 mV) 21 A across 0.04 Ω (RSP - RSN = 840 mV)	$MAXI_{TRIPTA}$	-7.5	–	7.5	%
MAXI Trip Point During Overlapping Dwell	$MAXI_{TRIPOD}$	-35	–	+35	%
Input Bias Current RSP and RSN	$I_{BIASRSX}$	-50	–	50	µA
Comparator Hysteresis Voltage NOMI MAXI	$NOMI_{HYS}$ $MAXII_{HYS}$	40 40	– –	70 70	% of VT
Input Voltage Range (Maximum voltage between RSN and RSP)(12)	$VCMVR_{CMVR}$	0.0	–	2.0	V
Ground Offset Voltage Range(12) Maximum offset between RSN pin and IC Ground (Exposed Pad)	$VGND_{OVR}$	-0.3	–	0.3	V
GENERAL PURPOSE GATE DRIVER PARAMETERS (GD 0:3)					
Gate Drive Sink and Source Current	I_{GD}	1.0	2.0	5	mA
Gate Drive Output Voltage I_{GD} = 1.0 mA I_{GD} = -1.0 mA	$V_{GS(ON)}$ $V_{GS(OFF)}$	4.8 0.0	7.0 0.2	9.0 0.5	V V
Short to Battery Fault Detection Voltage Threshold V_{DD} = 5.0 V, Outputs Programmed ON Programmable from 0.5 to 3.0 V in 0.5 V increments. (Table 14)	$V_{DS(FLT-TH)}$	-35%		+35%	V
Open Fault Detection Voltage Threshold (referenced to IC ground tab) V_{DD} = 5.0 V, Outputs Programmed OFF	$V_{DS(FLT-TH)}$	2.0	2.5	3.0	V
Output OFF Open Load Detection Current FBx = 18 V, Outputs Programmed OFF	$I_{FBX(FLT-SNS)}$	50	75	120	µA
Output Clamp Voltage Driver Command Off, Clamp Enabled, V_{GATE} = 2.0 V	V_{OC}	48	53	58	V
DIGITAL INTERFACE					
Input Logic High-voltage Thresholds	V_{IH}	0.7 x V_{DD}	–	V_{DD} + 0.3	V
Input Logic Low-voltage Thresholds	V_{IL}	GND - 0.3	–	0.2 x V_{DD}	V
Input Logic-voltage Hysteresis	V_{HYS}	100	–	400	mV
Input Logic Capacitance	C_{IN}	–	–	20	pF
Sleep Mode Input Logic Current V_{DD} = 0 V	I_{LOGIC_SS}	-10	–	10	µA

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where typical values reflect the parameter's approx. average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
Input Logic Pull-down Current 0.8 to 5.0 V (DIN_X and GIN_X)	I_{LOGIC_PD}	30	50	100	μA

Notes

12. This parameter is guaranteed by design, however it is not production tested.

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where typical values reflect the parameter's approx. average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE (CONTINUED)					
Input Logic Pull-down Current 0.8 to 5.0 V (SI)	I_{SI_PD}	5.0	15	25	µA
Input Logic Pull-up Current on $\overline{OUT\_EN}$ $\overline{OUT\_EN}$ = 0.0 V, V_{DD} = 5.0 V	$I_{\overline{OUT\_EN}\_PU}$	-30	-50	-100	µA
$\overline{OUT\_EN}$ Leakage Current to V_{DD} $\overline{OUT\_EN}$ = 5.0 V, V_{DD} = 0 V	$I_{\overline{OUT\_EN}(LKG)}$	–	–	50	µA
SCLK Pull-down Current V_{SCLK} = V_{DD}	I_{SCLK}	5	15	25	µA
Tri-state SO Output 0 to 5.0 V	I_{TRISO}	-10	–	10	µA
$\overline{CS}$ Input Current $\overline{CS}$ = V_{DD}	$I_{\overline{CS}}$	-50	–	50	µA
$\overline{CS}$ Pull-up Current $\overline{CS}$ = 0 V	$I_{\overline{CS}\_PU}$	-30	-50	-100	µA
$\overline{CS}$ Leakage Current to V_{DD} $\overline{CS}$ = 5.0 V, V_{DD} = 0 V	$I_{\overline{CS}(LKG)}$	–	–	50	µA
SO Input Capacitance in Tri-state Mode	C_{SO}	–	20	–	pF
SO High State Output Voltage $I_{SO-HIGH}$ = -1.0 mA	V_{SO_HIGH}	V_{DD} - 0.4	–	–	V
SO Low State Output Voltage I_{SO-LOW} = 1.0 mA	V_{SO_LOW}	–	–	0.4	V
NOMI, MAXI in V10 Mode Pull-down Current NOMI, MAXI = 0.8 V, V_{DD} = 5.0 V	I_{PD}	30	70	100	µA
$\overline{SPKDUR}$ Output Voltage $I_{\overline{SPKDUR}}$ = 1.0 mA	$V_{\overline{SPKDUR}\_LO}$	–	–	0.4	V
Output Pull-up Current for $\overline{SPKDUR}$	$I_{\overline{SPKDUR}\_PV}$	30	50	100	µA
NOMI, MAXI High State Output Voltage $I_{NOMI-HIGH}$ = -1.0 mA $I_{MAXI-HIGH}$ = -1.0 mA	V_{I_HIGH}	V_{DD} - 0.4	–	–	V
NOMI, MAXI Low State Output Voltage $I_{NOMI-LOW}$ = 250 µA $I_{MAXI-LOW}$ = 250 µA	V_{I_LOW}	–	–	0.4	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Required Low State Duration on VPWR for Under-voltage Detect $V_{PWR} \leq 0.2$ V	t_{UV}	1.0	–	–	µs
Required Low State Duration on VDD for Power On Reset $V_{DD} \leq 0.2$ V	t_{RESET}	1.0	–	–	µs
INJECTOR DRIVERS					
Output ON Current Limit Fault Filter Timer (Short to Battery Fault)	t_{SC}	30	60	90	µs
Output ON Open Circuit Fault Filter Timer	$t_{(ON)OC}$	3.0	7.5	12	ms
Output Retry Timer	t_{REF}	–	10	15	ms
Output OFF Open Circuit Fault Filter Timer	$t_{(OFF)OC}$	100		400	µs
Output Slew Rate (No faster than 1.5 µs from off to on and on to off) R_{LOAD} = 14 Ω, V_{LOAD} = 14 V	$t_{SR(RISE)}$	1.0	5.0	10	V/µs
Output Slew Rate R_{LOAD} = 14 Ω, V_{LOAD} = 14 V	$t_{SR(FALL)}$	1.0	5.0	10	V/µs
Propagation Delay (Input Rising Edge OR $\overline{CS}$ to Output Falling Edge) Input @ 50%V_{DD} to Output voltage 90% of V_{LOAD}	t_{PHL}		1.0	5.0	µs
Propagation Delay (Input Falling Edge OR $\overline{CS}$ to Output Rising Edge) Input @ 50%V_{DD} to Output voltage 10% of V_{LOAD}	t_{PLH}		1.0	5.0	µs
IGNITION & GENERAL PURPOSE GATE DRIVER PARAMETERS					
Propagation Delay (GINx Input Rising Edge OR $\overline{CS}$ to Output Rising Edge) Input @ 50%V_{DD} to Output voltage 10% of $V_{GS(ON)}$	t_{PLH}		0.2	1.0	µs
Propagation Delay (Input Falling Edge OR $\overline{CS}$ to Output Falling Edge) Input @ 50%V_{DD} to Output voltage 90% of $V_{GS(ON)}$	t_{PHL}		0.2	1.0	µs
IGNITION PARAMETERS					
Open Secondary Fault Timer accuracy (uncalibrated)		-35	–	35	%
Maximum Dwell Timer Accuracy (uncalibrated)		-35	–	35	%
End of Spark Filter Accuracy (uncalibrated)(13)		-35	–	35	%

Notes

13. This parameter is guaranteed by design, however it is not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

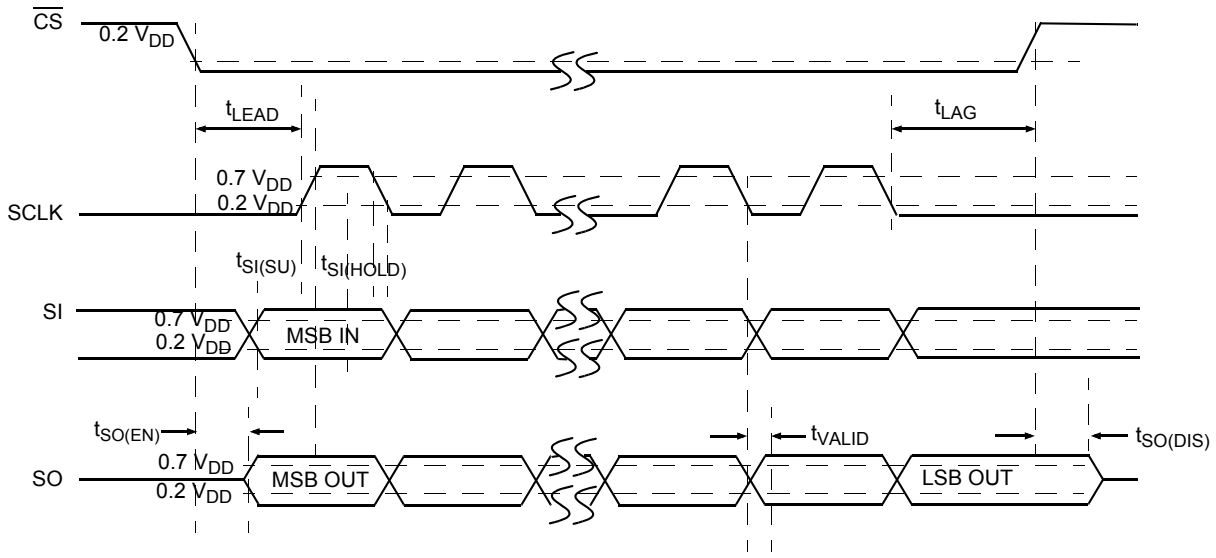
Characteristics noted under conditions of 3.0 V ≤ VDD ≤ 5.5 V, 6.0 V ≤ VPWR ≤ 32 V, -40°C ≤ TC ≤ 125°C, and calibrated timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with VPWR = 13 V, TA = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL PURPOSE GATE DRIVER PARAMETERS					
Short to Battery Fault Detection Filter Timer Accuracy VDD = High, Outputs Programmed ON Programmable from 30 µs to 960 µs in replicating increments Tolerance of timer after using calibration command Tolerance of timer before using calibration command	$V_{DS(flt-th)}$	 -10 -35		 +10 +35	%
Output OFF Open Circuit Fault Filter Timer VDD = 5.0 V, Outputs Off Tolerance of timer before using calibration command	$t_{(OFF)OC}$	 100		 400	µs
PWM Frequency 10 Hz to 1.28 kHz Tolerance after using calibration command	PWM_{FREQ}	-10%		10%	
PWM Frequency 10 Hz to 1.28 kHz Tolerance before using calibration command	PWM_{FREQ}	-35%		35%	
Gate Driver Short Fault Duty Cycle	GD_{SHRT_DC}		1.0	3.0	%
SPI DIGITAL INTERFACE TIMING(14)					
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK Required Setup Time	t_{LEAD}	 100	 –	 –	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ Required Setup Time	t_{LAG}	 50	 –	 –	ns
SI to Rising Edge of SCLK Required Setup Time	$t_{SI(SU)}$	 16	 –	 –	ns
Rising Edge of SCLK to SI Required Hold Time	$t_{SI(HOLD)}$	 20	 –	 –	ns
SI, $\overline{CS}$, SCLK Signal Rise Time(15)	$t_{R(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time(16)	$t_{F(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ Low-impedance(17)	$t_{SO(EN)}$	–	–	55	ns
Time from Rising Edge off $\overline{CS}$ to SO High-impedance(18)	$t_{SO(DIS)}$	–	–	55	ns
Time from Falling Edge of SCLK to SO Data Valid(19)	t_{VALID}	–	25	55	ns
Sequential Transfer Rate Time required between data transfers	t_{STR}	1.0	–	–	µs
DIGITAL INTERFACE					
Calibrated Timer Accuracy	t_{TIMER}	–	–	10	%
Un-calibrated Timer Accuracy	t_{TIMER}	–	–	35	%

Notes

14. These parameters are guaranteed by design. Production test equipment uses 1.0 MHz, 5.0 V SPI interface.
15. This parameter is guaranteed by design, however it is not production tested.
16. Rise and Fall time of incoming SI, $\overline{CS}$ and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
17. Time required for valid output status data to be available on SO pin.
18. Time required for output states data to be terminated at SO pin.
19. Time required to obtain valid data out from SO following the fall of SCLK with 200 pF load.

TIMING DIAGRAMS



FUNCTIONAL DESCRIPTION

FUNCTIONAL PIN DESCRIPTION

ANALOG SUPPLY VOLTAGE (VPWR)

The VPWR pin is the battery input to the 33810 IC. The VPWR pin requires external reverse battery and transient protection. All IC analog current and internal logic current is provided from the VPWR pin. With VDD applied to the IC, the application of VPWR will perform a POR.

DIGITAL LOGIC SUPPLY VOLTAGE (VDD)

The VDD input pin is used to determine communication logic levels between the microprocessor and the 33810 IC. Current from VDD is used to drive SO output and the pull-up current for $\overline{CS}$. V_{DD} must be applied for normal mode operation. Removing V_{DD} from the IC will place the device in sleep mode. With VPWR applied to the IC, the application of V_{DD} will perform a POR.

GROUND (GND)

The bottom pad or FLAG provides the only ground connection for the IC. The VPWR and VDD supplies are both referenced to the GND pad. The GND pad is used for both de-coupling the power supplies as well as power ground for the output drivers. Although the silicon die is epoxy attached to the top side of the pad, the pad must be grounded for proper electrical operation.

SERIAL CLOCK INPUT (SCLK)

The system clock (SCLK) pin clocks the internal shift register of the 33810. The SI data is latched into the input shift register on the rising edge of SCLK signal. The SO pin shifts status bits out on the falling edge of SCLK. The SO data is available for the MCU to read on the rising edge of SCLK. With $\overline{CS}$ in a logic high state, signals on the SCLK and SI pins will be ignored and the SO pin is tri-state

CHIP SELECT ($\overline{CS}$)

The system MCU selects the 33810 to receive communication using the chip select ($\overline{CS}$) pin. With the $\overline{CS}$ in a logic low state, command words may be sent to the 33810 via the serial input (SI) pin, and status information is received by the MCU via the serial output (SO) pin. The falling edge of $\overline{CS}$ enables the SO output and transfers status information into the SO buffer.

Rising edge of the $\overline{CS}$ initiates the following operation:

Disables the SO driver (high-impedance)

Activates the received command word, allowing the 33810 to activate/deactivate output drivers.

To avoid any spurious data, it is essential that the high-to-low and low-to-high transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic low state. Internal to the 33810 device is an active pull-up to VDD on $\overline{CS}$.

SERIAL INPUT DATA (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the rising edge of SCLK. A logic high state present on SI will program a *one* in the command word on the rising edge of the $\overline{CS}$ signal. To program a complete word, 16 bits of information or multiples of 8 there of must be entered into the device.

SERIAL OUTPUT DATA (SO)

The SO pin is the output from the shift register. The SO pin remains tri-stated until the $\overline{CS}$ pin transitions to a logic low state. All *normal operating drivers* are reported as *zero*, all *faulted drivers* are reported as *one*. The negative transition of $\overline{CS}$ enables the SO driver.

The SI/SO shifting of the data follows a first-in-first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

OUTPUT ENABLE ($\overline{OUTEN}$)

The $\overline{OUTEN}$ pin is an active low input. When the $\overline{OUTEN}$ pin is low, all the device outputs are active. The outputs are all disabled when $\overline{OUTEN}$ pin is high. SPI and parallel communications are still active in either state of $\overline{OUTEN}$.

FEEDBACK VOLTAGE SENSOR (FB0-FB3)

The FBx pin has multiple functions for control and diagnostics of the external MOSFET/IGBT Ignition gate driver.

In Ignition (IGBT) Gate Driver Mode, the feedback inputs monitor the IGBT's collector voltage to provide the spark duration timer control signal. The spark duration timer monitors this input to determine if the secondary clamp function should be activated. In secondary clamp mode, the IGBT's collector voltage is internally clamped to V_{PWR}+11V.

In the General Purpose Gate Driver mode, this input monitors the drain of an external MOSFET to provide short-circuit and open circuit detection by monitoring the MOSFET's drain to source voltage. The filter timer and threshold voltage are easily programmed through SPI (See tables 18 and 19 for SPI messages).

In General Purpose Gate Driver mode the FBx pin also provides a drain to gate clamp for fast turn off of inductive loads and external MOSFET protection.

GATE DRIVER OUTPUT (GD0-GD3)

The GD_X pins are the gate drive outputs for an external MOSFET or IGBT. Internal to the device is a Gate to Source resistor designed to hold the external device in the OFF state while the device is in the POR or SLEEP state.

LOW SIDE INJECTOR DRIVER OUTPUT (OUT0 - OUT3)

OUT0 - OUT3 are the Open drain low side (Injector) driver outputs. The drain voltage is actively clamped during turn off of inductive loads. These outputs can be connected in parallel for higher current loads provided the turn off energy rating is not exceeded.

RESISTOR SENSE POSITIVE (RSP)

Resistor Sense Positive - Positive input of a current sense amplifier. The ignition coil current is monitored by sensing the voltage across an external resistor connected between RSP and RSN. The output of the current sense amplifier feeds the inputs of the NOMI and MAXI comparators.

Note: RSN and RSP must be grounded in V10 mode.

RESISTOR SENSE NEGATIVE (RSN)

Resistor Sense Negative - Negative input of a current sense amplifier. The ignition coil current is monitored by sensing the voltage across an external resistor connected to RSP and RSN. The output of the current sense amplifier feeds the inputs of the NOMI and MAXI comparators.

Note: RSN and RSP must be grounded in V10 mode.

NOMINAL IGNITION COIL CURRENT (NOMI)

Nominal ignition coil current output flag. This output is asserted when the output current exceeds the level selected by the DAC.

NOMI can be configured as an input pin for V10 mode applications where the gate drive needs to be latched off by another device's MAXI current sense amplifier output. The NOMI input will latch off gate drivers 5 and 6 when configured as a V10 mode ignition gate driver See Figure 10.

SPARK DURATION OUTPUT (SPKDUR)

$\overline{\text{SPKDUR}}$ is the Spark Duration output. This open drain output is low while feedback inputs FB0 through FB3 are above the programmed spark detection threshold. This output indicates an ignition flyback event. Each feedback input (FB0 - FB3) is logically OR'd to drive the $\overline{\text{SPKDUR}}$ output. There is a 50μA pull up current source connected internally to the $\overline{\text{SPKDUR}}$ pin.

MAXIMUM IGNITION COIL CURRENT (MAXI)

Maximum ignition coil current output flag. This output is asserted when the output ignition coil current exceeds the selected level of the DAC. This signal also latches off the gate drive outputs when configured as an ignition gate driver. The MAXI current level is determined by the voltage drop across an external sense resistor connected to pins RSP and RSN.

MAXI can be configured as an input pin for V10 applications where the gate drive needs to be latched off by another devices MAXI current sense amplifier output. The MAXI input will latch off gate drivers 7 and 8 when configured as ignition gate drive outputs See Figure 10.

DRIVER INPUT (DIN0-DIN3), GATE DRIVER INPUT (GIN0-GIN3)

Parallel input pins for OUT0-OUT3 low side drivers and GD0-GD3 gate drivers. Each parallel input control pin is active high and has an internal pull-down current sink. The parallel input data is logically OR'd with the corresponding SPI input data register contents, except for the ignition mode IGBT drivers. They are only controlled by the parallel inputs GIN0-GIN3. In GPGD mode, GIN0-GIN3 are logically OR'd with SPI input data. All outputs are disabled when the $\overline{\text{OUTEN}}$ pin is HIGH, regardless of the state of the command inputs.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

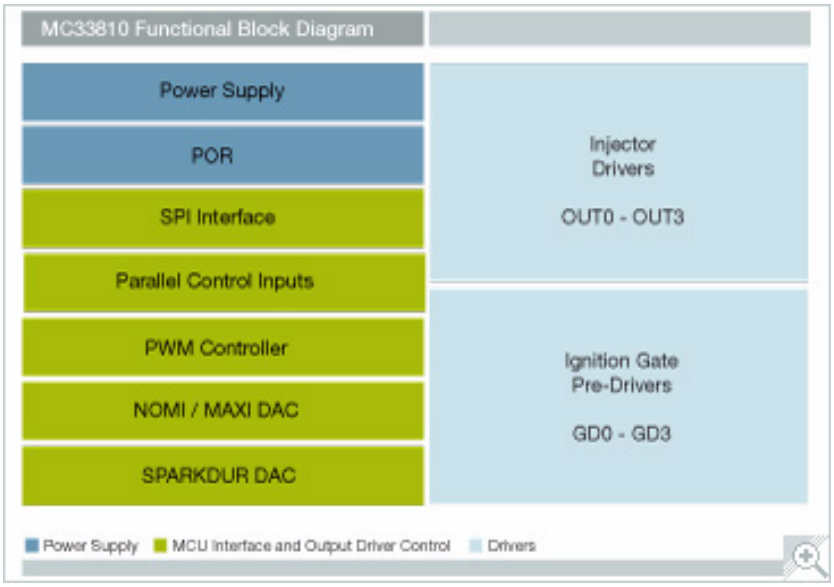


Figure 4. Functional Internal Block Diagram

POWER SUPPLY/POR

The 33810 is designed to operate from 4.5 to 36 V on the VPWR pin. The VPWR pin supplies power to all internal regulators, analog, and logic circuit blocks. The VDD supply is used for setting communication threshold levels and supplying power to the SO driver. This IC architecture provides a low quiescent current sleep mode. Applying VPWR and VDD to the device will generate a Power On Reset (POR) and place the device in the Normal State. The Power On Reset circuit incorporates a timer to prevent high frequency transients from causing a POR.

MCU INTERFACE AND OUTPUT CONTROL

This component provides parallel input pins for OUT0-OUT3 low side drivers and GD0-GD3 gate drivers. Each parallel input control pin is active high and has an internal pulldown current sink. The parallel input data is logically OR'd with the corresponding SPI input data register contents. All outputs are disabled when the OUTEN pin is HIGH, regardless of the state of the command inputs.

INJECTOR DRIVERS: OUT0 – OUT3

These pins are the Open drain low side (Injector) driver outputs. The drain voltage is actively clamped during turn off of inductive loads. These outputs can be connected in parallel for higher current loads, provided the turn off energy rating is not exceeded.

IGNITION GATE PRE-DRIVERS: GD0 – GD3

These pins are the gate drive outputs for an external MOSFET or IGBT. Internal to the device is a Gate to Source resistor designed to hold the external device in the OFF state while the device is in the POR or Sleep State.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

POWER SUPPLY

The 33810 is designed to operate from 4.5 to 36 V on the VPWR pin. The VPWR pin supplies power to all internal regulators, analog and logic circuit blocks. The VDD supply is used for setting communication threshold levels and supplying power to the SO driver. This IC architecture provides flexible microprocessor interfacing and low quiescent current sleep mode.

POWER-ON RESET (POR)

Applying V_{PWR} and V_{DD} to the device will generate a Power On Reset (POR) and place the device in the Normal State. The Power On Reset circuit incorporates a filter to prevent high frequency transients from causing a POR.

All outputs are disabled when the $\overline{\text{OUTEN}}$ input pin is HIGH regardless of the SPI control registers or the logic level on the parallel input pins. With the $\overline{\text{OUTEN}}$ pin high, SPI messages may be sent and received by the device. Upon enabling the device ($\overline{\text{OUTEN}}$ low), outputs will be activated based on the state of the command register or parallel input.

Table 5. Operational States

VPWR	VDD	$\overline{\text{OUTEN}}$	OUTPUTS	STATE
L	L	X	OFF	Power Off
L	H	X	OFF	POR
H	L	X	OFF	SLEEP
H		X	OFF	POR
	H	X	OFF	POR
	L	X	OFF	SLEEP
H	H	L	ACTIVE	NORMAL
H	H	H	OFF	NORMAL

SLEEP STATE

Sleep State is entered when the V_{DD} supply voltage is removed from the VDD pin. In Sleep State all outputs are off. Applying V_{DD} will force the device to exit the Sleep State and generates a POR.

NORMAL STATE

The default Normal State is entered when power is applied to the VPWR and VDD pins.

Control register settings from a Power-ON Reset (POR) are as follows:

- All outputs off
- IGNITION gate driver mode enabled (IGBT Ignition Mode).
- PWM frequency and duty cycle control disabled.
- Off State open load detection enabled (LSD)
- MAXI dac set to 14 A, NOMI DAC set to 5.5A
- Spark detect level VIL DAC set to V_{PWR} +5.5V
- Open secondary timer set to 100 μs
- Dwell timer set 32ms
- Soft shutdown disabled
- Low-voltage flyback clamp disabled
- Dwell overlap MAXI offset disabled

MODES OF OPERATION

In Normal State, the 33810 gate driver has three modes of operation, ignition Mode, GPGD (General Purpose Gate Driver) Mode and V10 mode.The operating mode of each gate driver may be set individually and is programmed using the Mode Select Command.

MODE SELECT COMMAND

The *MODE Select Command* is used to set the operating mode for the GDx gate driver outputs, over/under-voltage operation and to enable V10 Mode and the PWM generators. The Mode Select Command programmable features are listed below.

- Ignition/GPGD Mode select (gate drivers)
- V10 Mode enable
- Over/Under-voltage operation for all drivers
- GPGD PWM controller enable

IGNITION/GPGD MODE SELECT

The Ignition/General Purpose Gate Driver Mode select bits determine independently, the operating mode of each of the GDx gate driver outputs. Bits 8,9,10,11 correspond to GD0, GD1, GD2, GD3 respectively. Setting the bit to a logic 0 sets the GDx driver to the Ignition Mode. Setting the bit to a logic 1 commands the GDX driver to the General Purpose Mode and disables the ignition features for that particular gate driver (except the MAXI current shutdown feature). Further information on GDx gate driver in Ignition Mode and General Purpose Mode is provided later in this section of the data sheet.

V10 MODE ENABLE BIT

The V10 Enable bit allows the user to configure the device for 10 cylinder applications. When the V10 Mode is enabled, the device configures the NOMI pin and MAXI pin as digital inputs rather than outputs. The new MAXI input pin receives

the MAXI shutdown signal for GD0 and GD2 and the new NOMI input pin receives the MAXI shutdown signal for GD1 and GD3. Further information on V10 Mode is provided in the V10 Application section.

Note: RSN and RSP must be grounded in V10 Mode.

OVER/UNDER-VOLTAGE SHUTDOWN/RETRY BIT

The Over/Under-voltage Shutdown/Retry bit allows the user to select the global over and under-voltage fault strategy for all the outputs. In an over-voltage or under-voltage condition on the VPWR pin, all outputs are commanded off. The Over/Under-voltage control bit sets the operation of the outputs when returning from over/under- voltage. Setting the Over/Under-voltage bit to logic [1] will force all outputs to remain OFF when V_{PWR} returns to normal level. To turn the output on again, the corresponding input pin or SPI bit must be reactivated. Setting the Over/Under-voltage bit to logic [0] will command all outputs to resume their previous state when VPWR returns to normal level. Table 6 below provides the output state when returning from over or under-voltage.

Table 6. Over-voltage/Under-voltage Truth Table

GINx DINx Input Pin	SPI Bit	Over/ Under-voltage Control Bit	$\overline{\text{OUTEN}}$ Input pin	State When Returning From Over/Under-voltage
X	X	X	1	OFF
X	X	1	0	OFF
0	0	0*	0	OFF
X	1	0*	0	ON
1	X	0*	0	ON

* Default Setting

Note: The SPI bit does not control the Gate Driver outputs in the Ignition Mode, only in the GPGD Mode.

An under-voltage condition on VDD results in the global shutdown of all outputs and reset of all internal control registers. The V_{DD} under-voltage threshold is between 0.8V and 2.8V

PWM_X ENABLE BIT

Gate Driver outputs programmed as General Purpose Gate Drivers may be used as low frequency PWM outputs. The PWM generators are enabled via bits 0 through 3 in the Mode Select Command. Bits 0 through 3 correspond to outputs GD0 through GD3 respectively. Once the frequency and duty cycle are programmed through the PWM Frequency & DC command, the PWM output may be turned ON and OFF through the PWM enable bit. Further information on PWM control is provided in the General Purpose Gate Driver Mode section of this data sheet.

IGNITION (IGBT) GATE DRIVER MODE

The MC33810 contains dedicated circuitry necessary for automotive ignition control systems. Each gate driver may be individually configured as an Ignition Gate Driver with the following features:

- Spark duration signal
- Open secondary timer
- Soft shutdown control
- Low-voltage flyback clamp
- Ignition ignition coil current measurement
- MAXI output and control
- NOMI output
- Maximum dwell timer

In the Ignition Mode, several control strategies are in place to control the IGBT for enhanced system performance. Information acquired from the FBx pin allows the device to produce a spark duration signal output ($\overline{\text{SPKDUR}}$) and detect open secondary ignition coils. Based on the FBx signal and Spark Command register settings, the device performs the appropriate gate control (Low-voltage Flyback Clamp, Soft Shutdown) and produces the $\overline{\text{SPKDUR}}$ output.

The FBx pin is connected to the collector of the IGBT through an external 9:1 resistor divider network. The recommended values for the resistor divider network is 36K and 4.02K, with the 36K resistor connected from the IGBT collector to the FBx pin and the 4.02K resistor connected from the FBx pin to ground.

Additional controls to the gate driver are achieved by sensing the current through the external IGBT. The Resistor Sense Positive (RSP) and Resistor Sense Negative (RSN) inputs are use to measure the voltage across an external 20 mΩ or 40 mΩ current sense resistor. A gain select bit in the Spark Command SPI Command messages should be set to 1 (gain of 2) when using a 20 mΩ current sense resistor. When using a 40 mΩ current sense resistor, the gain select bit should be set to 0 (gain of 1 is the default value).

The ignition coil current is compared with the output of the DACs which have been programmed via the SPI Commands. The comparison generates the Nominal Current signal (NOMI) and the Maximum Current signal (MAXI). Both signals have a low output when the ignition coil current is below the programmed DAC value and a high output when the current is above the programmed DAC value.

When the GDx output is shutdown because of the control strategy, the output may be activated again by toggling the input control.

SPARK COMMAND

The Spark Command is an ignition mode command used to program the parameters for the ignition mode features listed below:

- End spark threshold (EndSparkTh bits)
- Open secondary fault timer (OSFLT bits)

- Secondary clamp (secondary clamp bit)
- Soft shutdown enable (SoftShutDn bit)
- Ignition ignition coil current amplifier gain (Gain Sel bit)
- Overlapping dwell disable (Overlap Dwell Disable bit)
- Maximum dwell enable (MaxDwellEn bit)
- Maximum dwell timer (MaxDwellTimer bits)
- End of spark filter timer value

Spark Command address and data bits are listed in Table 20

NOTE: Gate driver outputs programmed to be General Purpose Gate Drivers are not affected by the Spark Commands.

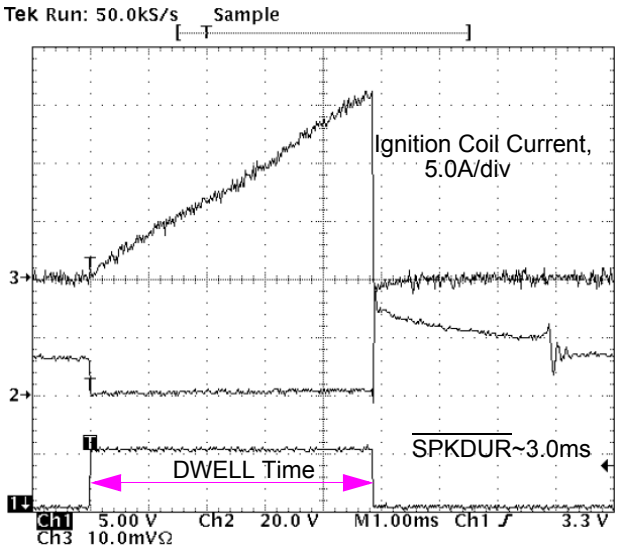
SPARK DURATION SIGNAL

The Spark Duration is defined as the beginning of current flow to the end of current flow across the spark plug gap. Because the extremely high-voltage ignition coil secondary output is difficult to monitor, corresponding lower voltage signals generated on the ignition coil primary are often used. The FBx pins monitor the ignition coil primary voltage (IGBT Collector) through a 10 to 1 voltage divider. When the IGBT is disabled, the rise in the FBx signal indicates a sparkout condition is occurring at the spark plug gap.

The device considers the initial thresholds for spark duration to be $V_{IH} = V_{PWR} + 21$ V for rising edge as measured on the collector of the IGBT. The spark duration falling edge reference is programmable via SPI through the **End Spark Threshold** bits 0 and 1 (See Table 7).

Figure 5 illustrates a typical ignition event with dwell time and spark duration indicated.

Figure 5. Ignition Coil Charge and Spark Event



Channel 1: GINx IGBT Gate Drive
Channel 2: IGBT Collector Voltage
Channel 3: IGBT Current @ 5.0A/Div

V_{PWR} = 16.0V
Default settings
Begin spark threshold $V_{IH} = V_{PWR} + 21V$
End spark threshold $V_{IL} = V_{PWR} + 5.5V$

The pulse width of the $\overline{\text{SPKDUR}}$ signal is measured by the MCU timer/input capture port to determine the actual spark duration. Spark duration information is then used by the MCU spark control algorithm to optimize the dwell time.

Table 7. End Spark Threshold

Spark Command Bit<b1,b0>	End Spark Threshold (VIL)
00	VPWR + 2.75
01	VPWR + 5.5
10	VPWR + 8.2
11	VPWR + 11.0

OPEN SECONDARY TIMER

A fault due to open in the ignition coil secondary circuit can be determined by waveforms established on the ignition coil primary during a spark event. The spark event is initiated by the turn off of the IGBT. The voltage on the collector of the IGBT rises up to the IGBT's internal collector to gate clamp voltage (typically 400 volts). Collector to gate clamp events normally last 5.0 to 50µs. In an open ignition coil secondary fault condition, the collector to gate clamp event lasts much longer. The oscilloscope waveform in Figure 6 and Figure 7 compare a normal spark signature with that of an open secondary fault condition signature.

Figure 6. Normal Spark Event

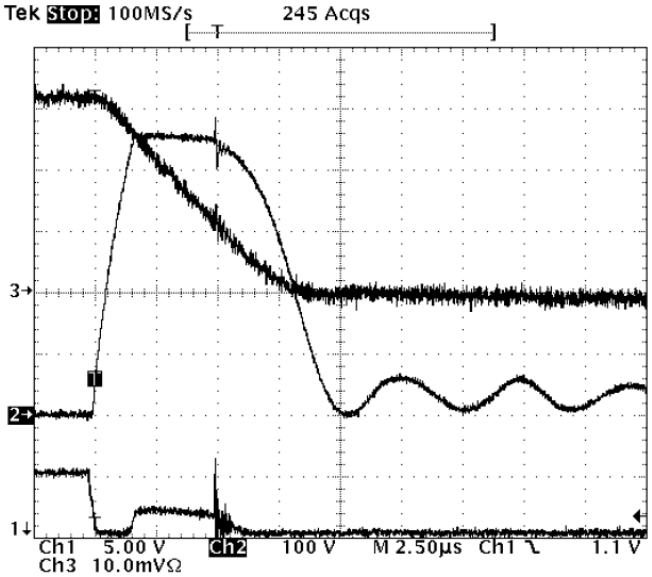
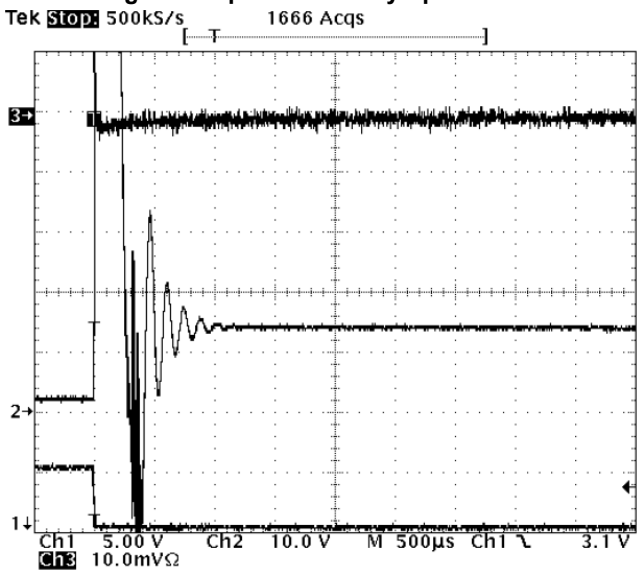


Figure 7. Open Secondary Spark Event



The Open Secondary timer is initiated on the rising edge of the ignition coil primary spark signal and terminated on the falling edge. The rising edge Open Secondary Threshold is V_{IH}= 135 V at primary, no hysteresis. The falling edge Open Secondary threshold is V_{IL} = 135V.

Collector to gate clamp durations that last longer than the selected Open Secondary Fault Time interval (Table 8) indicates a failed spark event. When the Open Secondary Fault Time is exceeded and the Low-voltage Clamp is enabled, the GDx output will activate the Low-voltage Clamp shown in figure 16. The Logic for this Low-voltage Clamp is defined in Figure 9

Table 8. Open Secondary Timer

Spark Command Bits<b3,b2>	Open Secondary Fault Timer OSFLT (µs)
00	10
01	20
10	50
11	100

LOW-VOLTAGE CLAMP

The Low-voltage Clamp is an internal clamp circuit which biases the IGBT's gate voltage in order to control the collector to emitter voltage to VPWR+11V. This technique is used to dissipate the energy stored in the ignition coil over a longer period of time than if the internal IGBT clamp were used.

In the open secondary fault condition, all of the stored energy in the ignition coil is dissipated by the IGBT. This fault condition requires the use of a higher energy rated IGBT than would otherwise be needed.

The Low-voltage Clamp spreads out the energy dissipation over a longer period of time, thus allowing the use of a lower energy rated IGBTs. The internal low-voltage clamp is connected between the IGBT's collector (through an external resistor) and the IGBT's gate. The energy stored in the ignition coil is dissipated by the IGBT, not the internal clamp. The internal clamp only provides the bias to the IGBT.

Several logical signals are required as inputs to activate the GDx Low-voltage Clamp feature. The GDx Low-voltage Clamp feature may be disabled through bit 4 of the Spark Command message.

Figure 8. Low-voltage Clamp

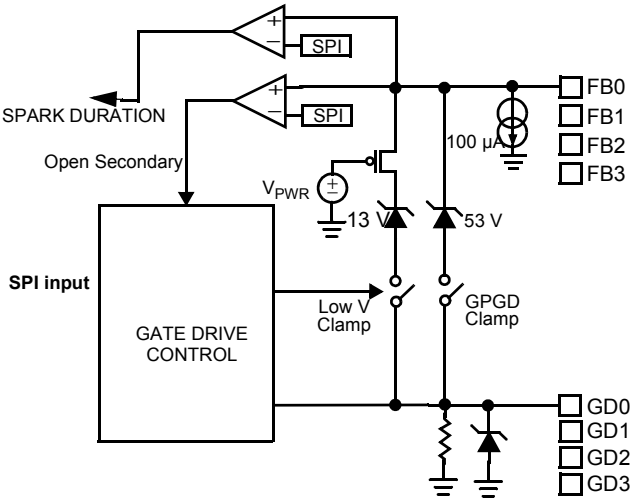
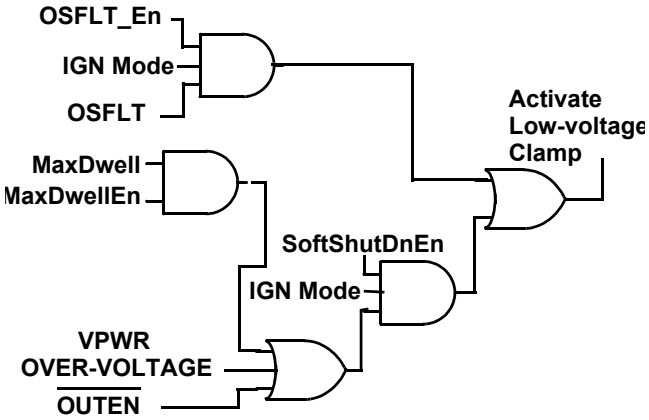


Figure 9. Low-voltage Clamp Logic



SOFT SHUTDOWN ENABLE

The soft shutdown feature is enabled via the SPI by asserting control bit 5 in the Spark Command message.

When enabled, the following events initiate a soft shutdown control of the gate driver.

- $\overline{\text{OUTEN}}$ = High (Outputs Disabled)
- Over-voltage on VPWR pin

- Max dwell time

Soft Shutdown is designed to prevent an ignition spark while turning off the external IGBT. The Low-voltage Clamp is activated to provide the mechanism for a soft shutdown.

GAIN SELECT BIT

The ignition coil current comparators are used to compare the programmed NOMI and MAXI DAC value with voltage across the external current sense resistor. When selecting a gain of two, the ignition coil current sense resistor must be reduced from 40mΩ to 20mΩ.

OVERLAPPING DWELL ENABLE BIT

Overlapping dwell occurs when two or more ignition mode drivers are commanded ON at the same time. In this condition, with the Overlapping Dwell Bit enabled the MAXI DAC threshold value is increased as a percentage of the nominal programmed value. The percent increase is determined by bit 5 through bit 7 of the DAC Command.

Table 9. Overlapping Dwell Compensation

DAC Command Bits<b7,b6,b5>	Overlap Compensation (%)
000	0%
001	7%
010	15%
011	24%
100	35% (default)
101	47%
110	63%
111	80%

MAXIMUM DWELL ENABLE BIT

Bit 8, the Maximum Dwell Enable bit allows the user to enable the Maximum Dwell Gate Turnoff Feature. When the Max Dwell bit is programmed as logic 0 (disabled) the device will not perform a Low-voltage Clamp due to Max Dwell (See Figure 9).

MAXIMUM DWELL GATE TURN OFF FEATURE

In automotive ignition systems, dwell time is defined as the duration of time that an ignition coil is allowed to charge. The MC33810 starts the measure of time from the gate drive ON command. If the dwell time is greater than the Max Dwell Timer setting (Table 10), the offending ignition gate driver is commanded OFF. The Max Dwell Gate Turn Off Feature may be disabled via bit 8 of the Spark Command. When the feature is disabled, the Max Dwell fault bits are always logic 0. The Max Dwell Timer feature pertains to Ignition Mode only and does not affect gate drivers configured as general purpose gate drivers.

The Max Dwell gate turn off signal is a logically ANDed with the Soft Shutdown bit to activate a Low-voltage Active Clamp (See Figure 9).

Table 10. Maximum Dwell Timer

Spark Command Bit<b11,b10,b9>	MAX Dwell Timer MaxDwell (ms)
000	2
001	4
010	8
011	16
100	32 (default)
101	64
110	64
111	64

DAC COMMAND (DIGITAL TO ANALOG CONVERSION COMMAND)

The DAC Command is an ignition mode command that sets the nominal ignition coil current (NOMI) and maximum ignition coil current (MAXI) DAC values. Bits 0 through 4 set the NOMI threshold value and, bits 8 through 11 set the MAXI threshold values. The DAC command and default values are listed in the SPI Command Summary Table 20. The NOMI output is used by the MCU as a variable in dwell and spark control algorithms.

NOMI DAC BITS

The NOMI output signal is generated by comparing the external current sense resistor differential voltage (Resistor Sense Positive, Resistor Sense Negative) with the SPI programmed NOMI DAC value. When the NOMI event occurs, the NOMI output pin is asserted (High). The NOMI output is only a flag to the MCU and it's output does not affect the gate driver.

When using a 20 mΩ resistor as the current sense resistor, the gain select of the differential amplifier connected to RSP and RSN, should be set to a gain of 2, via the SPI Command Message Spark Command (Command 0100, hex 4), Control bit 6 =1.

When using a 40mΩ resistor as the current sense resistor, the gain select of the differential amplifier connected to RSP and RSN, should be set to a gain of 1, via the SPI Command Message Spark Command (Command 0100, hex 4), Control bit 6 =0. This is also the default value.

The NOMI output provides a means to alert the MCU when the ignition coil primary current equals the value programmed into the NOMI DAC.

In V10 Mode, the NOMI pin is reconfigured as a MAXI input pin from a third MC33810 device in the system. In this mode a NOMI input has effectively the same control as an internal MAXI signal. Further information is provided in the V10 Mode application section of this data sheet.

Table 11. Nominal Current DAC Select

DAC Command Bits<4,3,2,1,0>	NOMI Current (A)	Differential Voltage (mV Rs = 20 mΩ (Gain = 2)	Differential Voltage (mV Rs = 40 mΩ (Gain = 1)
00000	3.00	60	120
00001	3.25	65	130
00010	3.50	70	140
00011	3.75	75	150
00100	4.00	80	160
00101	4.25	85	170
00110	4.50	90	180
00111	4.75	95	190
01000	5.00	100	200
01001	5.25	105	210
01010	5.50	110	220
01011	5.75	115	230
01100	6.00	120	240
01101	6.25	125	250
01110	6.50	130	260
01111	6.75	135	270
10000	7.00	140	280
10001	7.25	145	290
10010	7.50	150	300
10011	7.75	155	310

Table 11. Nominal Current DAC Select

DAC Command Bits<4,3,2,1,0>	NOMI Current (A)	Differential Voltage (mV Rs = 20 mΩ (Gain = 2)	Differential Voltage (mV Rs = 40 mΩ (Gain = 1)
	8.00	160	320
10101	8.25	165	330
10110	8.50	170	340
10111	8.75	175	350
11000	9.00	180	360
11001	9.25	185	370
11010	9.50	190	380
11011	9.75	195	390
11100	10.00	200	400
11101	10.25	205	410
11110	10.50	210	420
11111	10.75	215	430

MAXI DAC BITS

The MAXI control block provides a means to shut off all the ignition coil drivers if the current reaches a SPI programmable maximum level. Control is achieved by comparing the output of the current sense amplifier with a SPI programmed DAC value.

The MAXI comparator disables all gate drivers configured as ignition drivers when the DAC MAXI setting is exceeded. When a MAXI event occurs, the MAXI bit in the fault status register is set and the MAXI pin is asserted (High).

When using a 20mΩ resistor as the current sense resistor, the gain select of the differential amplifier connected to RSP and RSN, should be set to a gain of 2, via the SPI Command Message Spark Command (Command 0100, hex 4), Control bit 6 =1.

When using a 40mΩ resistor as the current sense resistor, the gain select of the differential amplifier connected to RSP and RSN, should be set to a gain of 1, via the SPI Command Message Spark Command (Command 0100, hex 4), Control bit 6 =0. This is also the default value.

The MAXI fault bit in the SPI fault status register is cleared when the MAXI condition no longer exists and the SPI fault status register has been read by the MCU.

In V10 Mode, the MAXI pin is configured as an input to receive the MAXI signal from a second MC33810 device in the system. In this mode a input MAXI signal has effectively the same control as an internal MAXI signal. Further information is provided in the V10 Mode application section of this specification.

Table 12. Maximum Current DAC Select

DAC Command Bit<b11,b10,b9,b8>	MAXI Current (A)	Differential Voltage (mV Rs = 20 mΩ	Differential Voltage (mV Rs = 40 mΩ
0000	6.0	120	240
0001	7.0	140	280
0010	8.0	160	320
0011	9.0	180	360
0100	10.0	200	400
0101	11.0	220	440
0110	12.0	240	480
0111	13.0	260	520
1000	14.0	280	560
1001	15.0	300	600
1010	16.0	320	640
1011	17.0	340	680
1100	18.0	360	720
1101	19.0	380	760
1110	20.0	400	800
1111	21.0	420	840

END OF SPARK FILTER BITS

The ringing at the end of the Spark signatures waveform can cause erroneous detection of the End of Spark event. To eliminate the effect of this ringing, a low pass filter with variable time values can be selected. Four time values for the low pass filter have been provided with a zero value indicating that no low pass filtering is to be used. The End of Spark Filter bits specify a 0, 4µs, 16µs, or 32µs time interval to sample the spark ignition coil primary current to ignore the ringing at the end of spark.

Table 13. End of Spark Filter Time Select

End of Spark Filter Bits<1, 0>	Filter Time µs
00	0.0
01	4.0
10	16.0
11	32.0

GENERAL PURPOSE GATE DRIVER MODE

Each gate driver can be individually configured as a General Purpose Gate Driver (GPGD) and controlled from the parallel GINx input pins, SPI Driver ON/OFF Command or may be programmed through the SPI for a specific frequency and duty cycle output (PWM).

In General Purpose Gate Driver mode the gate drivers have the following features:

- Gate driver for discrete external MOSFET
- Off state open load detect
- On state short circuit protection
- Programmable drain threshold and duration timer for short fault detection
- PWM frequency/duty cycle controller

In GPGD Mode the GDx output is a current controlled output driver with slew rate control, gate to source clamp, passive pull-down resistor and a drain to gate clamp for switching inductive loads.

Driver ON/OFF Command

The Driver ON/OFF Command, bits 4 through 7 control gate drivers that have been Mode Select Command programmed as GPGD. A logic 1 in bits 4 through 7 will command the specific output ON. A logic 0 in the appropriate bit location commands the specific output Off. Also contained in the Driver ON/OFF Command are SPI control bits for the integrated LSD output drivers. Further information on LSD control is provided in the Low Side Injector Driver section of the data sheet.

NOTE: Gate drivers programmed to IGNITION mode have parallel input control only, and cannot be turned off and on via SPI commands.

GPGD Short Threshold Voltage Command

Each GPGD driver is capable of detecting an open load in the off state and shorted load in the on state. All faults are reported through the SPI communication. For open load detection, a current source is placed between the FBx pin and ground of the IC. An open load fault is reported when the FBx voltage is less than the 2.5 V threshold. Open load fault detect threshold is set internally to 2.5 V and may not be programmed. A shorted load fault is reported when the FBx pin voltage is greater than the programmed short threshold voltage.

The short to battery fault threshold voltage of the external MOSFET is programmed via the GPGD Short Threshold Voltage Command. Table 14 illustrates the bit pattern to select a particular threshold. Drain voltages less than the selected threshold are considered normal operation. Drain voltages greater than the selected threshold voltage are considered faulted.

Table 14. FBx Fault Threshold Select

GPGD V_{DS} FLT Bits	FBx Fault Threshold Select
000	0.5V
001	1.0V
010	1.5V
011	2.0 (default)
100	2.5V
101	3.0V
110	No Change
111	No Change

GPGD SHORT TIMER COMMAND

The GPGD Short Timer Command allows the user to select the duration of time that the drain voltage is allowed to be greater than the programed threshold voltage without causing shutdown. External MOSFETS with drain voltages greater than the programed threshold for longer than the Fault Duration Timer are shutdown. Timer durations are listed in Table 15.

Table 15. FBx Short Fault Timer

GPGD FLT Timer Bits	Fault Timer Select
000	30µs
001	60µs
010	120µs
011	240µs (default)
100	480µs
101	960µs
110	No Change
111	No Change

Notes: Tolerance on this fault timer setting is ±10% after using the Calibration Command.

GPGD FAULT OPERATION COMMAND

The GPGD Fault Operation Command sets the operating parameters for the gate drivers under faulted conditions. A short fault is said to be “detected” when the drain source voltage, Vds, of the external MOSFET, exceeds the SPI programmed short threshold voltage. The short fault is said to be “declared” when the V_{DS} over-voltage lasts longer than the SPI programmed “fault timer.” (short duration time > fault timer programmed value)

Each gate driver is individually set to either, restore to the pre-fault state, or shutdown when a short fault is declared. By setting the Retry/Shutdown bit in the GPGD Fault Operation Command to logic 1 the specific output will try to go back to the pre-fault state when the fault is no longer declared, after a programmed “inhibit time”.

The retry strategy will cause the output to try to return to the pre-fault state on a 1% duty cycle basis. For example: If the fault timer is set to 120µs and a fault is declared (drain voltage greater than the programmed threshold for greater than 120µs), the GDx output driver will be forced off for 12ms. After 12ms has elapsed, if the inputs, GINx or SPI, have not tried to shut off the particular GDx output in the interim, the GDx output will try to set the external driver on again (the pre-fault state). A continued declared fault on the output would result in another 12ms shutdown period.

By setting the Retry/Shutdown bit in the GPGD Fault Operation Command to logic 0 the specific output will shutdown and remain off when the short fault is declared. Only a reissue of the turn on command, via SPI or GINx, will force the output to try and turn on again.

In the event that a GPGD is selected as a PWM controller and a short occurs on the output, the output retry strategy forces the output to a 1% duty cycle based on the fault timer setting. For example: If the fault timer is set to 120µs and a fault is detected (drain voltage greater than programmed threshold), the PWM output will be commanded off for 12ms and commanded ON again at the next PWM cycle.

Care should be taken to select a fault timer that is shorter than the minimum duty cycle ON time of the PWM controller. Selecting a fault timer that is longer will allow the PWM controller to continue to drive the external MOSFET into a shorted load.

PWM FREQUENCY/DUTY CYCLE COMMAND

The PWMx Freq & Duty Cycle command is use to program the GDx outputs with a frequency and duty cycle. Table 16 defines the user selectable output frequency. The frequency and duty cycle may be updated at any time using the PWM Freq&DC command, however the update will only begin on the next PWM rising edge time.

Once the PWM Freq & DC registers are programmed and the PWM controller is enabled through the Mode Command the PWM outputs are turned ON and OFF via the GINx pin OR the SPI GPGD ON/OFF Command control bit. All Parallel and serial On and Off command updates to the PWM controller are synchronous with the rising edge of the previous PWM period.

The truth table for GDx control in general purpose mode is provided in Table 8.

The duty cycle of the PWM outputs is controlled by bits 0-6, inclusive. The duty cycle value is 1% per binary count from 1-100 with counts of 101-127 defaulting to 100%. For example, sending SPI command 101001000001100 would set GD1, PWM output to 10Hz and 12% duty cycle.

.

Table 16. Frequency Select

PWM Freq&DC Command Bit<b9,b8,b7>	Frequency Hz
000	10 Hz (default)
001	20 Hz
010	40 Hz
011	80 Hz
100	160 Hz
101	320 Hz
110	640 Hz
111	1.28 kHz

Notes: Tolerance on selected frequency is ±10% after using the Calibration Command. Shorts to battery and open load faults will not be detected for frequency and duty cycle combinations inconsistent with fault timers.

Table 17. Pre-driver GDx Output Control

Mode Command IGN/GP Bit	Driver On/OFF GPGD Bit	PWMx Enable Bit	GINx terminal	GDx Output
1	0	X	0	OFF
1	0	0	1	ON
1	1	0	X	ON
1	X	1	1	Freq/DC
1	1	1	X	Freq/DC

V10 MODE

V10 Mode provides a method for monitoring 10 ignition events while using only two current sense resistors. This is achieved using three MC33810 devices. Two MC33810 devices are programmed as Normal Ignition mode outputs and one is programmed as a V10 ignition mode output. The ignition gate driver outputs are partitioned into two banks of five outputs each (See Figure 10). Each bank contains one or two driver(s) from the V10 device.

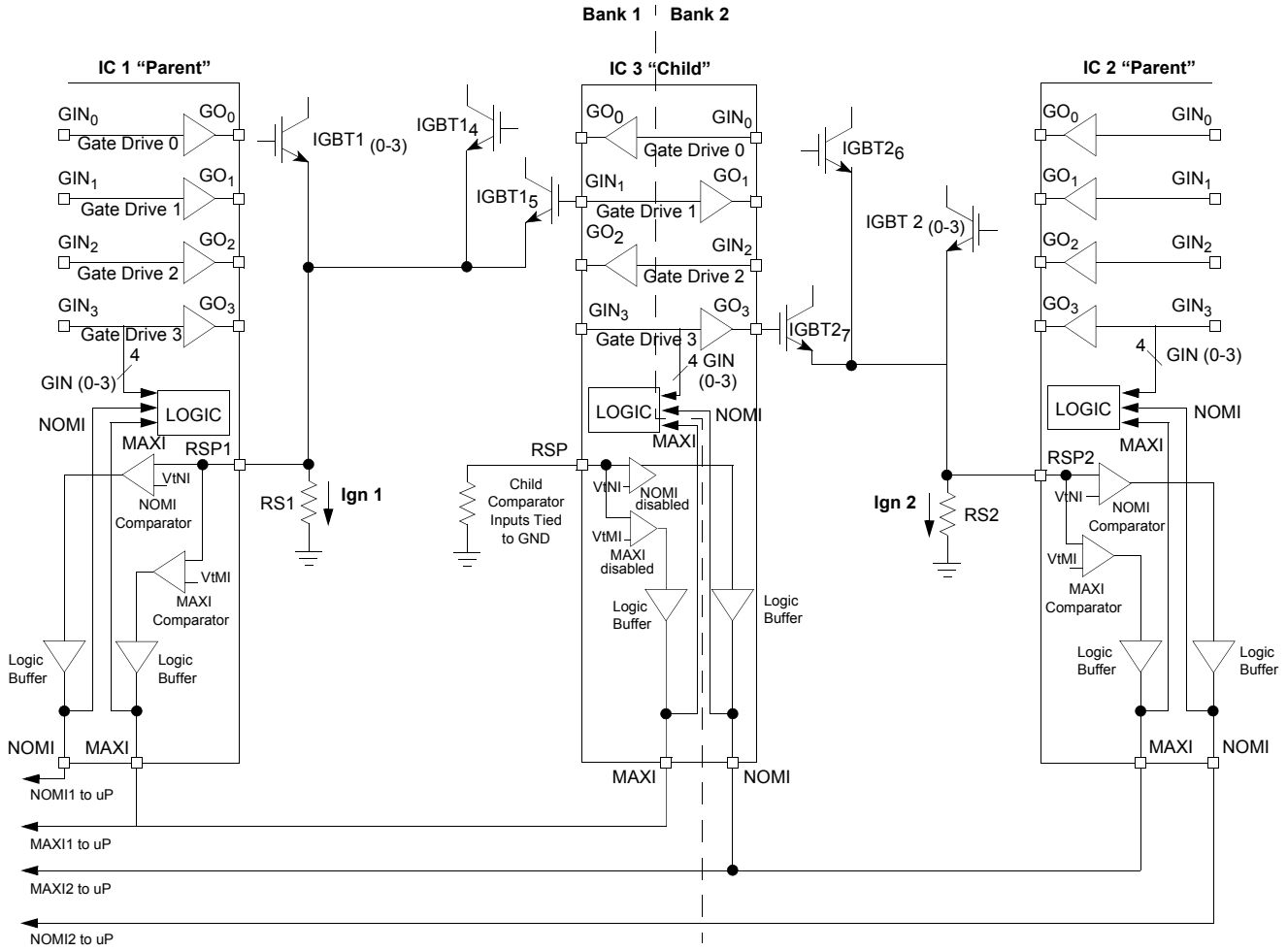
Drivers in the V10 device are grouped in two's (GD0&GD2, GD1&GD3). Current from each V10 mode IGBT group is monitored by the appropriate Normal Mode device (See Figure 10). The MAXI signal from one Normal Mode device is ported to the V10 Mode MAXI input pin. Likewise the MAXI signal from the second Normal Mode device is ported to the V10 Mode NOMI input pin. The V10 Mode NOMI/MAXI inputs are used as MAXI shutdown signals for the appropriate ignition gate drive group.

V10 Mode contains the same features as Ignition Mode gate drivers with the following exceptions:

- NOMI/MAXI configured as input pins
- MAXI shutdown for GPGD disabled
- NOMI/MAXI comparators disabled

In V10 Mode, Spark Command bits 7 and 8 (Gain Select, Overlapping Dwell) are disabled. These two features are achieved through the Normal Mode devices.

RSN and RSP must be grounded in V10 Mode.



Note: For "child" input NOMI is for channel 1&3, input MAXI is for channel 0&2

Figure 10. V10 Mode

LOW SIDE INJECTOR DRIVER

The four open drain low side injector drivers are designed to control various automotive loads such as injectors, solenoids, lamps, relays and unipolar stepper motors. Each driver includes off and on state open load detection, short circuit protection and diagnostics. The injector drivers are individually controlled through the ON/OFF SPI input command Table 20 or parallel input pins DIN0 to DIN3. Serial and parallel control of the output state is determined by the logical OR of the SPI serial bit and the DINx parallel input pins. All four outputs are disabled when the $\overline{\text{OUTEN}}$ input pin is high regardless of the state of the SPI control bit or the state of the DINx pin. All four injector drivers are not affected by the selection of the gate driver's three modes of operation (Ignition Mode, General Purpose Mode, V10 mode).

ON/OFF CONTROL COMMAND

To program the individual output of the 33810 ON or OFF, a 16-bit serial stream of data is entered into the SI pin. The first 4 bits of the control word are used to identify the On/Off Command. Bit 0 through bit 3 of the ON/OFF Control Command turn ON or OFF the specific output driver.

INJECTOR DRIVER FAULT COMMANDS

Fault protection strategies for the injector drivers are programmed by the SPI LSD Fault Command. Bit 8 through 11 determine the type of short circuit protection to be used, bits 0 through 7 set the open load strategy.

Short-circuit protection consists of three strategies. All strategies utilize current limiting as an active element to protect the output driver from failure.The T_{LIM} and Timer options are used to enhance the short circuit protection strategy of the Injector drivers. The timer protection scheme uses a low duty cycle in the event of a short-circuit. The T_{LIM}

protection circuit uses the junction temperature of the output driver to determine the fault. Both methods may be used together or individually.

TIMER PROTECTION

The first protection scheme uses a low ON to OFF duty cycle to protect the output driver. The low duty cycle allows the device to cool so that the maximum junction temperatures are not exceeded. During a short condition, the device enters current limit. The driver will shutdown for short conditions lasting longer than the current limit timer (~60μs)

TEMPERATURE LIMIT (T_{LIM})

The second scheme senses the temperature of the individual output driver. During a short event the device enters current limit and will remain in current limit until the output driver temperature limit is exceeded (T_{LIM}). At this point, the device will shutdown until the junction temperature falls below the hysteresis temperature value. The T_{LIM} hysteresis value is listed in the previous specification tables.

The third method combines both protection schemes into one. During a short event the device will enter current limit. The output driver will shutdown for short conditions lasting longer than the current limit timer. In the event that the output driver temperature is higher than maximum specified temperature the output will shutdown.

The Shutdown/Retry bit allows the user to determine how the drivers will respond to each short circuit strategy. Table 18 provides fault operation for all three strategies.

Outputs may be used in parallel to drive higher current loads provided the turn-off energy of the load does not exceed the energy rating of a single output driver (100mJ maximum).

Table 18. Injector Driver (OUTx) Fault Operation

Shutdn Retry Bit 11	TLIM Bit 10	Fault Timer Bit 9	Operation During Short Fault
1	0	X	Timer only, Outputs will retry on period OUT0-OUT3 = 60μs ON, ~10ms OFF
1	1	0	T_{LIM} only, Outputs will retry on T_{LIM} hysteresis.
1	1	1	Timer and T_{LIM}, Outputs will retry on period and driver temperature below threshold. OUT0-OUT3= 60μs ON, ~10ms OFF
0	0	X	Timer only, Outputs will not retry on period OUT0-OUT3 = 60μs ON, OFF
0	1	0	T_{LIM} only, Outputs will not retry on TLim hysteresis.
0	1	1	Timer and T_{LIM}, Outputs will not retry on period or T_{LIM}. OUT0-OUT3 = 60μs ON, OFF

OUTPUT DRIVER DIAGNOSTICS.

Short to battery, Temperature Limit (T_{LIM}) and open load faults are reported through the All Status Response message Table 21.

OFF OPEN LOAD PULL-DOWN CURRENT ENABLE BITS

An open load on the output driver is detected by the voltage level on the drain of the MOSFET in the off state. Internal to the device is a 75μA pull-down current sink. In the event of an open load the drain voltage is pulled low. When the voltage crosses the threshold, and open load is detected. The pull-down current source may be disabled by bit 0 through bit 3 in the LSD Fault Command. With the driver off and the Off Open Load bit disabled, the Off Open Load fault status bit will be logic 0.

ON OPEN LOAD ENABLE BITS

The On State Open Load enable bit allows the user to determine an On State Open Load. When the On State Open Load bit disabled, the On State Fault bit is always logic 0. On Open Load is determined by monitoring the current through the OUTx MOSFET. In the ON state, currents less than 20 to 200mA are considered open.

Table 19. InjectorDriver Diagnostics

Program State			Fault	Fault Bits			
Off State Open Load Pull Dwn	On State Open Load En Bit	Driver On/Off	Output STB STG OPEN	OUTx Batt Short Fault	OUTx OFF Open Fault	OUTx ON Open Fault	Fault Reported
0	X	Off	STB	0	0	0	No Fault
0	X	Off	STG	0	0	0	No Fault
0	X	Off	OPEN	0	0	0	No Fault
1	X	Off	STB	0	0	0	No Fault
1	X	Off	STG	0	1	0	Open Load
1	X	Off	OPEN	0	1	0	Open Load
X	0	On	STB	1	0	0	Short to Batt
X	0	On	STG	0	0	0	No Fault
X	0	On	OPEN	0	0	0	No Fault
X	1	On	STB	1	0	0	Short to Batt
X	1	On	STG	0	0	1	Open Load
X	1	On	OPEN	0	0	1	Open Load

CLOCK CALIBRATION COMMAND

In cases where an accurate time base is required, the user must calibrate the internal timers using the *clock calibration command* (refer to Table 20). After the 33810 device receives the calibration command, the device expects to receive a 32µs logic [0] calibration pulse on the $\overline{CS}$ pin. The pulse is used to calibrate the internal clock. Any SPI message may be sent during the 32µs calibration chip select. Because the oscillator frequency may shift up to 35% with temperature, calibration is required for an accurate time base. The *calibration command* should be used to update the device on a periodic basis.

SPI COMMAND SUMMARY

The SPI commands are defined as 16 bits with 4 address control bits and 12 command data bits. There are 12 separate commands that are used to set operational parameters of device. The operational parameters are stored internally in 16 bit registers.

Table 20 defines the commands and default state of the internal registers at POR. SPI commands may be sent to the device at any time in NORMAL STATE.

Messages sent are acted upon on the rising edge of the $\overline{CS}$ input.

Table 20. SPI Command Message Set and Default State

Command		Control Address Bits				Command Bits											
	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Registers Command	0	0	0	0	0	1	0	1	0	<0000> Internal Register Address				0	0	0	0
All Status Command	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
SPI Check Command	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
Mode Select Command	1	0	0	0	1	<0000> IGN/GP Mode Select **Set to IGN Mode**				<0> V10 En **Disab**	<0> OVR/ Undr Vtg	X	X	<0> pwm3 EN **Disab**	<0> pwm2 EN **Disab**	<0> pwm1 EN **Disab**	<0> pwm0 EN **Disab**

Table 20. SPI Command Message Set and Default State

Command		Control Address Bits				Command Bits											
	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSD Fault Command	2	0	0	1	0	<10X> LSD Flt Operation shutdn,Tlim,Timer Retry on timer and No Tlim			X	<1> OUT3 ON Open Load **Enabl**	<1> OUT2 ON Open Load **Enabl**	<1> OUT1 ON Open Load **Enabl**	<1> OUT0 ON Open Load **Enabl**	<1> OUT3 OFF Open Load **Enabl**	<1> OUT2 OFF Open Load **Enabl**	<1> OUT1 OFF Open Load **Enabl**	<1> OUT0 OFF Open Load **Enabl**
Driver ON/OFF Command 0 = OFF, 1 = ON	3	0	0	1	1	X	X	X	X	<0000> GPGD **OFF** (ignored in Ignition Mode)				<0000> OUTx Driver **OFF**			
Spark Command	4	0	1	0	0	<100> Max Dwell Timer MaxDwell **Default=32 ms** (In Ignition Mode Only)			<0> Max Dwell En **Disab**	<0> Over lap Dwell Disab	<0> Gain Sel **Gain = 1**	<0> Soft Shut Dn En **Disab**	<0> Open 2ed Clmp **Disab**	<11> Open Secondary **OSFLT =100 µs**		<01> End Spark Threshold VPWR +5.5 V	
End Spark Filter	5	0	1	0	1	X	X	X	X	X	X	X	X	X	X	<01> End Spark Filter 4.0 µs	
DAC Command	6	0	1	1	0	<1000> MAXI DAC Threshold MAXI=14 A				<100> Overlap Setting **Overlap 50%**				<01010> NOMI DAC Threshold NOMI=5.5 A			
GPGD Short Threshold Voltage Command	7	0	1	1	1	<011> Short to Batt V_{FB3} **Vth = 2.0 V**				<011> Short to Batt V_{FB2} **Vth = 2.0 V**				<011> Short to Batt V_{FB1} **Vth = 2.0 V**		<011> Short to Batt V_{FB0} **Vth = 2.0 V**	
GPGD Short Duration Timer Command	8	1	0	0	0	<011> Short to Batt t_{FB3} **Timer = 240 µs**				<011> Short to Batt t_{FB2} **Timer = 240 µs**				<011> Short to Batt t_{FB1} **Timer = 240 µs**		<011> Short to Batt t_{FB0} **Timer = 240 µs**	
GPGD Fault Operation Select Command	9	1	0	0	1	<1111> Retry/Shutdown Bit **Retry on Fault**				X	X	X	X	<0000> Shutdown Drivers on MAXI **Disabled**			
PWM0 to PWM3 Freq & DC Command	A	1	0	1	0	<00> PWMx address **PWM0**		<000> PWM Frequency **10 Hz**		<0000000> PWM Duty Cycle **0% Duty Cycle**							
INVALID COMMAND	B	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
INVALID COMMAND	C	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
INVALID COMMAND	D	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
Clock Calibration Command	E	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
INVALID COMMAND	F	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

SPI RESPONSE REGISTERS

Fault reporting is accomplished through the SPI interface. All logic [1]s received by the MCU via the SO pin indicate faults. All logic [0]s received by the MCU via Pin indicate no faults. Timing between two write words must be greater than the fault timer to allow adequate time to sense and report the proper fault status.

.

Table 21. SPI Response Messages

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Next SO Response to: SPI Check Command	0	0	0	0	1	1	0	1	0	0	0	0	1	0	1	0
Next SO Response to HEX1 to HEX A Commands and Read All Status Command ALL STATUS RESPONSE	Reset	COR	SOR	NMF	IGN3 Fault	IGN2 Fault	IGN1 Fault	IGN0 Fault	GP3 Fault	GP2 Fault	GP1 Fault	GP0 Fault	OUT3 Fault	OUT2 Fault	OUT1 Fault	OUT0 Fault
Next SO Response to READ REGISTER COMMAND	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address **<0000>** All Status Register 0 = No Fault, 1 = Fault	Reset	COR	SOR	NMF	IGN3 Fault	IGN2 Fault	IGN1 Fault	IGN0 Fault	GP3 Fault	GP2 Fault	GP1 Fault	GP0 Fault	OUT3 Fault	OUT2 Fault	OUT1 Fault	OUT0 Fault
Address **<0001>** OUT1, OUT0 Fault Register 0 = No Fault, 1 = Fault	Reset	COR	OVER Voltage	LOW Voltage	0	0	0	0	OUT1 TLIM Fault	OUT1 Battery Short Fault	OUT1 OFF Open Fault	OUT1 ON Open Fault	OUT0 TLIM Fault	OUT0 Battery Short Fault	OUT0 OFF Open Fault	OUT0 ON Open Fault
Address **<0010>** OUT3, OUT2 Fault Register 0 = No Fault, 1 = Fault	Reset	COR	OVER Voltage	LOW Voltage	0	0	0	0	OUT3 TLIM Fault	OUT3 Battery Short Fault	OUT3 OFF Open Fault	OUT3 ON Open Fault	OUT2 TLIM Fault	OUT2 Battery Short Fault	OUT2 OFF Open Fault	OUT2 ON Open Fault
Address **<0011>** GPGD Mode Fault Register 0 = No Fault, 1 = Fault	Reset	COR	OVER Voltage	LOW Voltage	0	0	0	0	GP3 Short Circuit Fault	GP3 Open Load Fault	GP2 Short Circuit Fault	GP2 Open Load Fault	GP1 Short Circuit Fault	GP1 Open Load Fault	GP0 Short Circuit Fault	GP0 Open Load Fault
Address **<0100>** IGN Mode Fault Register 0 = No Fault, 1 = Fault	Reset	COR	OVER Voltage	LOW Voltage	IGN3 MAXI Fault	IGN3 Max Dwell Fault	IGN3 Open Second Fault	IGN2 MAXI Fault	IGN2 Max Dwell Fault	IGN2 Open Second Fault	IGN1 MAXI Fault	IGN1 Max Dwell Fault	IGN1 Open Second Fault	IGN0 MAXI Fault	IGN0 Max Dwell Fault	IGN0 Open Second Fault
Address **<0101>** Mode Command Register	Reset	COR	OVER Voltage	LOW Voltage	IGN/GP Mode Select				V10 En	OVR Vtg	X	X	PWM 3 EN	PWM 2 EN	PWM 1 EN	PWM 0 EN
Address **<0110>** LSD Fault Command Register	Reset	COR	OVER Voltage	LOW Voltage	LSD Flt Operation shutdn,Tlim,Timer			X	OUT3 ON Open Load	OUT2 ON Open Load	OUT1 ON Open Load	OUT0 ON Open Load	OUT3 OFF Open Load	OUT2 OFF Open Load	OUT1 OFF Open Load	OUT0 OFF Open Load
Address **<0111>** Drvr ON/OFF Command Reg	Reset	COR	OVER Voltage	LOW Voltage	X	X	X	X	GPGD[20]				OUTx Driver[20]			
Address **<1000>** Spark Command Register	Reset	COR	OVER Voltage	LOW Voltage	Max Dwell Timer MaxDwell			Max Dwell En	Overlap Dwell	Gain Sel	Soft Shut Dn En	Open 2ed Clmp	Open Secondary		End Spark Threshold	

Notes

20. These bits refer to command On or Off state in the command registers, not the state of the respective output lines. These bits are not to be confused with the ignition mode state which is controlled only by the parallel inputs and their state is not reflected in these bits.

Table 21. SPI Response Messages

Address **<0101>** End Spark filter Register	Reset	COR	OVER Voltage	under voltage	X	X	X	X	X	X	X	X	X	X	End spark Filter
Address **<1010>** DAC Command Register	Reset	COR	OVER Voltage	LOW Voltage	MAXI DAC Threshold				Overlap Setting			NOMI DAC Threshold			
Address **<1011>** GPGD FBx Short to Battery Threshold Voltage Register	Reset	COR	OVER Voltage	LOW Voltage	Short to Batt V_{FB3}				Short to Batt V_{FB2}			Short to Batt V_{FB1}			Short to Batt V_{FB0}
Address **<1100>** GPGD FBx Short to Battery Threshold Timer Register	Reset	COR	OVER Voltage	LOW Voltage	Short to Batt t_{FB3}				Short to Batt t_{FB2}			Short to Batt t_{FB1}			Short to Batt t_{FB0}
Address **<1101>** GPGD Fault Operation Register	Reset	COR	OVER Voltage	LOW Voltage	Retry/Shutdown Bit				X	X	X	X	Shutdown Drivers on IMAX		
Address **<1110>** PWM Freq&DC Register (last channel programmed)	Reset	COR	OVER Voltage	LOW Voltage	PWMx address		PWM Frequency		PWM Duty Cycle						
Address **<1111>** Revision ID, Trim, Clock Cal.	Reset	COR	OVR Vtg	LOW Voltage	3	REV 2	ID 1	0	X	X	CAL Too HI	CAL Too LOW	X	X	TRIM Parity Error	TRIM Lock Out

Legend

COR = Command Out of Range

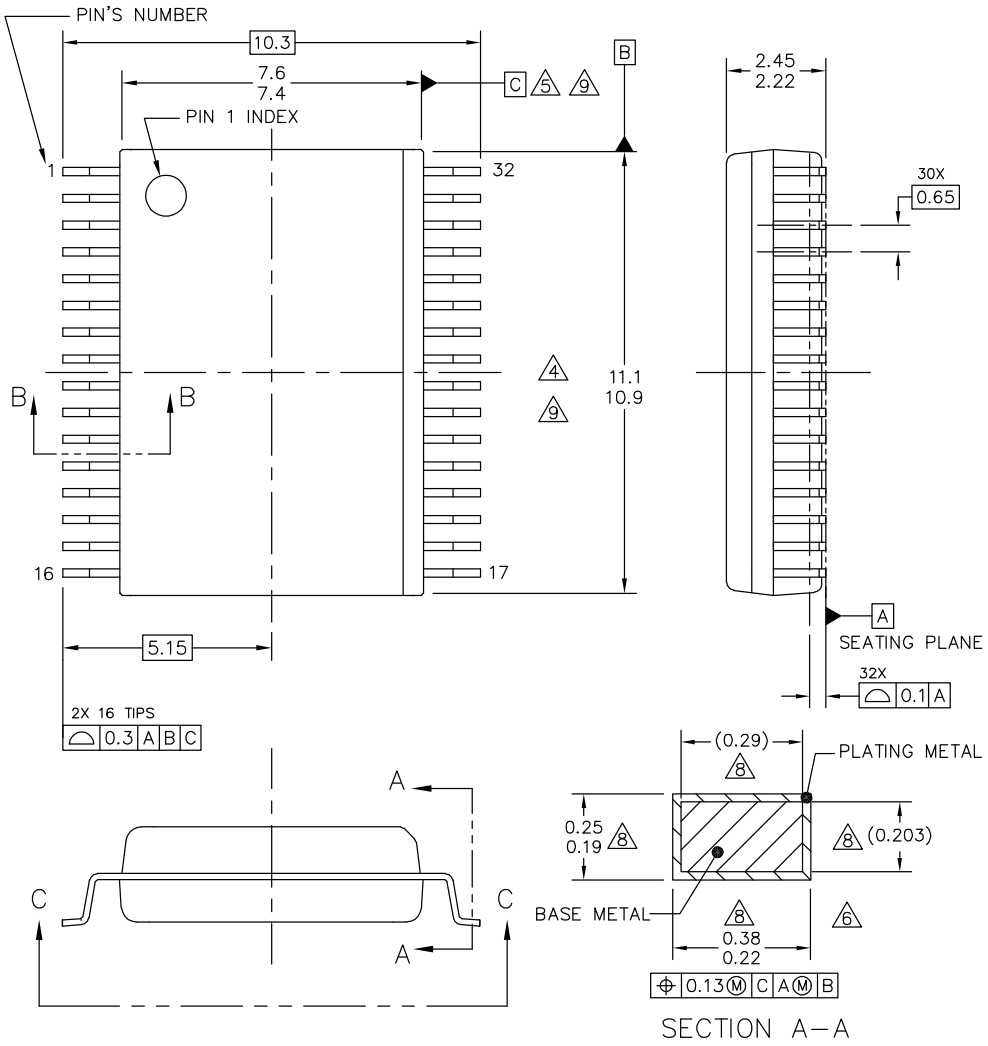
SOR = Supply Out of Range

NMF = Set When Faults Occur on V10 Mode MAXI and NOMI Inputs and V10 Mode Ignition Driver are OFF.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.

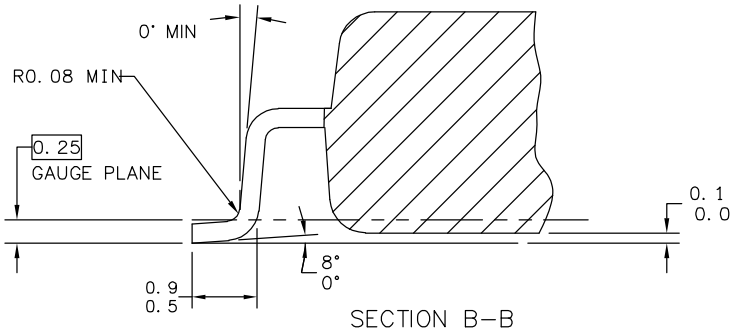


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10556D	REV: D
	CASE NUMBER: 1454–04	20 JUN 2008
	STANDARD: NON–JEDEC	

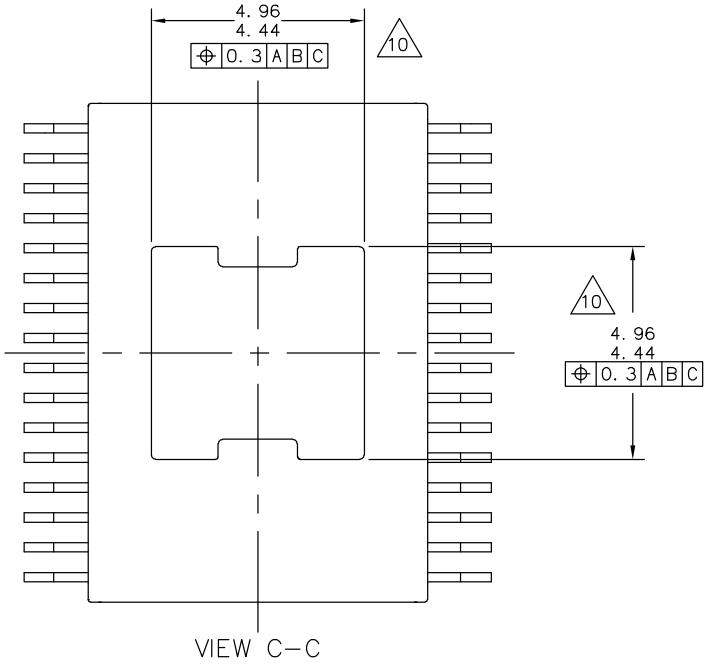
EK (Pb-FREE) SUFFIX
32-PIN
98ASA10556D
ISSUE D

33810

.



SECTION B–B



VIEW C–C

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10556D	REV: D
	CASE NUMBER: 1454–04	20 JUN 2008
	STANDARD: NON–JEDEC	

EK (Pb-FREE) SUFFIX
32-PIN
98ASA10556D
ISSUE D

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10556D	REV: D
	CASE NUMBER: 1454–04	20 JUN 2008
	STANDARD: NON–JEDEC	

EK (Pb-FREE) SUFFIX
32-PIN
98ASA10556D
ISSUE D

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	10/2007	• Initial Release
4.0	2/2008	• Fixed several typos throughout document • Changed Static Electrical Characteristics, Table 3, Digital Interface, $\overline{\text{OUT\_EN}}$ Leakage Current to $V_{DD,}$ maximum from 10 to 50μA. • Reworded Table 15. • Added Table 16 back (it was inadvertently deleted. • Added “Ignition &” to tile in Table 4.
5.0	8/2008	• Updated package drawing.
6.0	12/2008	• Parameter changes to Gate Drive Source Current, Spark Duration Comparator Threshold, NOMI Trip Threshold Accuracy, MAXI Trip Point During Overlapping Dwell, Comparator Hysteresis Voltage, Short to Battery Fault Detection Voltage Threshold, Output OFF Open Load Detection Current, and Input Logic-voltage Hysteresis. • Made change to End of Spark Filter Time Select • Changed orderable Part Number from PCZ33810EK/R2 to MCZ33810EK/R2 on Page 1. • Revised Exposed Pad pin definition in Table 1, page 3. • Changed Package outline drawing to 98ASA10556D.
7.0	7/2010	• Changed introduction paragraph to Tables 3 and 4 from “9.0 V ≤ VPWR ≤ 18 V” to “6.0 V ≤ VPWR ≤ 32 V” • Changed Gate Driver Parameters of $V_{GS(ON)}$ from 5.0 to 4.8.
8.0	7/2010	• Changed Table 3 Characteristics from 18V to 32V for: $I_{VPWR(SS),}$ $I_{(OFF)OCO}$ and $I_{FBX(FLT-SNS)}$
9.0	2/2011	• Changed See Output OFF Open Load Detection Current on page 6 from 100 μA to 115 μA for the maximum value.
10.0	4/2011	• Corrected Table 13, End of Spark Filter Time Select. • Corrected Table 20, SPI Command Message Set and Default State (Command: End Spark Filter).

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC33810
Rev. 10.0
4/2011