FemtoClock® Crystal-to-3.3V, 2.5V LVPECL 400MHz Frequency Synthesizer

ICS843801I-24

DATA SHEET

General Description

The ICS843801I-24 is a 400MHz Frequency Synthesizer. The ICS843801I-24 uses an 18pF parallel resonant crystal over the range of 21.5625MHz - 25.3125MHz. The ICS843801I-24 has excellent <1ps phase jitter performance, over the 12kHz - 20MHz integration range. The ICS843801I-24 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

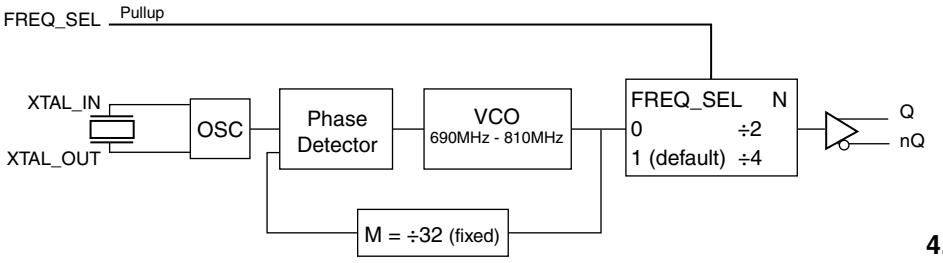
Features

- One differential 3.3V, 2.5V LVPECL output
- Crystal oscillator interface, 18pF parallel resonant crystal (21.5625MHz - 25.3125MHz)
- Output frequency range: 172.5MHz - 202.5MHz, and 345MHz - 405MHz
- VCO range: 690MHz – 810MHz
- RMS phase jitter at 400MHz, using a 25MHz crystal (12kHz – 20MHz): 0.88ps (typical), @ 3.3V
- Full 3.3V or 2.5V operating supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

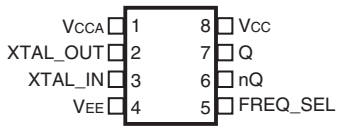
Common Configuration Table

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	0	32	2	16	400
25	1 (default)	32	4	8	200

Block Diagram



Pin Assignment



ICS843801I-24
8 Lead TSSOP
4.40mm x 3.0mm x 0.925 package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin
2, 3	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	V_{EE}	Power		Negative supply pin.
5	FREQ_SEL	Input	Pullup	Frequency select pin, LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.09	3.3	V_{CC}	V
I_{CC}	Power Supply Current				66	mA
I_{CCA}	Analog Supply Current				9	mA
I_{EE}	Power Supply Current				72	mA

Table 3B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.09	2.5	V_{CC}	V
I_{CC}	Power Supply Current				60	mA
I_{CCA}	Analog Supply Current				9	mA
I_{EE}	Power Supply Current				72	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.3V	2		V_{CC} + 0.3	V
		V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.3V	-0.3		0.8	V
		V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 3D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 3E. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		21.5625		25.3125	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		172.5		202.5	MHz
			345		405	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	200MHz, Integration Range: 12kHz – 20MHz		0.87	1.02	ps
		400MHz, Integration Range: 12kHz – 20MHz		0.88	0.98	ps
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 2				13	ps
t_{jit}(per)	RMS Period Jitter			0.18	2.1	ps
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle		48		52	%

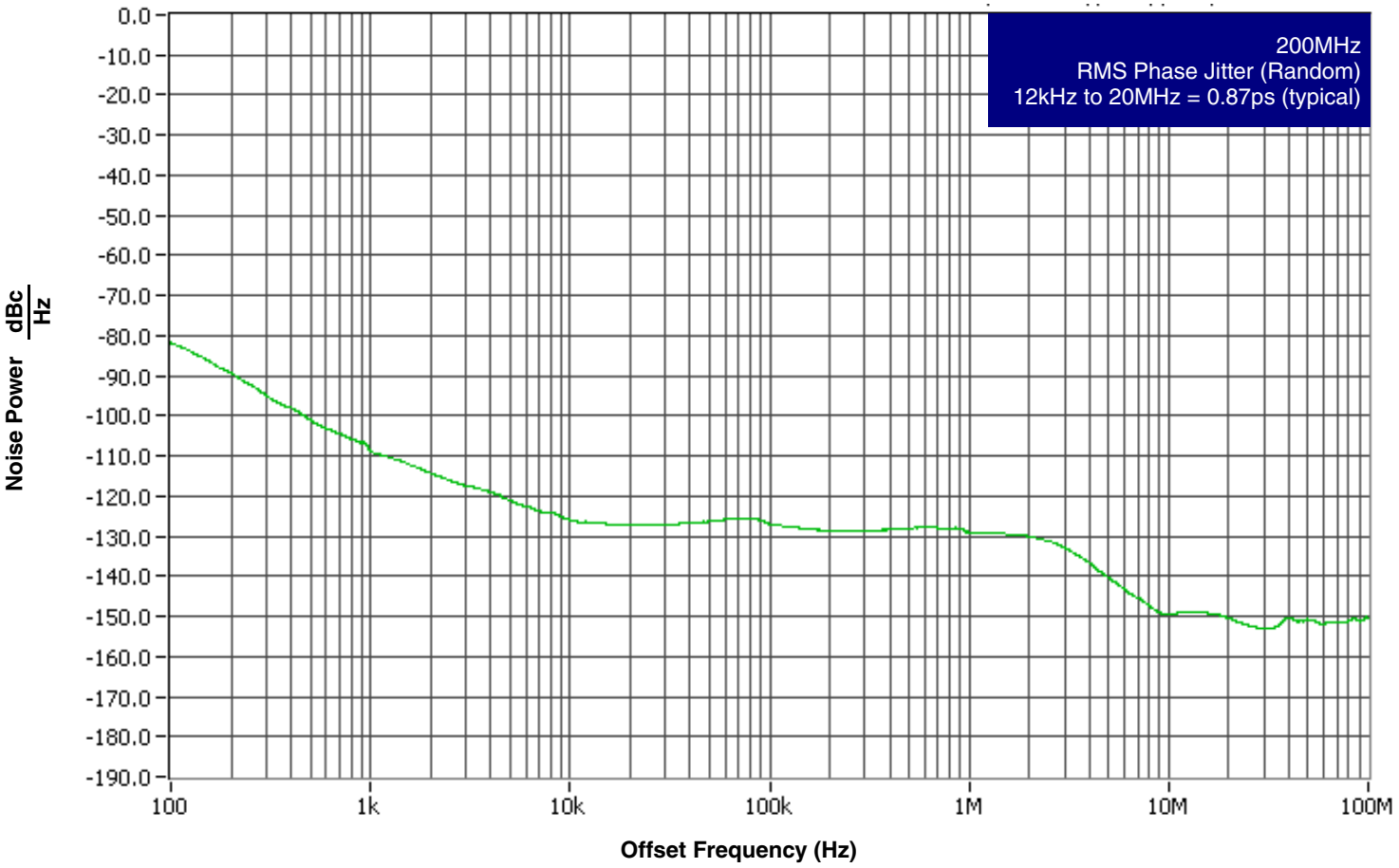
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: These parameters are guaranteed by characterization. Not tested in production.

Table 5B. AC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°

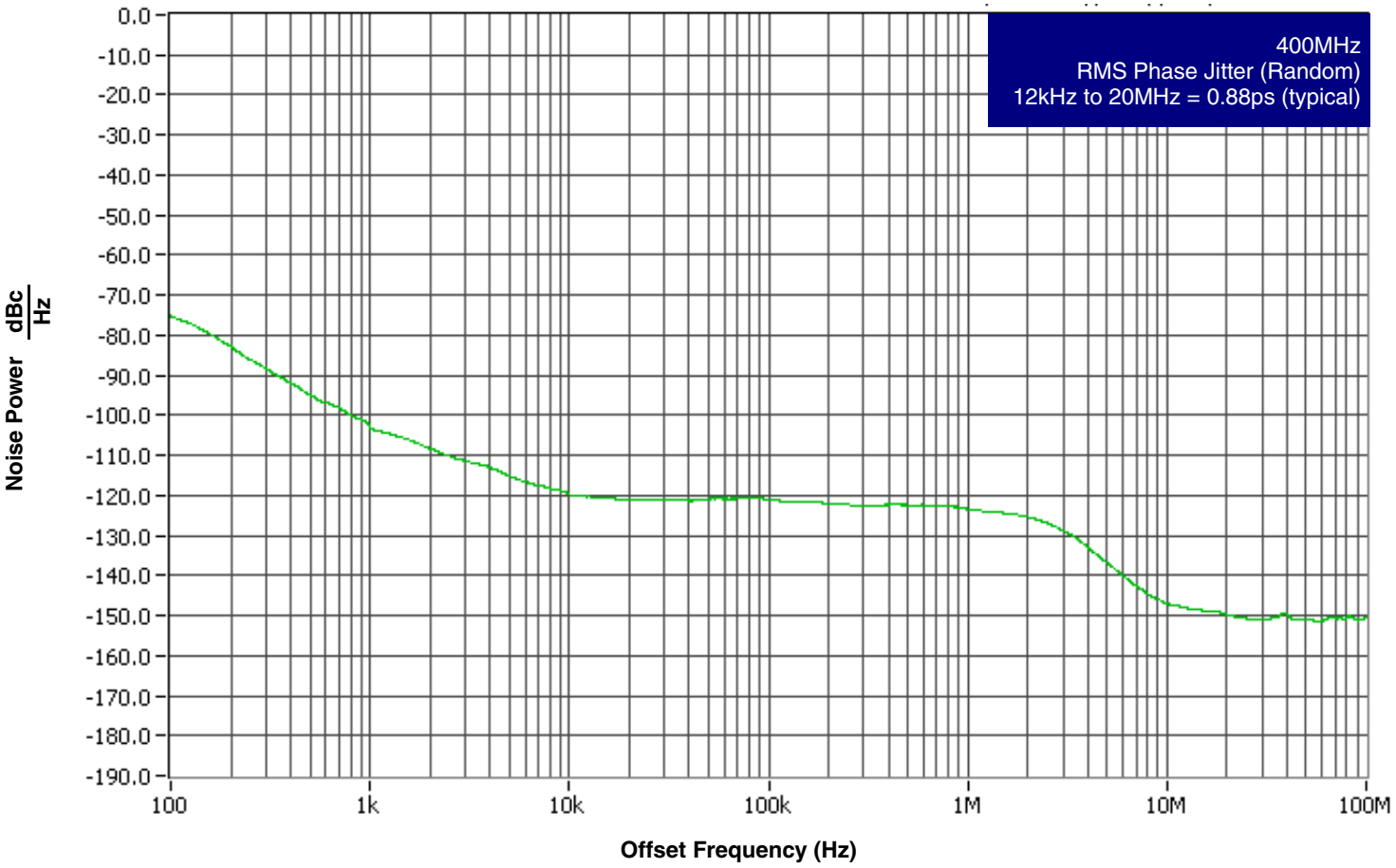
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		172.5		202.5	MHz
			345		405	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	200MHz, Integration Range: 12kHz – 20MHz		0.87	1.05	ps
		400MHz, Integration Range: 12kHz – 20MHz		0.89	1.06	ps
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 2				16	ps
t_{jit}(per)	RMS Period Jitter			0.20	2.6	ps
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: These parameters are guaranteed by characterization. Not tested in production.

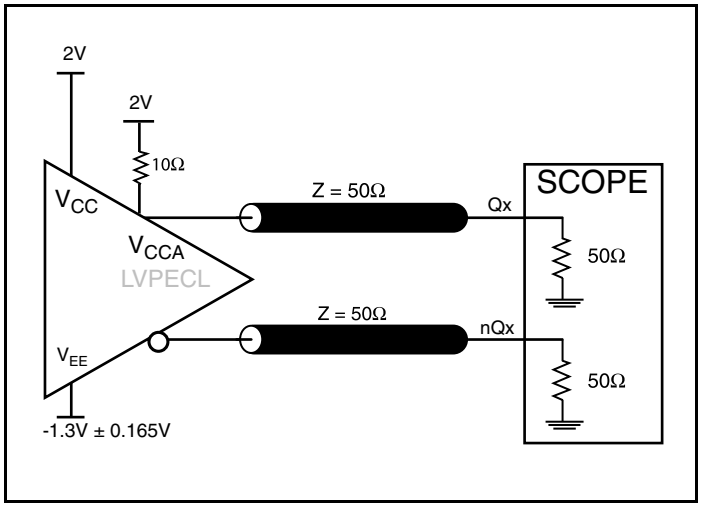
Typical Phase Noise at 200MHz, (3.3V)



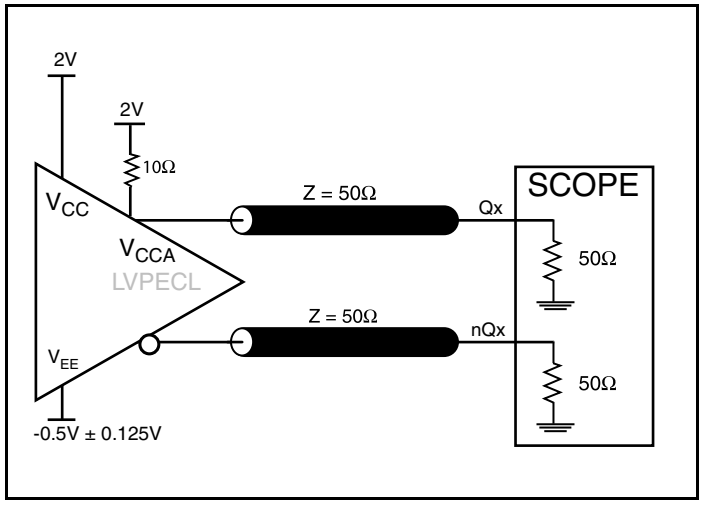
Typical Phase Noise at 400MHz, (3.3V)



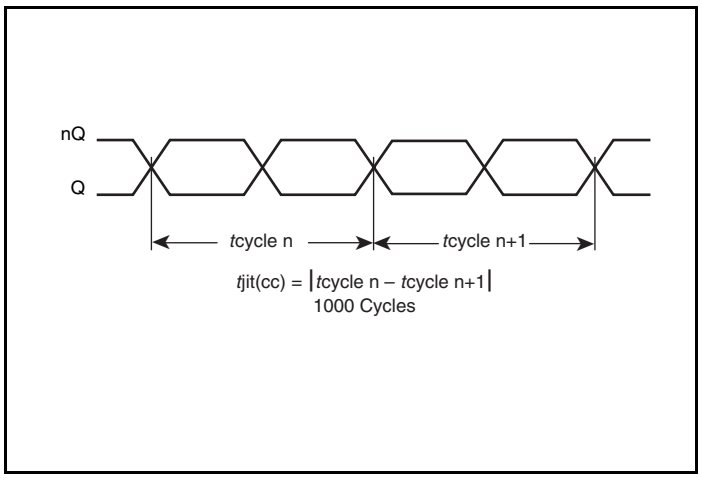
Parameter Measurement Information



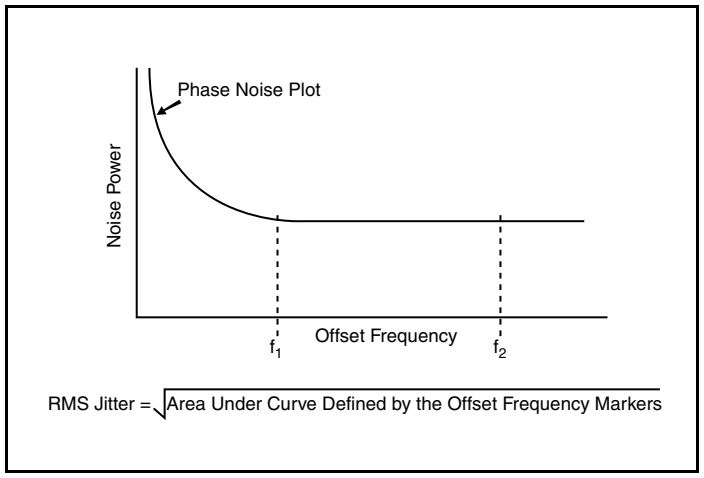
3.3V Core/ 3.3V LVPECL Output Load AC Test Circuit



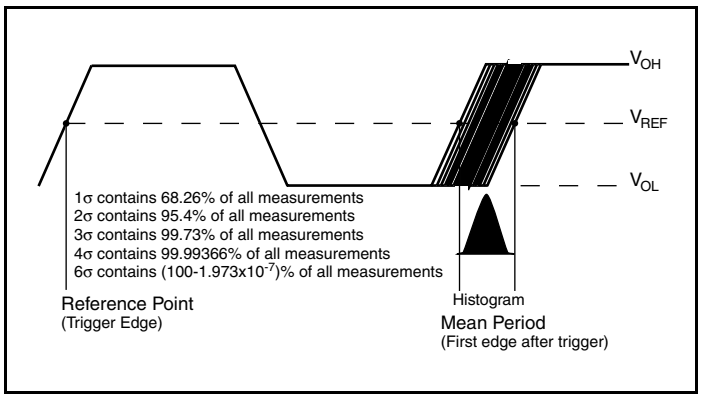
2.5V LVPECL Output Load AC Test Circuit



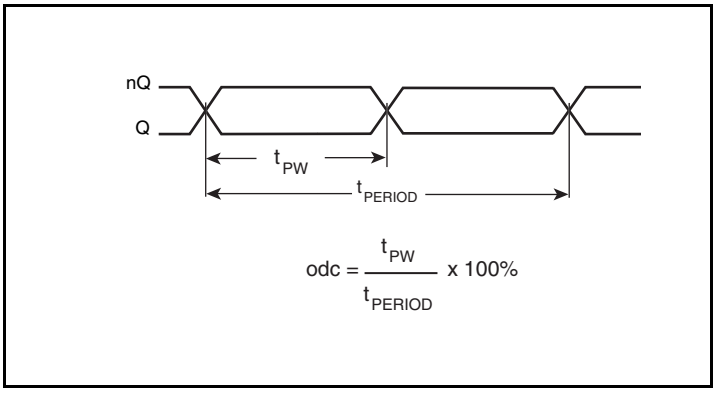
Cycle-to-Cycle Jitter



RMS Phase Jitter

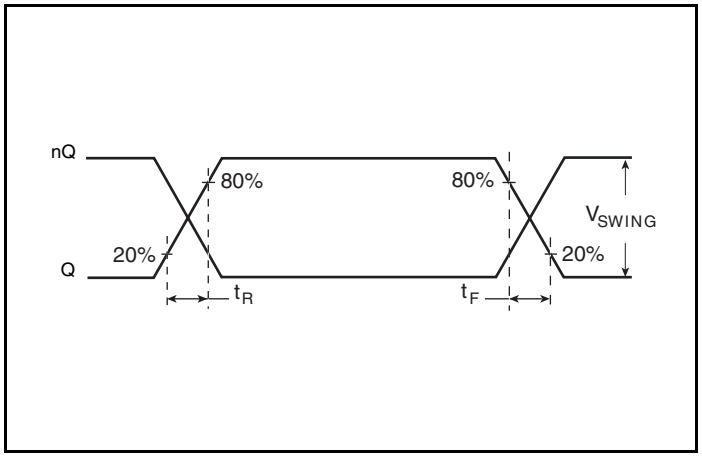


Period Jitter

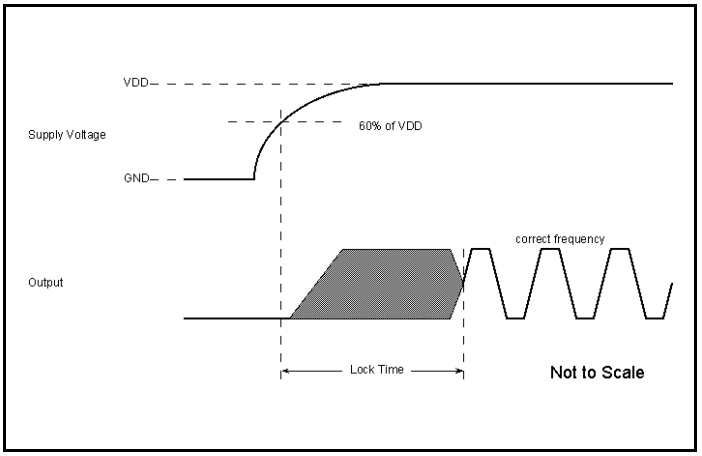


Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Output Rise/Fall Time



PLL Lock Time

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

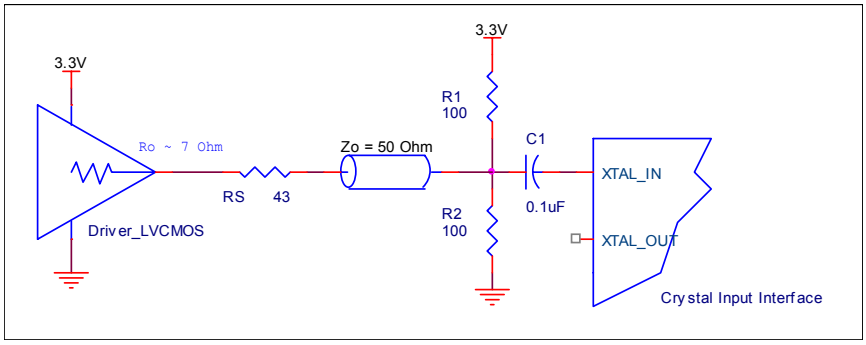


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

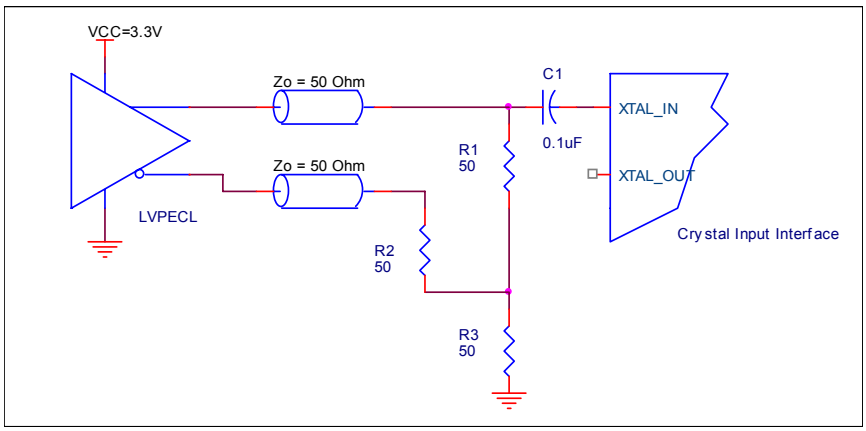


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

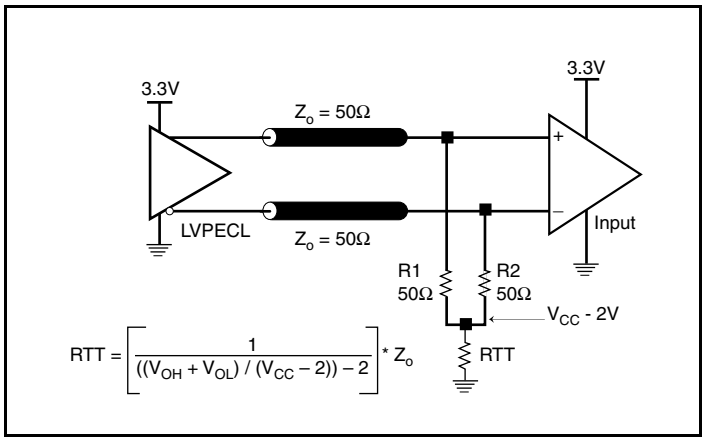


Figure 2A. 3.3V LVPECL Output Termination

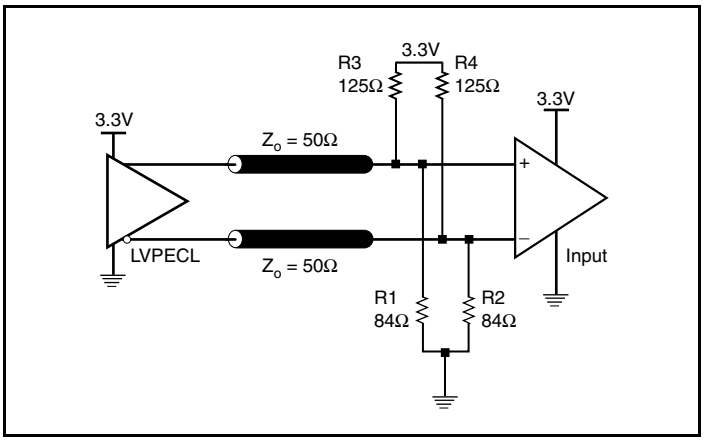


Figure 2B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CO} – 2V. For V_{CC}= 2.5V, the V_{CC}– 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

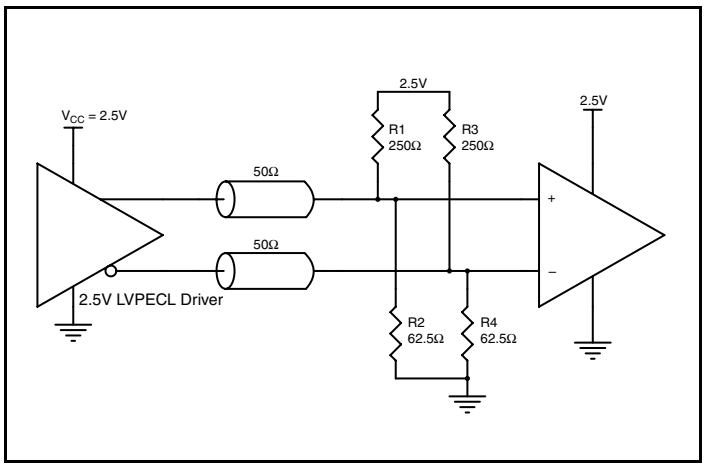


Figure 3A. 2.5V LVPECL Driver Termination Example

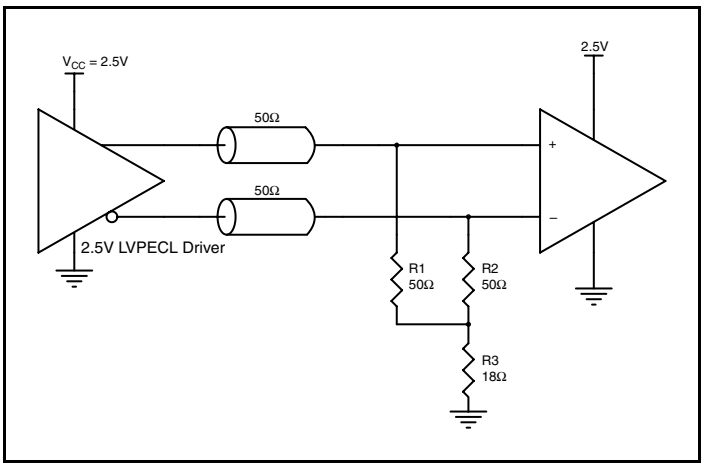


Figure 3B. 2.5V LVPECL Driver Termination Example

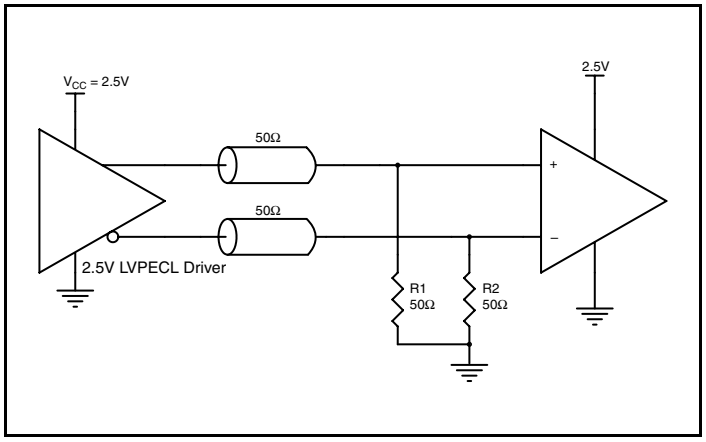


Figure 3C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 4 shows an example of ICS843801I-24 application schematic. In this example, the device is operated at $V_{CC} = V_{CCA} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843801I-24 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

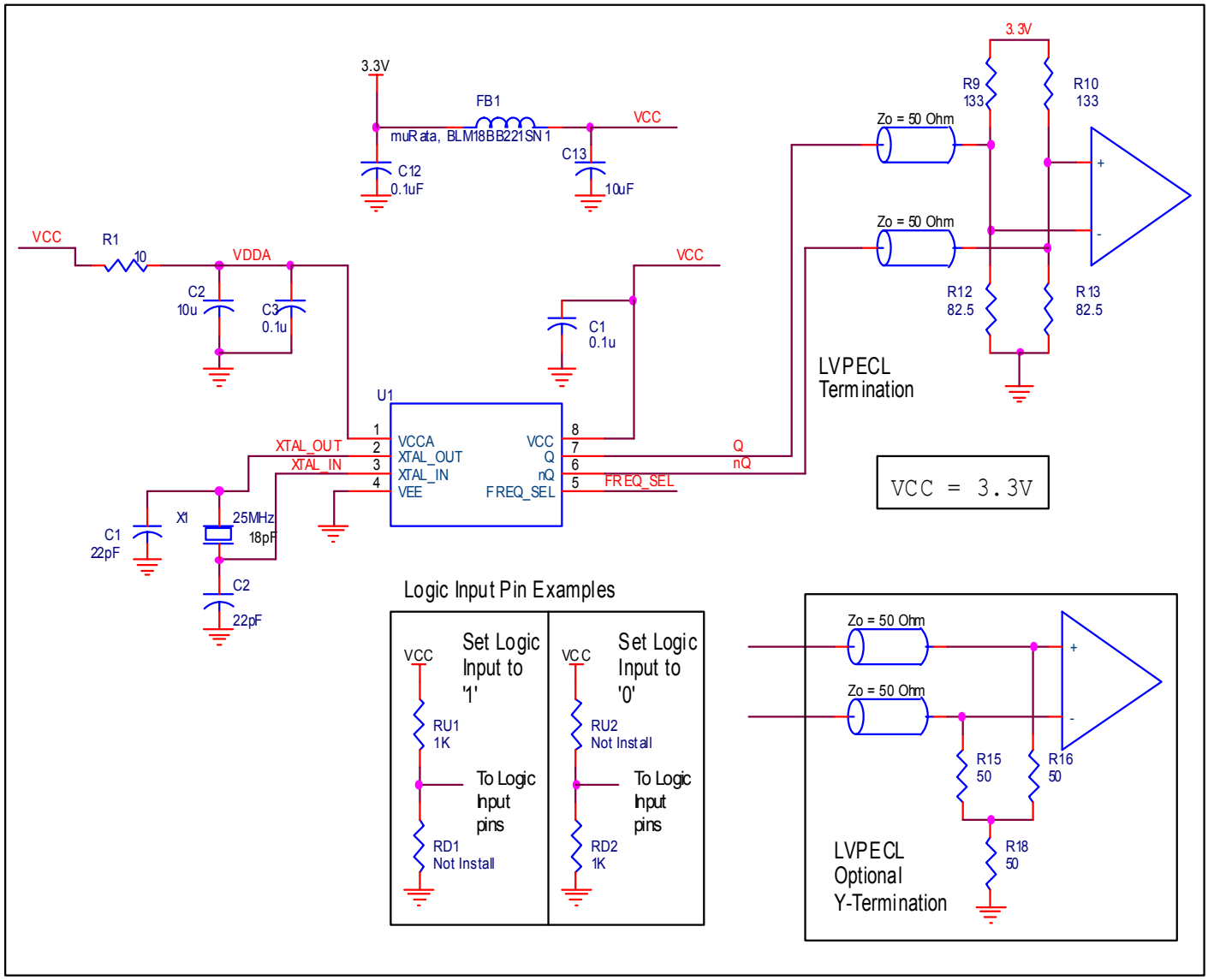


Figure 4. ICS843801I-24 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843801I-24.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843801I-24 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 72mA = **249.48mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 249.48mW + 30mW = **279.48mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.279W * 129.5°C/W = 121.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resitance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 5.*

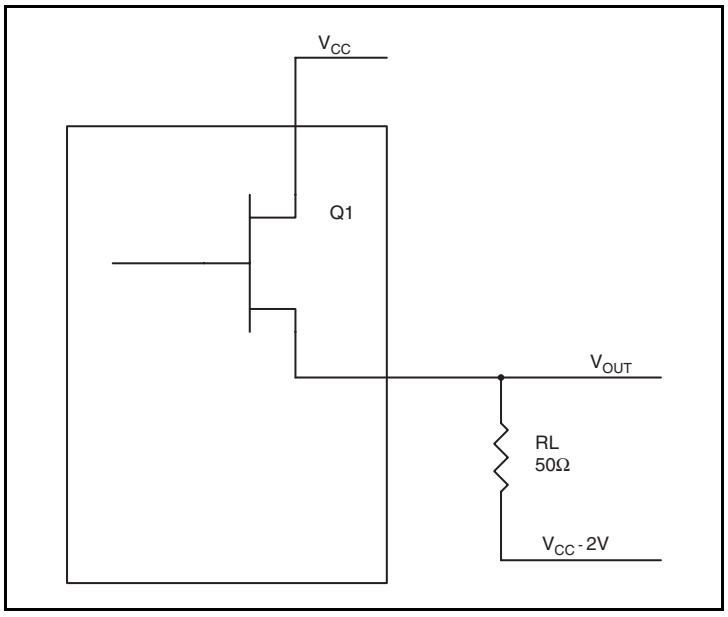


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for ICS843801I-24 is: 1649

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

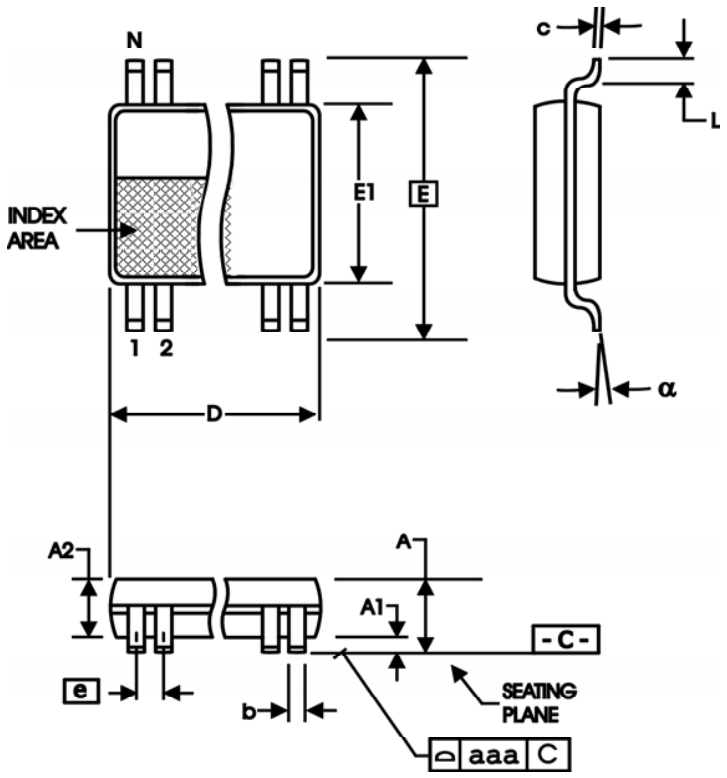


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843801AGI-24LF	AI24L	“Lead-Free” 8 Lead TSSOP	Tube	-40°C to 85°C
843801AGI-24LFT	AI24L	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056