



175MHZ, FEMTOCLOCK™ VCXO BASED SONET/SDH JITTER ATTENUATOR

ICS843002I-40

General Description



The ICS843002I-40 is a member of the HiperClockS™ family of high performance clock solutions from IDT. The ICS843002I-40 is a PLL based synchronous clock generator that is optimized for SONET/SDH line card applications

where jitter attenuation and frequency translation is needed. The device contains two internal PLL stages that are cascaded in series. The first PLL stage uses a VCXO which is optimized to provide reference clock jitter attenuation and to be jitter tolerant, and to provide a stable reference clock for the 2nd PLL stage (typically 19.44MHz). The second PLL stage provides additional frequency multiplication (x32), and it maintains low output jitter by using a low phase noise FemtoClock VCO. PLL multiplication ratios are selected from internal lookup tables using device input selection pins. The device performance and the PLL multiplication ratios are optimized to support non-FEC (non-Forward Error Correction) SONET/SDH applications with rates up to OC-48 (SONET) or STM-16 (SDH). The VCXO requires the use of an external, inexpensive pullable crystal. VCXO PLL uses external passive loop filter components which are used to optimize the PLL loop bandwidth and damping characteristics for the given line card application.

The ICS843002I-40 includes two clock input ports. Each one can accept either a single-ended or differential input. Each input port also includes an activity detector circuit, which reports input clock activity through the LOR0 and LOR1 logic output pins. The two input ports feed an input selection mux. "Hitless switching" is accomplished through proper filter tuning. Jitter transfer and wander characteristics are influenced by loop filter tuning, and phase transient performance is influenced by both loop filter tuning and alignment error between the two reference clocks.

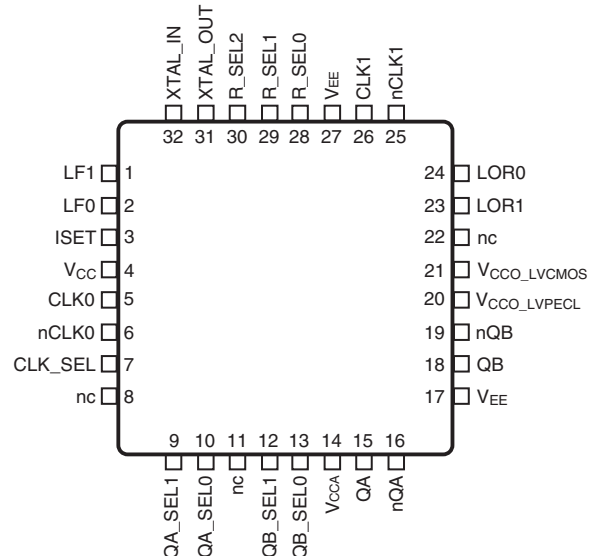
Typical ICS843002I-40 configuration in SONET/SDH Systems:

- VCXO 19.44MHz crystal
- Loop bandwidth: 50Hz - 250Hz
- Input Reference clock frequency selections:
19.44MHz, 38.88MHz, 77.76MHz, 155.52MHz, 311.04MHz, 622.08MHz
- Output clock frequency selections:
19.44MHz, 77.76MHz, 155.52MHz, Hi-Z

Features

- Two Differential LVPECL outputs
- Selectable CLKx, nCLKx differential input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL or single-ended LVC MOS or LV TTL levels
- Maximum output frequency: 175MHz
- FemtoClock VCO frequency range: 560MHz - 700MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz to 20MHz): 0.81ps (typical)
- Full 3.3V or mixed 3.3V core/2.5V output operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment



ICS843002I-40

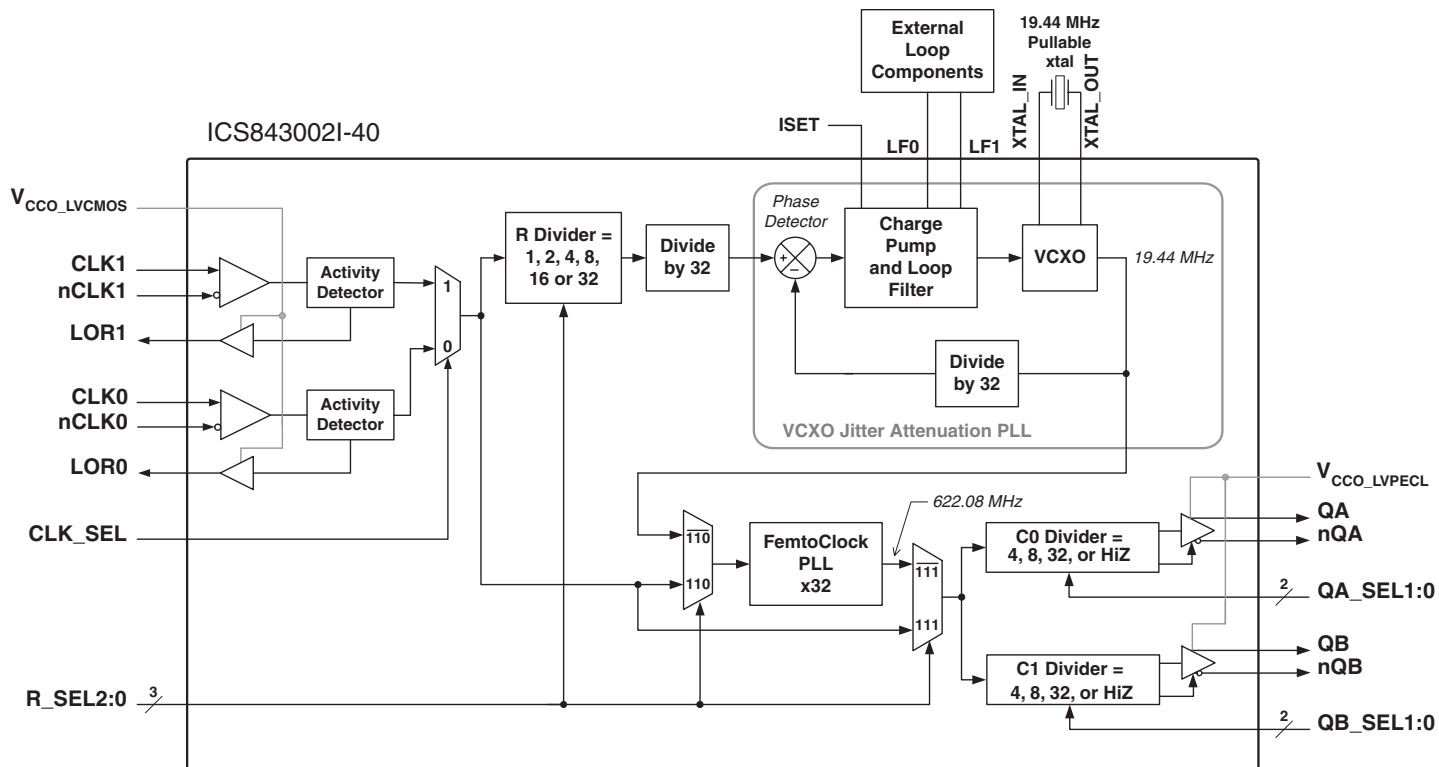
32-Lead VFQFN

5mm x 5mm x 0.925mm package body

K Package

Top View

Block Diagram



NOTE: 19.44MHz VCXO crystal shown is typical for SONET/SDH device applications.

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|------------|------------------------------|---------------------|--------------------|--|
| 1, 2 | LF1, LF0 | Analog Input/Output | | Loop filter connection node pins. |
| 3 | ISSET | Analog Input/Output | | Charge pump current setting pin. |
| 4 | V _{CC} | Power | | Core power supply pin. |
| 5 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 6 | nCLK0 | Input | Pullup Pulldown | Inverting differential clock input. V _{CC} /2 bias voltage when left floating. |
| 7 | CLK_SEL | Input | Pulldown | Input clock select. LVCMOS/LVTTL interface levels. See Table 3A. |
| 8, 11, 22 | nc | Unused | | No connect. |
| 9, 10 | QA_SEL1, QA_SEL0 | Input | Pullup | Output divider control for QA/nQA LVPECL outputs. LVCMOS/LVTTL interface levels. See Table 3C. |
| 12, 13 | QB_SEL1, QB_SEL0 | Input | Pullup | Output divider control for QB/nQB LVPECL outputs. LVCMOS/LVTTL interface levels. See Table 3C. |
| 14 | V _{CCA} | Power | | Analog supply pin. |
| 15, 16 | QA, nQA | Output | | Differential clock output pair. LVPECL interface levels. |
| 17, 27 | V _{EE} | Power | | Negative supply pins. |
| 18, 19 | QB, nQB | Output | | Differential clock output pair. LVPECL interface levels. |
| 20 | V _{CCO_LVPECL} | Power | | Output supply pin for LVPECL outputs. |
| 21 | V _{CCO_LVCMOS} | Power | | Output supply pin for LVCMOS/LVTTL outputs. |
| 23 | LOR1 | Output | | Alarm output, loss of reference for CLK1/nCLK1. LVCMOS/LVTTL interface levels. |
| 24 | LOR0 | Output | | Alarm output, loss of reference for CLK0/nCLK0. LVCMOS/LVTTL interface levels. |
| 25 | nCLK1 | Input | Pullup Pulldown | Inverting differential clock input. V _{CC} /2 bias voltage when left floating. |
| 26 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 28, 29, 30 | R_SEL0, R_SEL1, R_SEL2 | Input | Pulldown | Input divider selection. LVCMOS/LVTTL interface levels. See Table 3B. |
| 31, 32 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. The XTAL_IN is the input. XTAL_OUT is the output. |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 50 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 50 | | kΩ |

Function Tables

Table 3A. Input Reference Selection Function Table

| Input | Function |
|---------|----------------|
| CLK_SEL | Input Selected |
| 0 | CLK0/nCLK0 |
| 1 | CLK1/nCLK1 |

Table 3B. Input Reference Divider Selection Function Table

| Inputs | | | Function |
|--------|--------|--------|---------------------------------|
| R_SEL2 | R_SEL1 | R_SEL0 | R Divider Value or State |
| 0 | 0 | 0 | ÷1 |
| 0 | 0 | 1 | ÷2 |
| 0 | 1 | 0 | ÷4 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷16 |
| 1 | 0 | 1 | ÷32 |
| 1 | 1 | 0 | bypass VCXO PLL |
| 1 | 1 | 1 | bypass VCXO and FemtoClock PLLs |

Table 3C. Output Divider Selection Function Table

| Inputs | | Function |
|---------|---------|--------------------------------|
| QX_SEL1 | QX_SEL0 | Output Divider Value or State |
| 0 | 0 | Output QX/nQX (High-Impedance) |
| 0 | 1 | ÷32 |
| 1 | 0 | ÷8 |
| 1 | 1 | ÷4 |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|-----------------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, V_O (LVCMOS) | -0.5V to $V_{CCO_LVCMOS} + 0.5V$ |
| Outputs, I_O (LVPECL) Continuous Current Surge Current | 50mA 100mA |
| Package Thermal Impedance, θ_{JA} | 37°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, V_{CCO_LVCMOS} , $V_{CCO_LVPECL} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.15$ | 3.3 | V_{CC} | V |
| V_{CCO_LVCMOS} , V_{CCO_LVPECL} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| I_{EE} | Power Supply Current | | | | 210 | mA |
| I_{CCA} | Analog Supply Current | | | | 15 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO_LVCMOS} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|-----------------------------|---|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | QA_SEL[0:1], QB_SEL[0:1] | $V_{CC} = V_{IN} = 3.465V$ | | | 5 | μA |
| | | CLK_SEL, R_SEL[0:2] | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | QA_SEL[0:1], QB_SEL[0:1] | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | μA |
| | | CLK_SEL, R_SEL[0:2] | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | μA |
| V_{OH} | Output High Voltage | LOR0, LOR1 | $V_{CCO_LVCMOS} = 3.465V$, $I_{OH} = 1mA$ | 2.6 | | | V |
| | | | $V_{CCO_LVCMOS} = 2.625V$, $I_{OH} = 1mA$ | 1.8 | | | V |
| V_{OL} | Output Low Voltage | LOR0, LOR1 | $V_{CCO_LVCMOS} = 3.465V$ or $2.625V$, $I_{OL} = -1mA$ | | | 0.5 | V |

Table 4C. Differential DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO_LVPECL} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|---------------------------|-----------------------------------|----------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK0/nCLK0, CLK1/nCLK1 | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK0, CLK1 | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | μA |
| | | nCLK0, nCLK1 | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: V_{IL} cannot be less than -0.3VNOTE 2: Common mode input voltage is defined as V_{IH} .**Table 4D. LVPECL DC Characteristics**, $V_{CC} = V_{CCO_LVPECL} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_LVPECL} - 2V$.

Table 4E. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO_LVPECL} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.5$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.4 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_LVPECL} - 2V$.

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO_LVCMOS} = V_{CCO_LVPECL} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------------------|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | 19.44 | | 175 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 1, 2 | | | | 150 | ps |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 3 | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.81 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 100 | | 800 | ps |
| odc | Output Duty Cycle | | 45 | | 55 | % |

See Parameter Measurement Information section.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

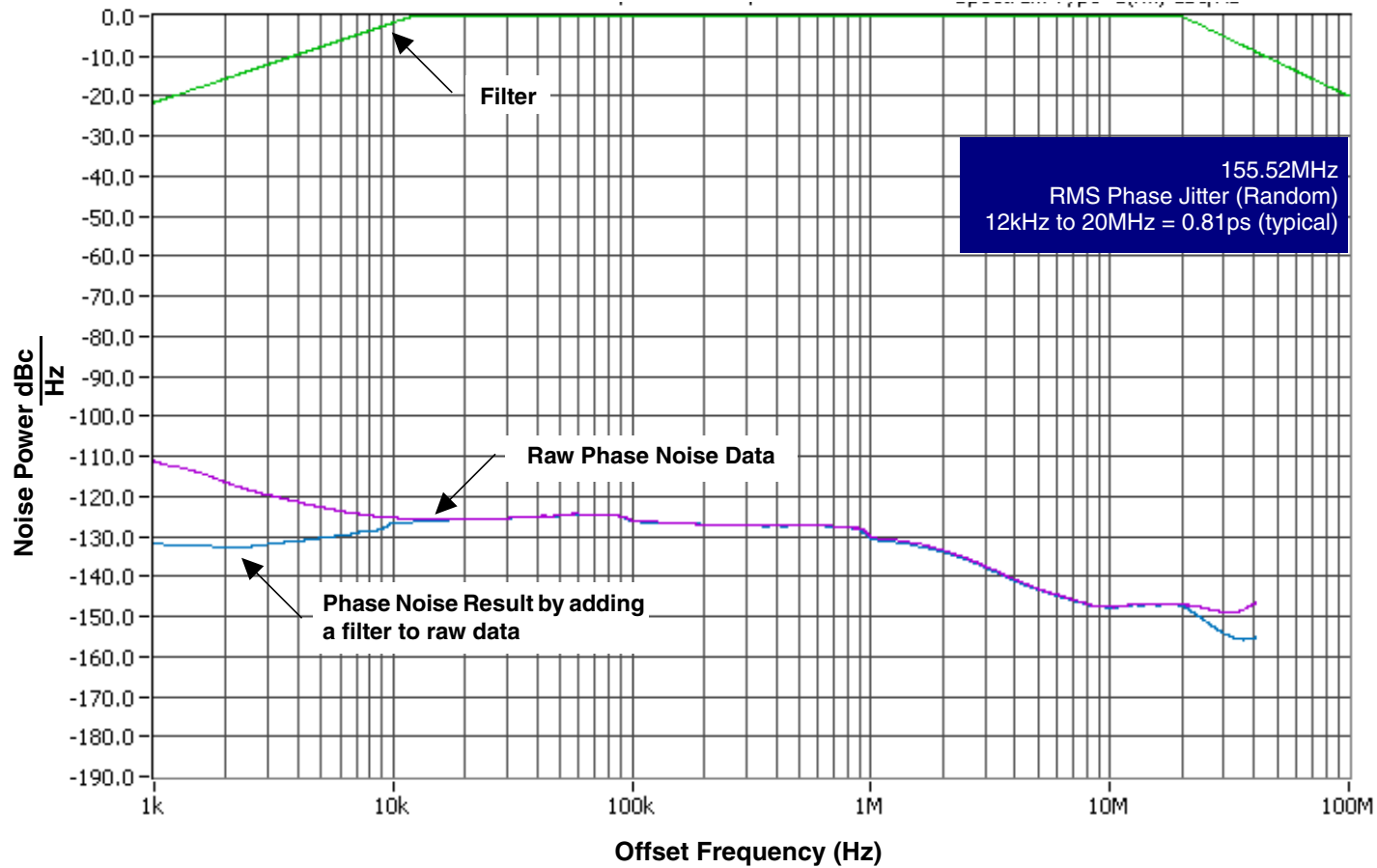
NOTE 1: Defined as skew between outputs at the same supply voltage, same frequency, and with equal load conditions.

Measured at the output differential cross points.

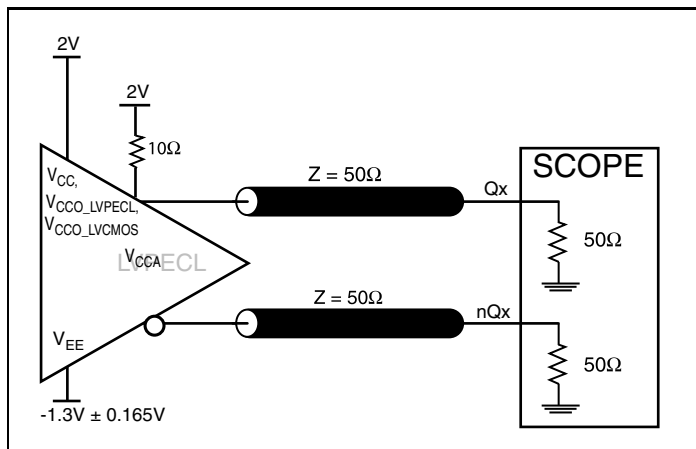
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise plots.

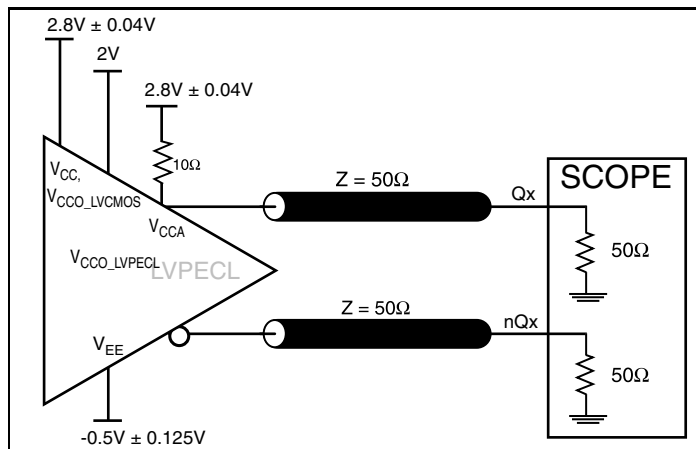
Typical Phase Noise at 155.52MHz



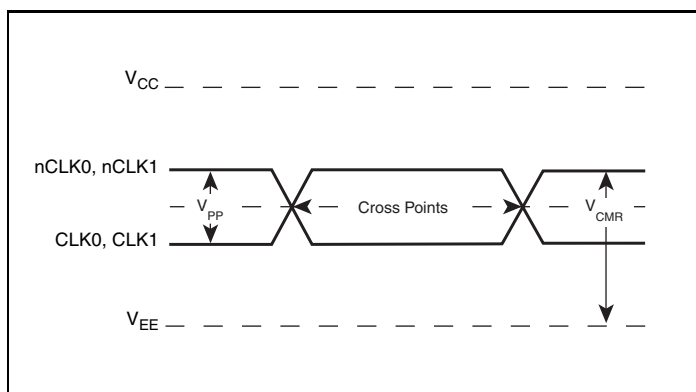
Parameter Measurement Information



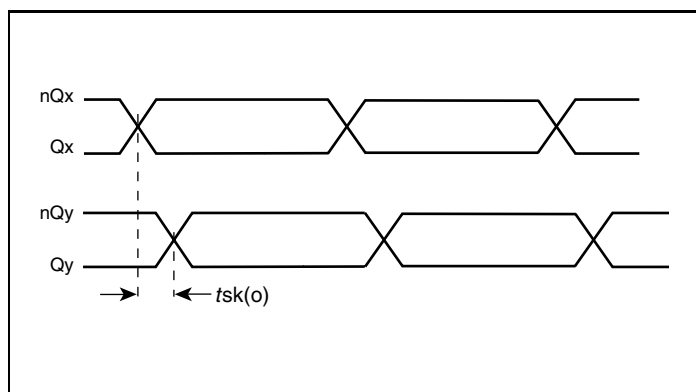
3.3V Core/3.3V LVPECL Output Load AC Test Circuit



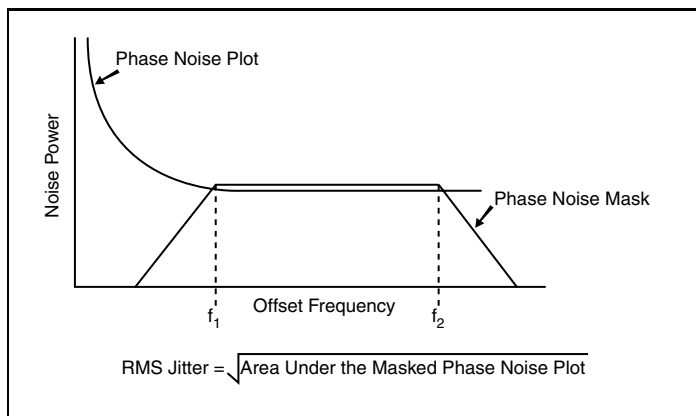
3.3V Core/2.5V LVPECL Output Load AC Test Circuit



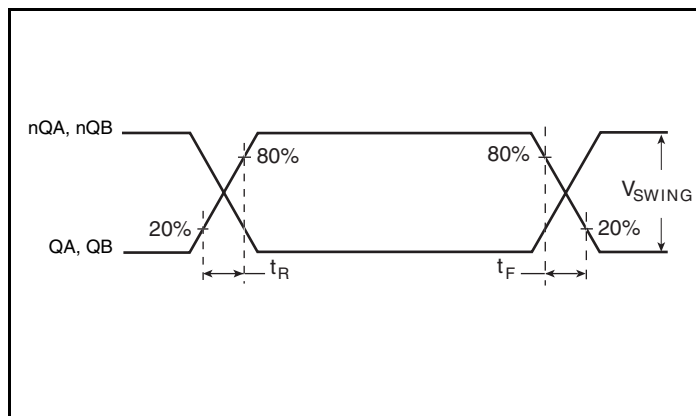
Differential Input Level



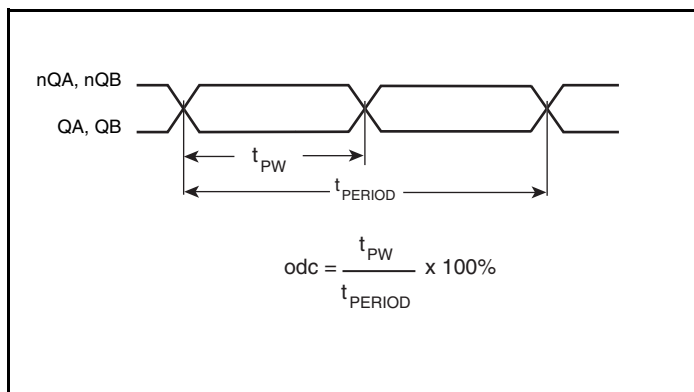
Output Skew



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground.

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843002I-40 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , V_{CCO_LVPECL} and V_{CCO_LVCMOS} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{CCA} pin.

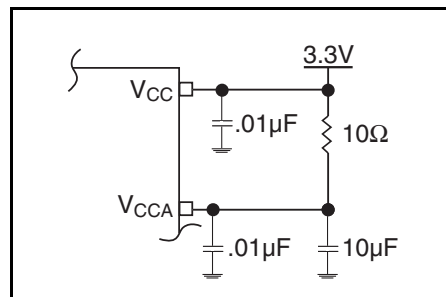


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio of $R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3\text{V}$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

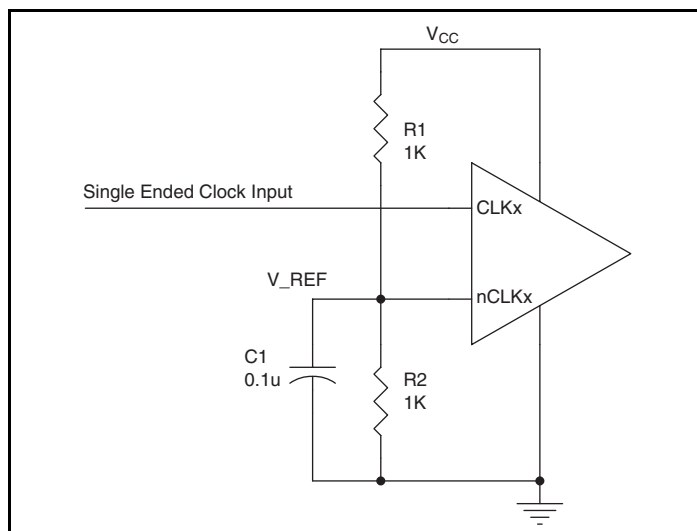


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

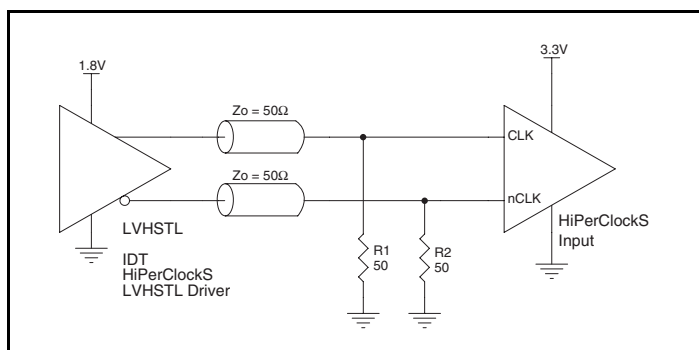


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

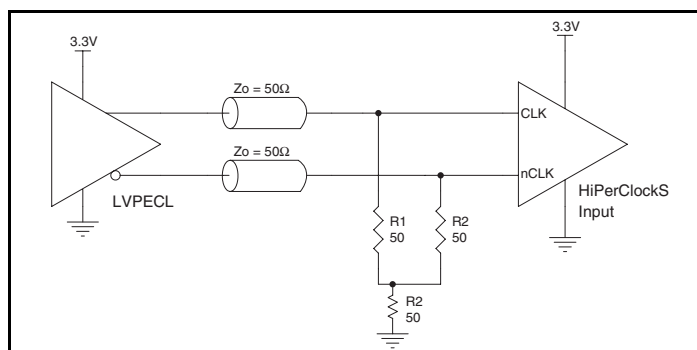


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

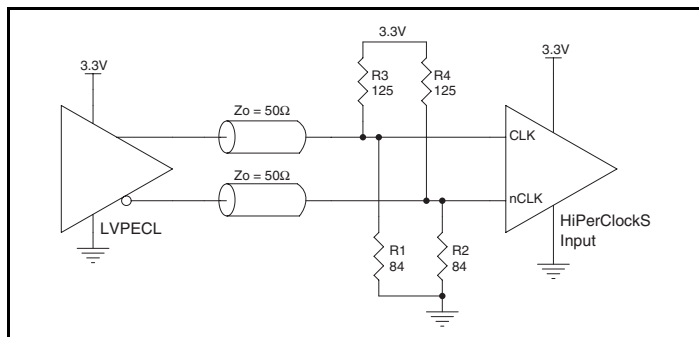


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

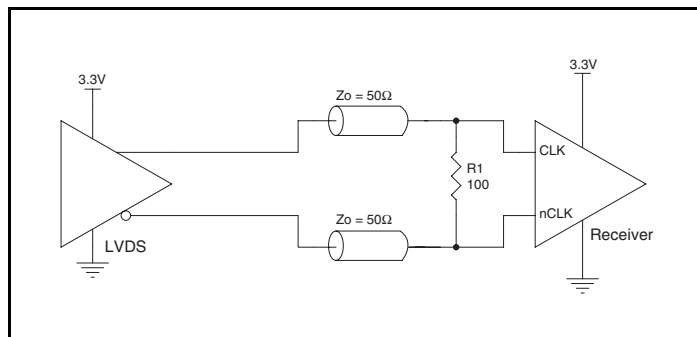


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

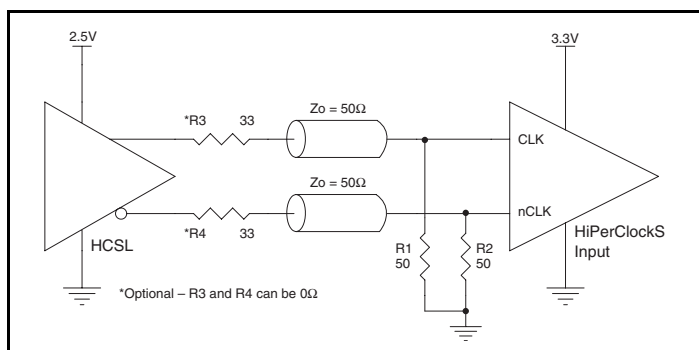


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

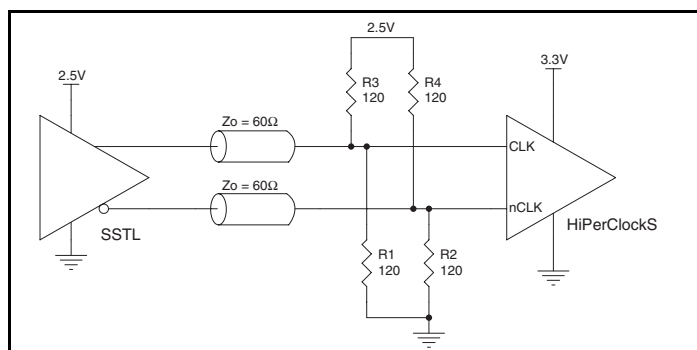


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are

application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

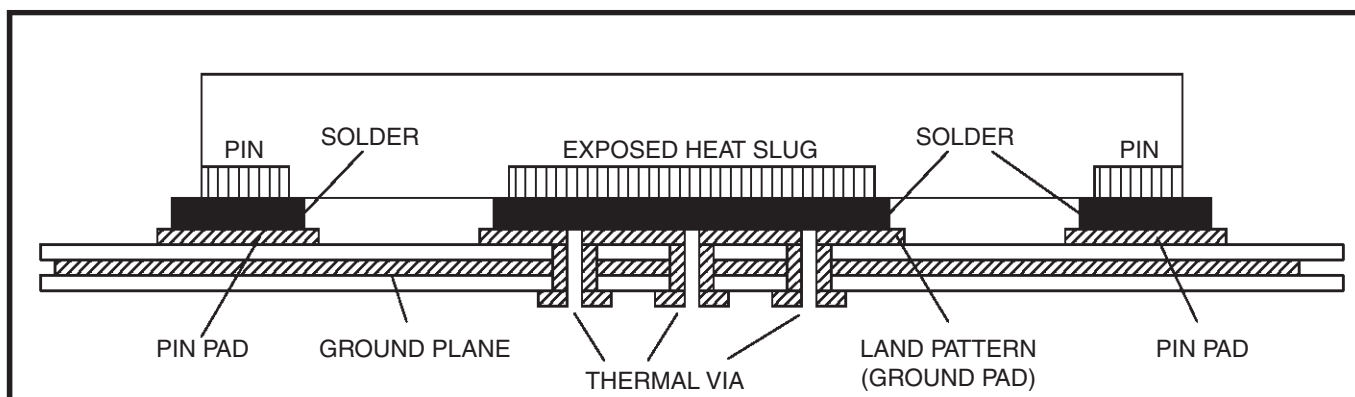


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

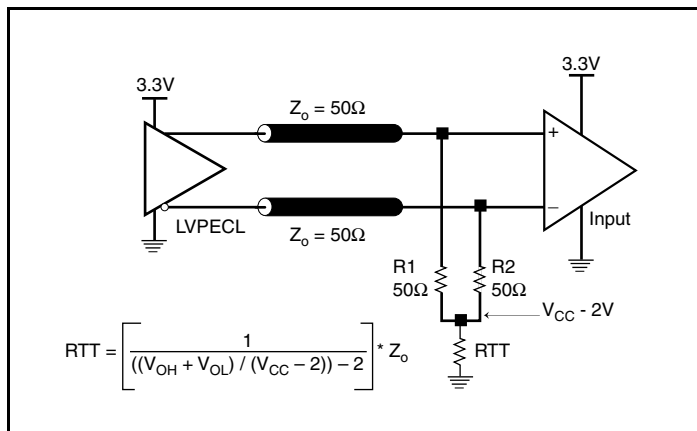


Figure 5A. 3.3V LVPECL Output Termination

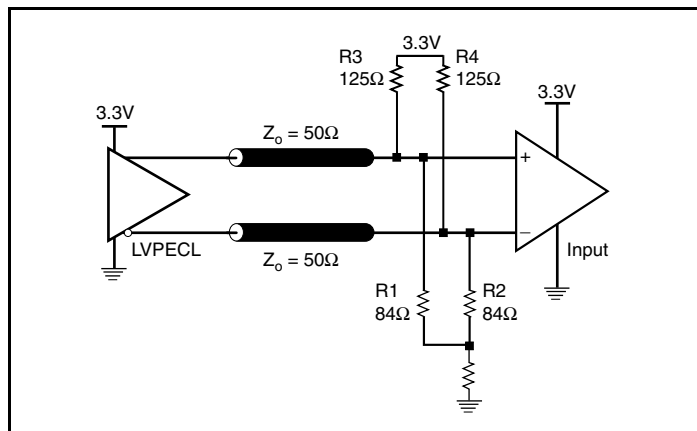


Figure 5B. 3.3V LVPECL Output Termination

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC0} = 2.5V$, the $V_{CC0} - 2V$ is very close to

ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C*.

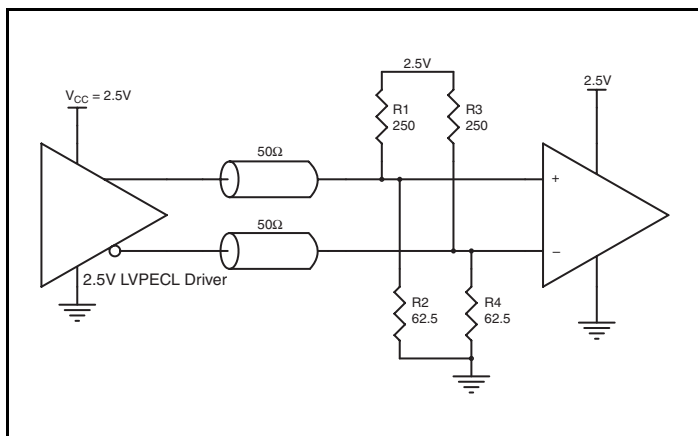


Figure 6A. 2.5V LVPECL Driver Termination Example

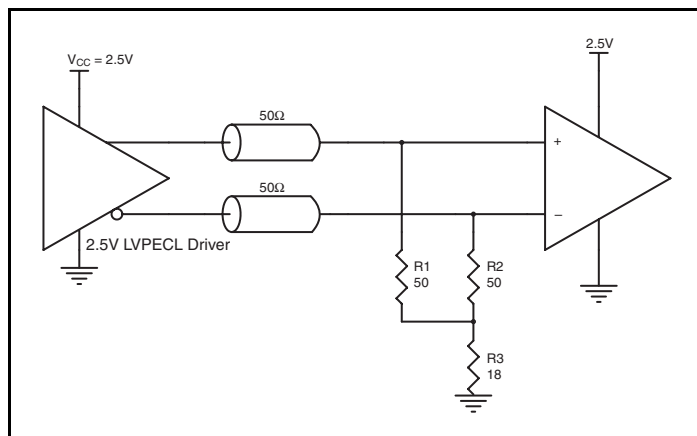


Figure 6B. 2.5V LVPECL Driver Termination Example

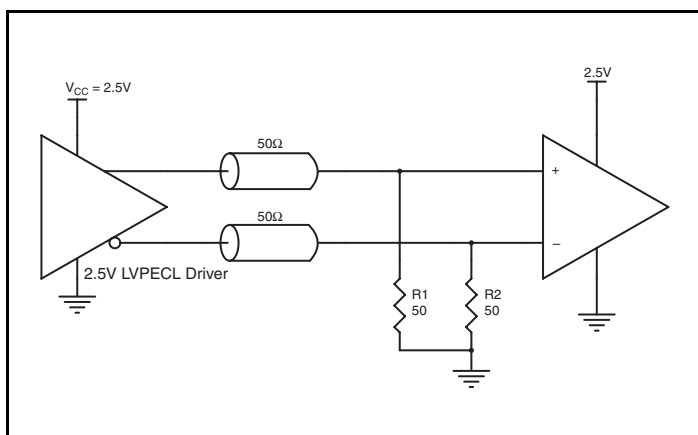


Figure 6C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 7 shows a schematic example of the ICS843002I-40 application schematic. In this example, the device is operated at $V_{CC} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL

driver. The 2-pole filter example is used in this schematic. Please refer to the ICS843002I-40 datasheet for additional loop filter recommendations.

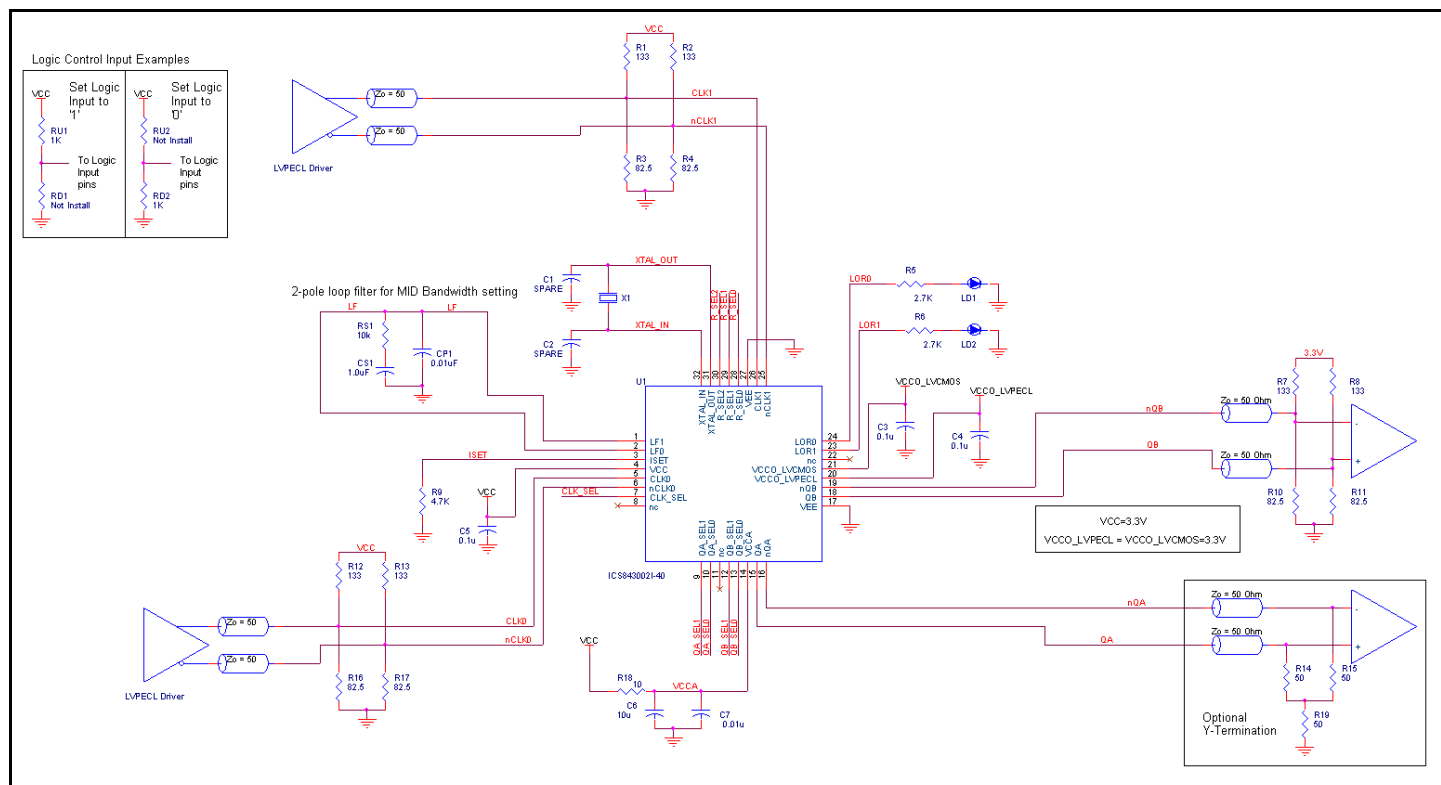


Figure 7. ICS843002I-40 Schematic Example

Loss of Reference Indicator (LOR0 and LOR1) Output Pins

The LOR0 and LOR1 pins are controlled by the internal clock activity monitor circuits. The clock activity monitor circuits are clocked by the VCXO PLL phase detector feedback clock. The LOR output is asserted high if there are three consecutive feedback clock edges without any reference clock edges (in both

cases, either a negative or positive transition is counted as an “edge”). The LOR output will otherwise be low. In a phase detector observation interval, the activity monitor does not flag excessive reference transitions as an error. The monitor only distinguishes between transitions occurring and no transitions occurring.

VCXO-PLL EXTERNAL COMPONENTS

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note*.

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal (C_L) is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is

VCXO Characteristics Table

| Symbol | Parameter | Typical | Units |
|---------------|---------------------------|---------|-------|
| k_{VCXO} | VCXO Gain | 5800 | Hz/V |
| C_{V_LOW} | Low Varactor Capacitance | 12.6 | pF |
| C_{V_HIGH} | High Varactor Capacitance | 24.5 | pF |

VCXO-PLL Loop Bandwidth Selection Table

| Bandwidth | Crystal Frequency (MHz) | R_S (k Ω) | C_S (μ F) | C_P (μ F) | R_{SET} (k Ω) |
|--------------|-------------------------|---------------------|------------------|------------------|-------------------------|
| 10Hz (Low) | 19.44 | 5 | 1.0 | 0.10 | 9.5 |
| 70Hz (Mid) | 19.44 | 10 | 1.0 | 0.01 | 4.75 |
| 100Hz (High) | 19.44 | 15 | 1.0 | 0.01 | 4.75 |

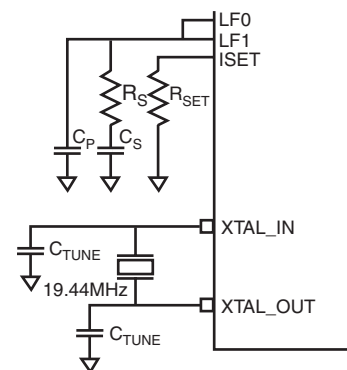
Crystal Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|------------------------------|-----------------|-------------|---------|------------------|--------------|
| | Mode of Oscillation | | Fundamental | | | |
| f_N | Frequency | | | 19.44 | | MHz |
| f_T | Frequency Tolerance | | | | ± 20 | ppm |
| f_S | Frequency Stability | | | | ± 20 | ppm |
| | Operating Temperature Range | | -40 | | +85 | $^{\circ}$ C |
| C_L | Load Capacitance | | | 12 | | pF |
| C_O | Shunt Capacitance | | | 4 | | pF |
| C_O / C_1 | Pullability Ratio | | | 220 | 240 | |
| ESR | Equivalent Series Resistance | | | | 50 | Ω |
| | Drive Level | | | | 1 | mW |
| | Aging @ 25 $^{\circ}$ C | | | | ± 3 per year | ppm |

reduced. The correct value of C_L is dependant on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_S , C_S and C_P values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note*.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843002I-40. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843002I-40 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 210mA = 727.65mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = 60mW$

Total Power_{MAX} (3.3V, with all outputs switching) = $727.65mW + 60mW = 787.65mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.788W * 37^\circ C/W = 114.2^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 48 Lead TQFP, Forced Convection

| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.0°C/W | 32.4°C/W | 29.0°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8*.

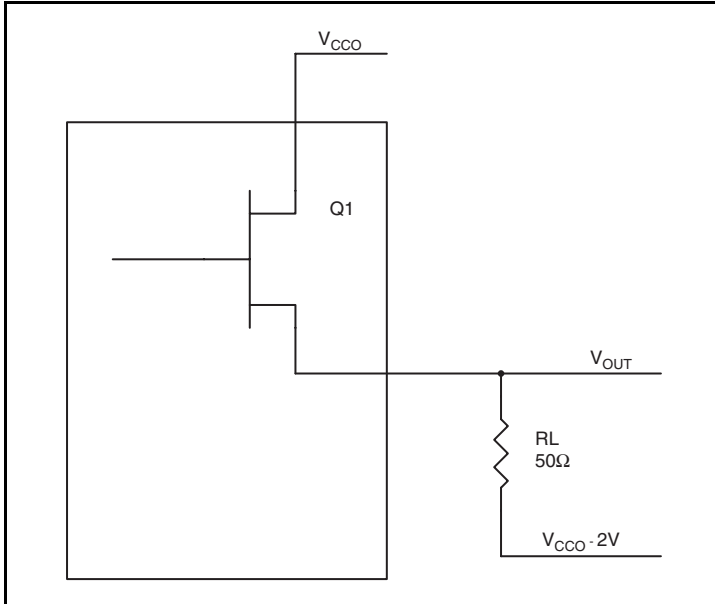


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$
($V_{CCO_MAX} - V_{OH_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$
($V_{CCO_MAX} - V_{OL_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30mW}$$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.0°C/W | 32.4°C/W | 29.0°C/W |

Transistor Count

The transistor count for ICS843002I-40 is: 5536

Package Outline - K Suffix for 32-Lead VFQFN

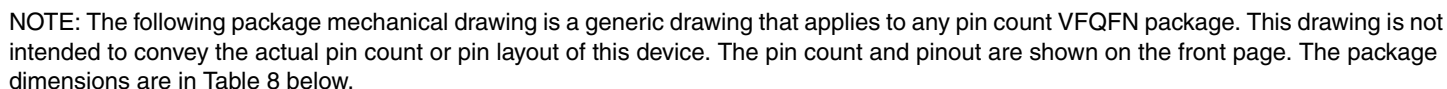


Table 8. Package Dimensions

| JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters | | | |
|---|------------|---------|---------|
| Symbol | Minimum | Nominal | Maximum |
| N | 32 | | |
| A | 0.80 | | 1.00 |
| A1 | 0 | | 0.05 |
| A3 | 0.25 Ref. | | |
| b | 0.18 | 0.25 | 0.30 |
| N_D & N_E | | | 8 |
| D & E | 5.00 Basic | | |
| D2 & E2 | 3.0 | | 3.3 |
| e | 0.50 Basic | | |
| L | 0.30 | 0.40 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|-------------|---------------------------|--------------------|---------------|
| 843002AKI-40 | ICS3002AI40 | 32 Lead VFQFN | Tray | -40°C to 85°C |
| 843002AKI-40T | ICS3002AI40 | 32 Lead VFQFN | 2500 Tape & Reel | -40°C to 85°C |
| 843002AKI-40LF | ICS002AI40L | "Lead-Free" 32 Lead VFQFN | Tray | -40°C to 85°C |
| 843002AKI-40LFT | ICS002AI40L | "Lead-Free" 32 Lead VFQFN | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications, such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|--|---------|
| A | T4B | 6 | LVC MOS DC Characteristics Table - added conditions to V_{OH} and V_{OL} . | 1/22/09 |
| B | T5 | 7 | AC Characteristics Table - changed output skew from 50ps max. to 150ps max. | 4/27/09 |
| | | | | |

ICS843002I-40

175MHZ, FEMTOCLOCKS™ VCXO BASED SONET/SDH JITTER ATTENUATOR

Contact Information:

www.IDT.com

Sales

800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support

netcom@idt.com
+480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)

