

SYSTEM PERIPHERAL CLOCK SOURCE

ICS650-01

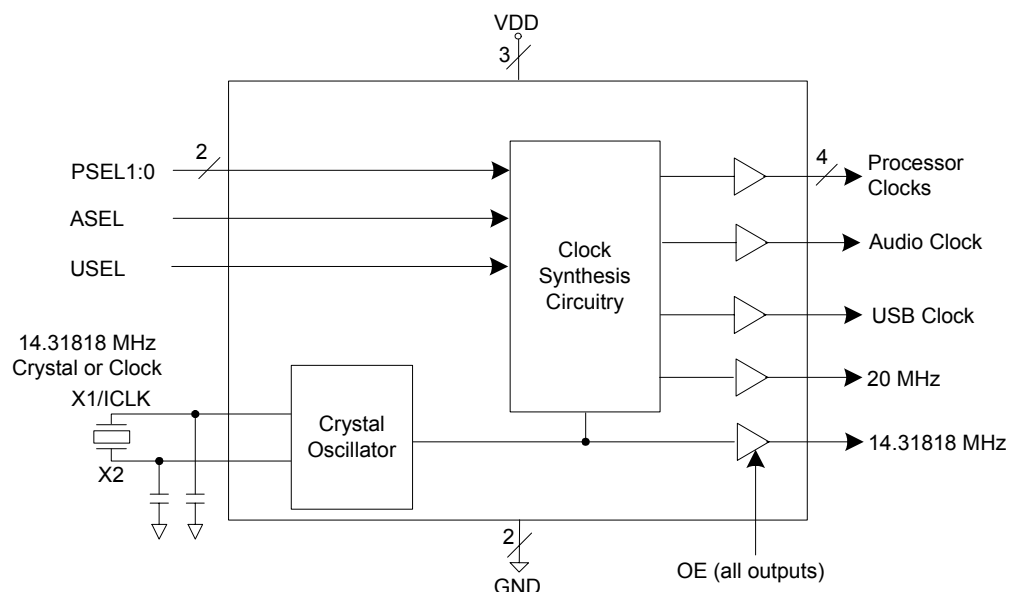
Description

The ICS650-01 is a low-cost, low-jitter, high-performance clock synthesizer for system peripheral applications. Using analog/digital Phase-Locked Loop (PLL) techniques, the device accepts a parallel resonant 14.31818 MHz crystal input to produce up to eight output clocks. The device provides clocks for PCI, SCSI, Fast Ethernet, Ethernet, USB, and AC97. The user can select one of three USB frequencies and also one of two AC97 audio frequencies. The OE pin puts all outputs into a high impedance state for board level testing. All frequencies are generated with less than one ppm error, meeting the demands of SCSI and Ethernet clocking.

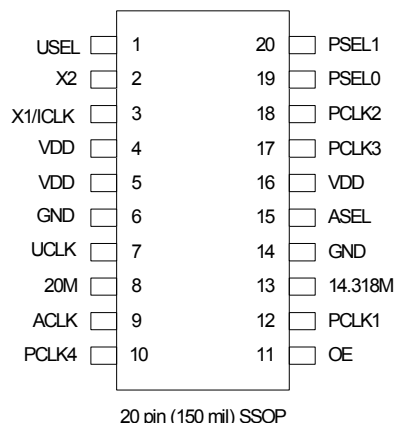
Features

- Packaged in 20-pin SSOP (QSOP)
- Pb (lead) free package
- Operating voltage of 3.3 V or 5 V
- Less than one ppm synthesis error in all clocks
- Inexpensive 14.31818 MHz crystal or clock input
- Provides Ethernet and Fast Ethernet clocks
- Provides SCSI clocks
- Provides PCI clocks
- Selectable AC97 audio clock
- Selectable USB clock
- OE pin tri-states the outputs for testing
- Selectable frequencies on three clocks
- Duty cycle of 40/60
- Advanced, low-power CMOS process
- Industrial temperature range available

Block Diagram



Pin Assignment



USB Clock (MHz)

| USEL | UCLK |
|------|------|
| 0 | 12 |
| M | 24 |
| 1 | 48 |

Processor Clock (MHz)

| PSEL1 | PSEL0 | PCLK1 | PCLK2, 3 | PCLK4 |
|-------|-------|---------------------------------|----------|-------|
| 0 | 0 | 25 | 50 | 18.75 |
| 0 | M | TEST | TEST | TEST |
| 0 | 1 | TEST | TEST | TEST |
| M | 0 | 40 | 80 | 20 |
| M | M | 33.3334 | 66.6667 | 25 |
| M | 1 | 20 | 40 | 25 |
| 1 | 0 | 20 | 33.3334 | 25 |
| 1 | M | 20 | 66.6667 | 25 |
| 1 | 1 | Stops low all clocks except 20M | | |

Audio Clock (MHz)

| ASEL | ACLK |
|------|--------|
| 0 | 49.152 |
| M | 24.576 |
| 1 | 12.288 |

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | USEL | Input | UCLK select pin. Determines frequency of USB clock per table above. |
| 2 | X2 | XO | Crystal connection. Connect to parallel mode 14.31818 MHz crystal. Leave open for clock. |
| 3 | X1/CLK | XI | Crystal connection. Connect to parallel mode 14.31818 MHz crystal or clock. |
| 4 | VDD | Power | Connect to VDD. Must be same value as other VDD. Decouple with pin 6. |
| 5 | VDD | Power | Connect to VDD. Must be same value as other VDD. |
| 6 | GND | Power | Connect to ground. |
| 7 | UCLK | Output | USB clock output per table above. |
| 8 | 20M | Output | Fixed 20 MHz output for Ethernet. Only clock that runs when PSEL1=PSEL0=1. |
| 9 | ACLK | Output | AC97 audio clock output per table above. |
| 10 | PCLK4 | Output | PCLK output number 4 per table above. |

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 11 | OE | Input | Output enable. Tri-states all outputs when low. |
| 12 | PCLK1 | Output | PCLK output number 1 per table above. |
| 13 | 14.318M | Output | 14.31818 MHz Buffered reference clock output. |
| 14 | GND | Power | Connect to ground. |
| 15 | ASEL | Input | ACLK select pin. Determines frequency of Audio clock per table above. |
| 16 | VDD | Power | Connect to VDD. Must be same value as other VDD. Decouple with pin 14. |
| 17 | PCLK3 | Output | PCLK output number 3 per table above. |
| 18 | PCLK2 | Output | PCLK output number 2 per table above. |
| 19 | PSEL0 | Input | Processor select pin #0. Determines frequencies on PCLKs 1-4 per table above. |
| 20 | PSEL1 | Input | Processor select pin #1. Determines frequencies on PCLKs 1-4 per table above. |

External Components

The ICS650-01 requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.01μF must be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line,

as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant, 300 ppm or better (to meet Ethernet specs). Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 12) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 8 pF capacitors should be used. If a clock input is used, drive it into X1 and leave X2 unconnected.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | +3.3 | +5.5 | V |

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5% (or 5 V unless noted)**, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-----------------|--|---------|------|------|-------|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Supply Current | IDD | At 5 V, No load, Note 1 | | 50 | | mA |
| Supply Current | IDD | At 3.3 V, No load, Note 1 | | 30 | | mA |
| Input High Voltage | V _{IH} | Select inputs, OE | 2 | | | V |
| Input Low Voltage | V _{IL} | Select inputs, OE | | | 0.8 | V |
| Output High Voltage | V _{OH} | VDD = 3.3 V, I _{OH} = -8 mA | 2.4 | | | V |
| Output High Voltage | V _{OH} | VDD = 3.3 V or 5 V, I _{OH} = -8 mA | VDD-0.4 | | | V |
| Output Low Voltage | V _{OL} | VDD = 3.3 V, I _{OL} = 8mA | | | 0.4 | V |
| Short Circuit Current | I _{OS} | VDD = 3.3 V, each output | | ±50 | | mA |
| Input Capacitance | | Except X1 | | 7 | | pF |

Note 1: With all clocks at highest frequencies.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5% (or 5 V unless noted)**, Ambient Temperature 0 to +70° C

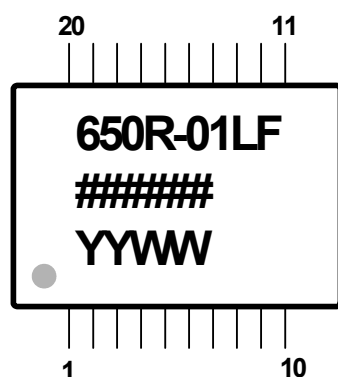
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|----------|----------------------|------|----------|------|-------|
| Input Frequency | | | | 14.31818 | | MHz |
| Output Clocks Accuracy (synthesis error) | | All clocks | | | 1 | ppm |
| Output Rise Time | t_{OR} | 0.8 to 2.0 V, Note 1 | | 1.5 | | ns |
| Output Fall Time | t_{OF} | 2.0 to 0.8 V, Note 1 | | 1.5 | | ns |
| Output Clock Duty Cycle | | At VDD/2 | 40 | 50 | 60 | % |
| One Sigma Jitter | | except ACLK | | 75 | | ps |
| | | ACLK | | 170 | | ps |
| Absolute Clock Period Jitter | | PCLK, UCLK, 20M | -500 | | 500 | ps |

Note 1: Measured with 15 pF load

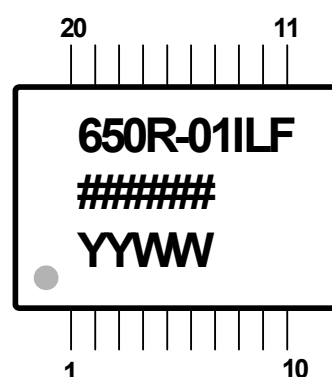
Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 135 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 93 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 78 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 60 | | °C/W |

Marking Diagram—ICS650R-01LF



Marking Diagram—ICS650R-01ILF

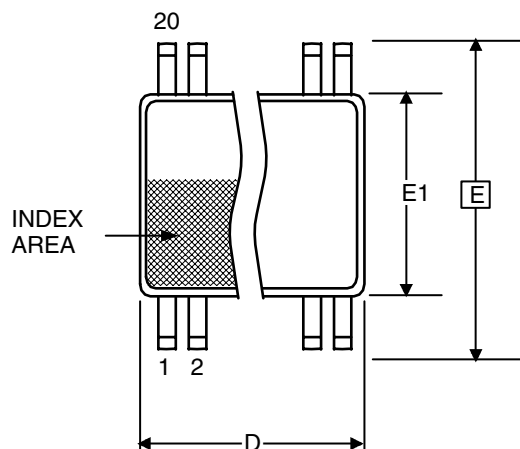


Notes:

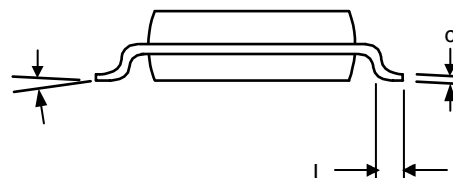
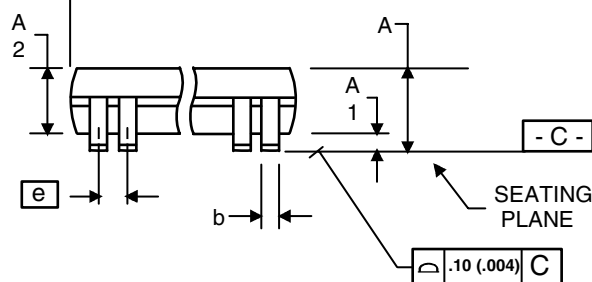
1. ##### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. "LF" denotes Pb (lead) free package.
4. "I" denotes industrial grade device.
5. Bottom marking: (origin) = country of origin if not USA.

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches | |
|----------|-------------|------|------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | -- | 1.50 | -- | 0.059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | .635 Basic | | .025 Basic | |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| α | 0° | 8° | 0° | 8° |



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|-------------|--------------|
| 650R-01LF | see page 6 | Tubes | 20-pin SSOP | 0 to +70° C |
| 650R-01LFT | | Tape and Reel | 20-pin SSOP | 0 to +70° C |
| 650R-01ILF | | Tubes | 20-pin SSOP | -40 to 85° C |
| 650R-01ILFT | | Tape and Reel | 20-pin SSOP | -40 to 85° C |

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