NETWORKING SYSTEM CLOCK ICS650-14

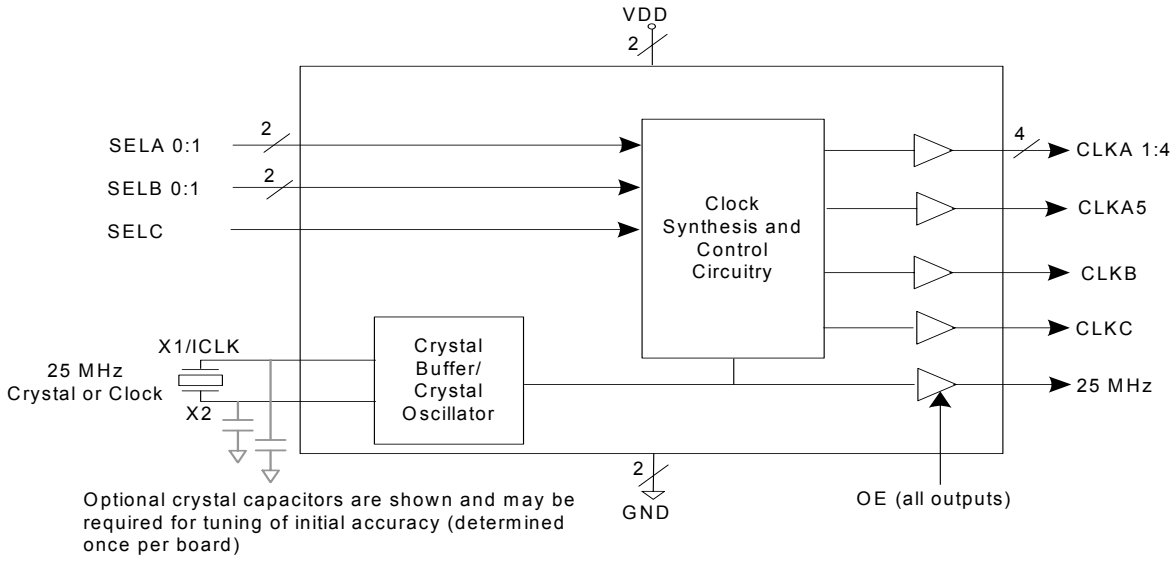
Description

The ICS650-14 is a low-cost, low-jitter, high-performance clock synthesizer customized for networking systems applications. Using analog/digital Phase-Locked Loop (PLL) techniques, the device accepts a 25 MHz clock or fundamental mode crystal input to produce multiple output clocks of one fixed 25 MHz, a four (plus one) frequency selectable bank, and two frequency selectable clocks. All output clocks are frequency locked together. All of the ICS650-14 outputs have zero ppm synthesis error.

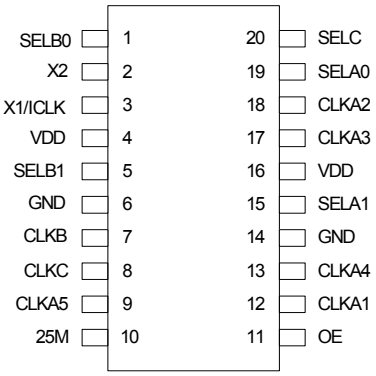
Features

- Packaged in 20-pin (150 mil) SSOP (QSOP)
- 25 MHz fundamental crystal clock or clock input
- One fixed output clock of 25 MHz
- One bank of four frequency selectable output clocks
- Three frequency selectable clocks outputs
- Zero ppm synthesis error in all clocks
- Ideal for networking systems
- Full CMOS output swing
- Advanced, low-power sub-micron CMOS process
- Operating voltage of 3.3 V or 5 V
- Industrial temperature range available
- Pb-free, RoHS compliant package

Block Diagram



Pin Assignment



20-pin (150 mil) SSOP

Table 1

SELA1	SELA0	CLKA1:4	CLKA5
0	0	33.33	66.66
0	M	50	75
0	1	66.67	133.33
M	0	100	33.33
M	M	33.33	83.33
M	1	50	125
1	0	33.33	100
1	M	25	75
1	1	66.67	100

Table 2

SELB1	SELB0	CLKB
0	0	30
0	M	27
0	1	48
1	0	83.33
1	M	19.44
1	1	80

Table 3

SELC	CLKC
0	CLKB/4
M	62.5
1	125

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	SELB0	TI	Select pin for CLKB. See table 2.
2	X2	XO	Crystal connection. Connect to a 25 MHz crystal or leave unconnected for clock input.
3	X1/ICLK	XI	Crystal connection. Connect to a 25 MHz fundamental crystal or clock input.
4	VDD	P	Connect to 3.3 V or 5 V. Must be same as other VDDs.
5	SELB1	I(Pu)	Select pin for CLK B. See table 2.
6	GND	P	Connect to ground.
7	CLKB	O	Selectable clock output. See table 2.
8	CLKC	O	Selectable clock output. See table 3.
9	CLKA5	O	Selectable clock output. See table 1.
10	25M	Ou	25 MHz clock output.
11	OE	I(Pu)	Output enable. Tri-states all outputs when low. Internal pull-up.
12	CLKA1	O	Selectable clock output. See table 1.

Pin Number	Pin Name	Pin Type	Pin Description
13	CLKA4	O	Selectable clock output. See table 1.
14	GND	P	Connect to ground.
15	SELA1	TI	Select pin for CLKA1:4 and CLKA5 outputs. See table 1.
16	VDD	P	Connect to 3.3 Vor 5 V. Must be same as other VDDs.
17	CLKA3	O	Selectable clock output. See table 1.
18	CLKA2	O	Selectable clock output. See table 1.
19	SELA0	TI	Select pin for CLKA1:4 and CLKA5 outputs. See table 1.
20	SELC	TI	Select pin for CLKC output. See table 3.

Key: XI, XO = crystal connections; I = input; I(Pu) = input with pull-up; O = output; P = power supply connection; TI = tri-level input

External Components

The ICS650-14 requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.01µF must be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. For a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-14. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referecned to GND)	7 V
Inputs and Outputs (referecned to GND)	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Ambient Operating Temperature (industrial “I” version)	-40 to 85° C
Soldering Temperature (max. of 20 seconds)	-65 to +150° C
Storage Temperature	260° C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

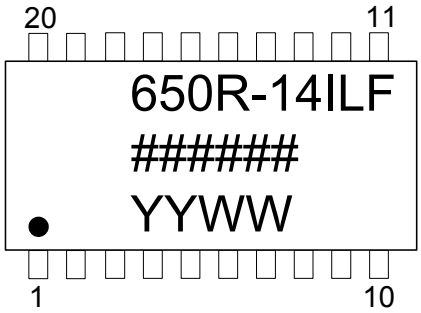
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage (X1 pin only)	V_{IH}	Clock input	VDD/2+1			V
Input Low Voltage (X1 pin only)	V_{IL}	Clock input			VDD/2-1	V
Input High Voltage (SEL pins only)	V_{IH}		VDD-0.5			V
Input Low Voltage (SEL pins only)	V_{IL}				0.5	V
Input High Voltage (OE pin only)	V_{IH}		2.0			V
Input Low Voltage (OE pin only)	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output High Voltage (CMOS level)	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	I_{DD}	No load, VDD = 3.3 V		32		mA
Short Circuit Current		Each output		±50		mA

AC Electrical Characteristics

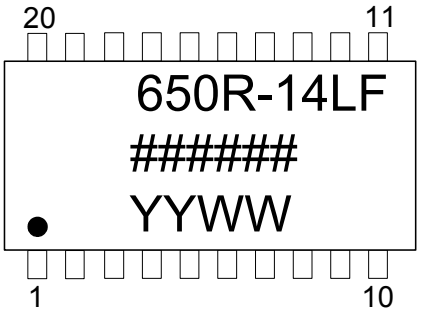
Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		At VDD/2	45	50	55	%
Frequency Error		All clocks			0	ppm
Absolute Jitter, short term		CLKB = 27M		±250		ps
		CLKC = 62.5M		±300		ps
		Other Clocks		±350		ps

Marking Diagram (ICS650R-14ILF)



Marking Diagram (ICS650R-14LF)

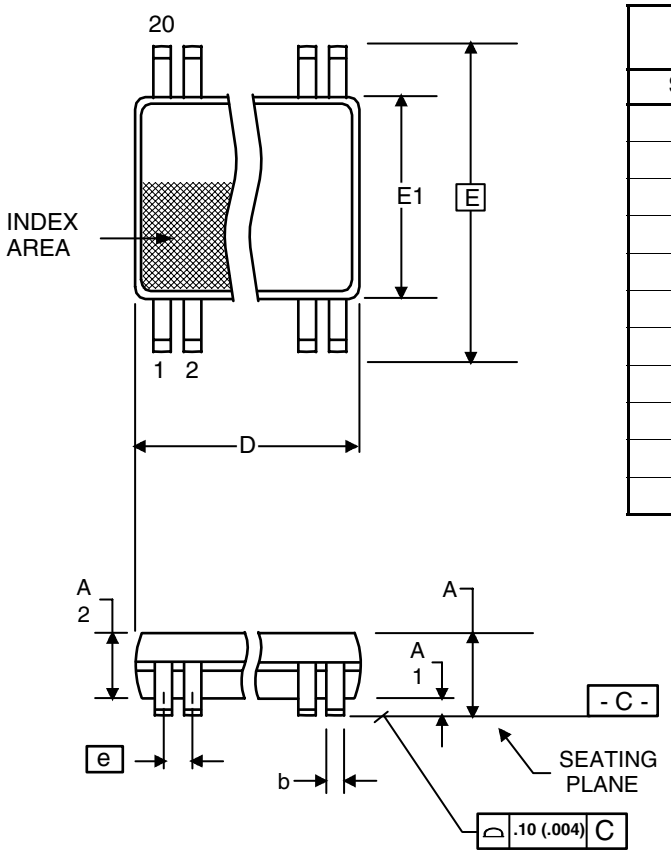


Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. ”LF” denotes Pb-free, RoHS compliant package.
4. “I” denotes industrial grade device.
5. Bottom marking: country of origin.

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	--	1.50	--	0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650R-14LF	see page 5	Tubes	20-pin SSOP	0 to +70° C
650R-14LFT		Tape and Reel	20-pin SSOP	0 to +70° C
650R-14ILF		Tubes	20-pin SSOP	-40 to 85° C
650R-14ILFT		Tape and Reel	20-pin SSOP	-40 to 85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
www.idt.com/go/clockhelp

Corporate Headquarters
Integrated Device Technology, Inc.
www.idt.com

www.IDT.com