500MHz, Crystal-to-3.3V, 2.5V Differential LVPECL Frequency Synthesizer

ICS8430-62

DATASHEET

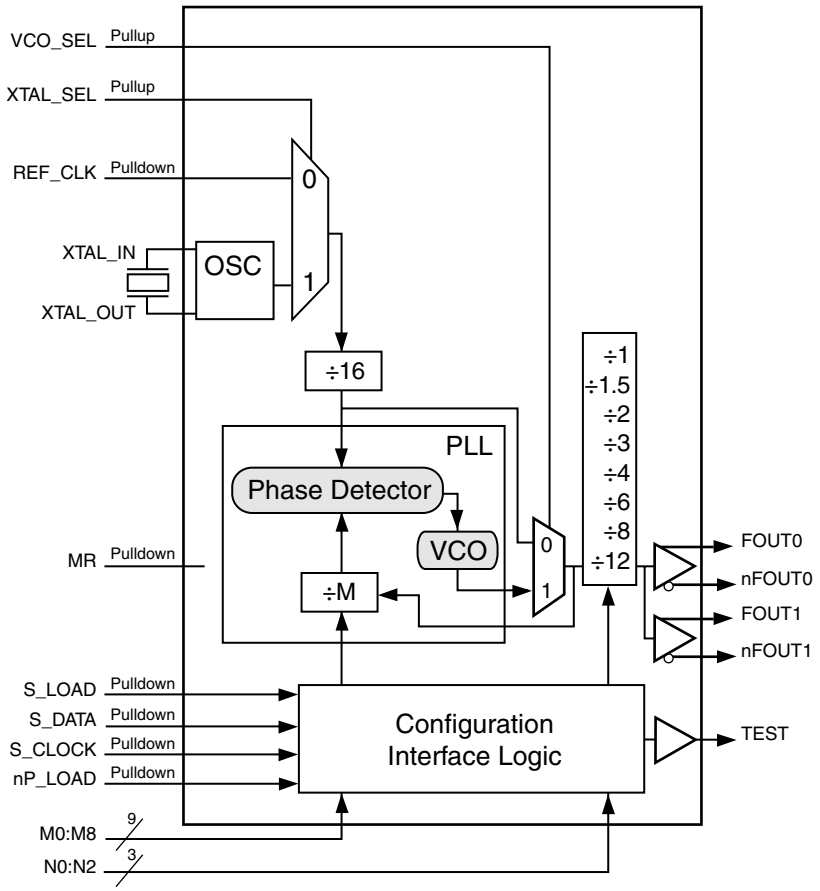
General Description

The ICS8430-62 is a general purpose, dual output Crystal-to-3.3V, 2.5V Differential LVPECL High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8430-62 has a selectable REF_CLK or crystal inputs. The VCO operates at a frequency range of 250MHz to 500MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. Frequency steps as small as 1MHz can be achieved using a 16MHz crystal or REF_CLK.

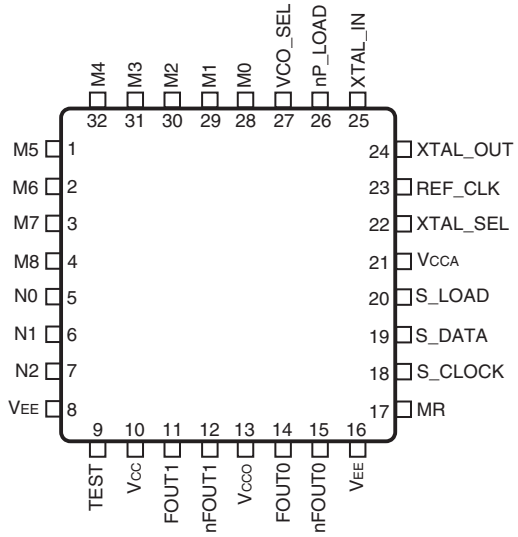
Features

- Dual differential 3.3V or 2.5V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_CLK
- Output frequency range: 20.83MHz to 500MHz
- Crystal input frequency range: 14MHz to 27MHz
- VCO range: 250MHz to 500MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 5ps (maximum)
- Cycle-to-cycle jitter: 35ps (maximum)
- Full 3.3V or 3.3V core/2.5V output supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8430-62
32 Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8430-62 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A parallel-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal, this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 500MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8430-62 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 through N2 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hard-wired to set the M divider and N output divider to a specific default state that will automatically occur during power-up.

The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fXTAL \times M}{16}$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 16MHz reference are defined as $250 \leq M \leq 500$. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fXTAL \times M}{16 \quad N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_DATA, Shift Register Input
1	0	Output of M Divider
1	1	Do Not Use

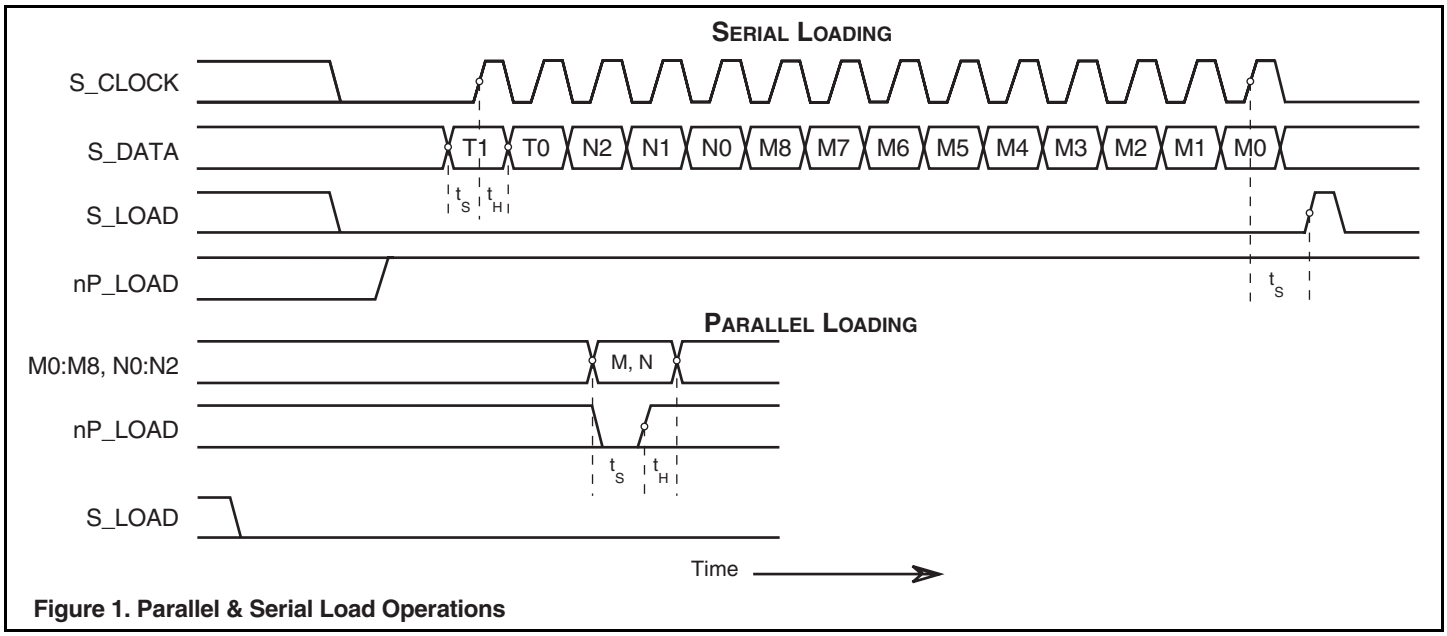


Figure 1. Parallel & Serial Load Operations

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 28, 29, 30, 31, 32	M5, M6, M0, M1, M2, M3, M4	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
3, 4	M7, M8	Input	Pullup	
5, 7	N0, N2	Input	Pulldown	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
6	N1	Input	Pullup	
8, 16	V_{EE}	Power		Negative supply pins.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.
10	V_{CC}	Power		Core supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output pair for the synthesizer. LVPECL interface levels.
13	V_{CCO}	Power		Output supply pin for LVPECL outputs.
14, 15	FOUT0, nFOUT0	Output		Differential output pair for the synthesizer. LVPECL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When Logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS/LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
21	V_{CCA}	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or REF_CLK inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when LOW. LVCMOS/LVTTL interface levels.
23	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
24, 25	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N2:N0 sets the N output divider value. LVCMOS/LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. When LOW, synthesizer is in bypass mode, when HIGH,synthesizer is in PLL mode. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Parallel and Serial Mode Function Table

Inputs							
MR	**nP_LOAD**	**M**	**N**	**S_LOAD**	**S_CLOCK**	**S_DATA**	**Conditions**
H	X	X	X	X	X	X	Reset. Forces true outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	**M7**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	**M0**
250	250	0	1	1	1	1	1	0	1	0
251	251	0	1	1	1	1	1	0	1	1
252	252	0	1	1	1	1	1	1	0	0
253	253	0	1	1	1	1	1	1	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
498	498	1	1	1	1	1	0	0	1	0
499	499	1	1	1	1	1	0	0	1	1
500	500	1	1	1	1	1	0	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to a REF_CLK or crystal frequency of 16MHz.

Table 3C. Programmable Output Divider Function Table

Inputs			N Divider Value	Output Frequency (MHz)	
N2	N1	N0		Minimum	Maximum
0	0	0	1	250	500
0	0	1	1.5	166.66	333.33
0	1	0	2	125	250
0	1	1	3	83.33	166.66
1	0	0	4	62.5	125
1	0	1	6	41.66	83.33
1	1	0	8	31.25	62.5
1	1	1	12	20.83	41.66

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	65.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{CCO} = 3.3V±5% or 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.14	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current				14	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5%, V_{CCO} = 3.3V±5% or 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	M[0:6], N0, N2, MR, S_CLOCK, REF_CLK, S_DATA, S_LOAD, nP_LOAD	V_{CC} = V_{IN} = 3.465V			150	µA
		M7, M8, N1, XTAL_SEL, VCO_SEL	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	M[0:6], N0, N2, MR, S_CLOCK, REF_CLK, S_DATA, S_LOAD, nP_LOAD	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		M7, M8, N1, XTAL_SEL, VCO_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1	V_{CCO} = 3.3V±%	2.6			V
			V_{CCO} = 2.5V±5%	1.8			V
V_{OL}	Output Low Voltage	TEST; NOTE 1	V_{CCO} = 3.3V±5% or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO}/2. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4C. LVPECL DC Characteristics, V_{CC} = V_{CCO} = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CCO} – 1.4		V_{CCO} – 0.9	µA
V_{OL}	Output Low Current; NOTE 1		V_{CCO}– 2.0		V_{CCO} – 1.7	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V±5%, V_{CCO} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CCO} – 1.4		V_{CCO} – 0.9	µA
V_{OL}	Output Low Current; NOTE 1		V_{CCO}– 2.0		V_{CCO} – 1.5	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 5. Input Characteristics, V_{CC} = 3.3V±5%, V_{CCO} = 3.3V±5% or 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	REF_CLK; NOTE 1		14		27	MHz
		XTAL_IN, XTAL_OUT; NOTE 1		14		27	MHz
		S_CLOCK				50	MHz
t_R / t_F	Input Rise/Fall Time	REF_CLK				5	ns
		S_CLOCK, S_DATA, S_LOAD			6		ns
		nP_LOAD				50	ns

NOTE 1: For the input crystal and REF_CLK frequency range, the M value must be set for the VCO to operate within the 250MHz to 500MHz range. Using the minimum input frequency of 14MHz, valid values of M are 286 ≤ M ≤ 511. Using the maximum input frequency of 27MHz, valid values of M are 149 ≤ M ≤ 296.

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		27	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 7A. AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			20.83		500	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2		N ≠ 1.5			35	ps
			N = 1.5			200	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1		N ≠ 1.5			5	ps
*t*sk(o)	Output Skew; NOTE 2, 3					20	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		Even N Dividers	48		52	%
			Odd N Dividers	43		57	%
t_{LOCK}	PLL Lock time					10	ms

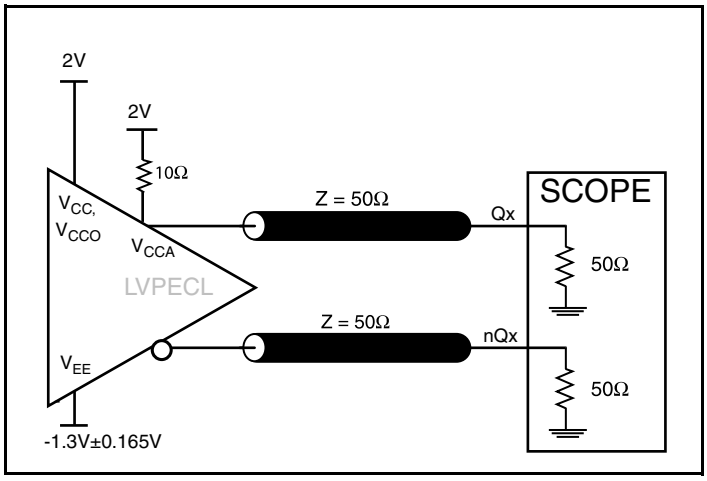
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.

Table 7B. AC Characteristics, V_{CC} = 3.3V±5%, V_{CCO} = 2.5V±5%, T_A = 0°C to 70°C

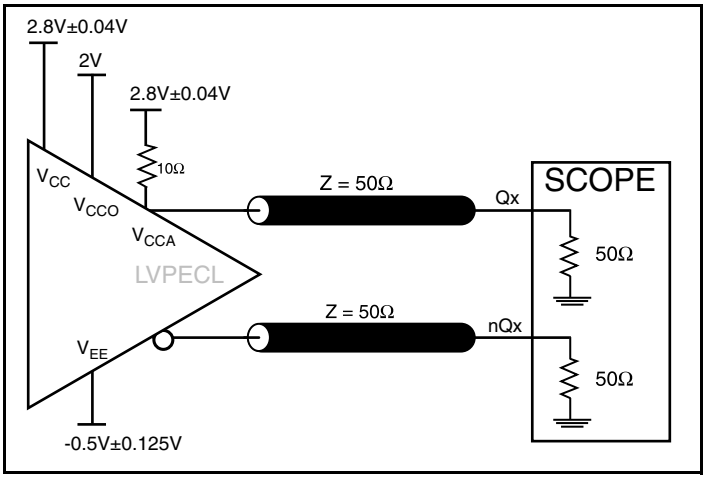
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			20.83		500	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2		N ≠ 1.5			35	ps
			N = 1.5			200	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1		N ≠ 1.5			6	ps
*t*sk(o)	Output Skew; NOTE 2, 3					20	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		Even N Dividers	48		52	%
			Odd N Dividers	43		57	%
t_{LOCK}	PLL Lock time					10	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.

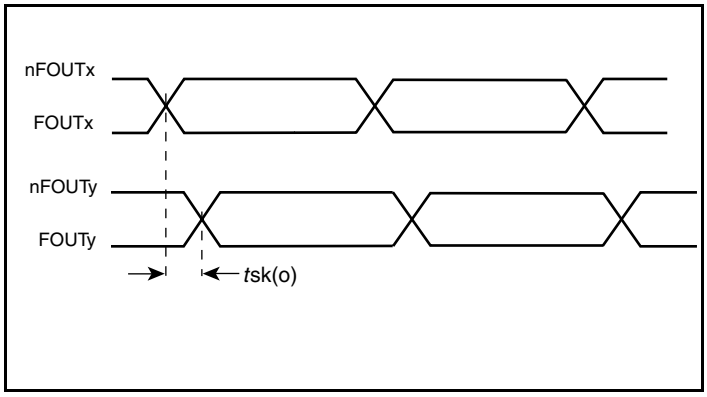
Parameter Measurement Information



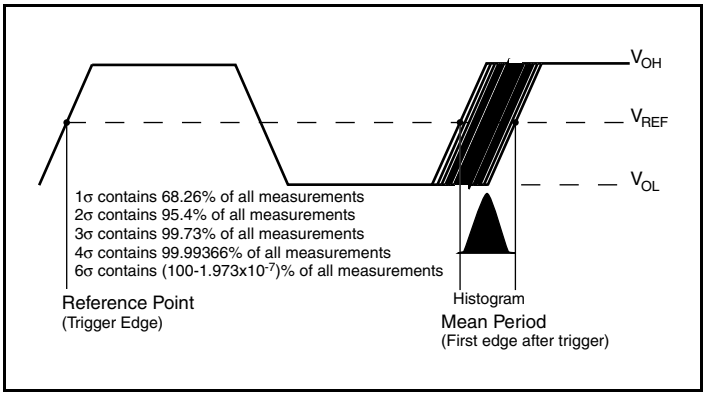
3.3/3.3V LVPECL Output Load AC Test Circuit



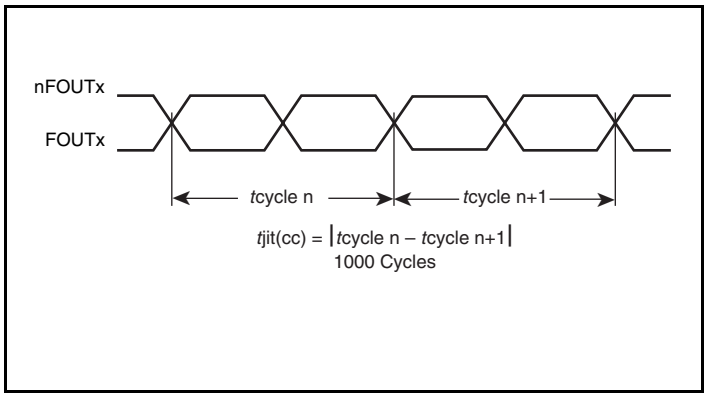
3.3V/2.5V LVPECL Output Load AC Test Circuit



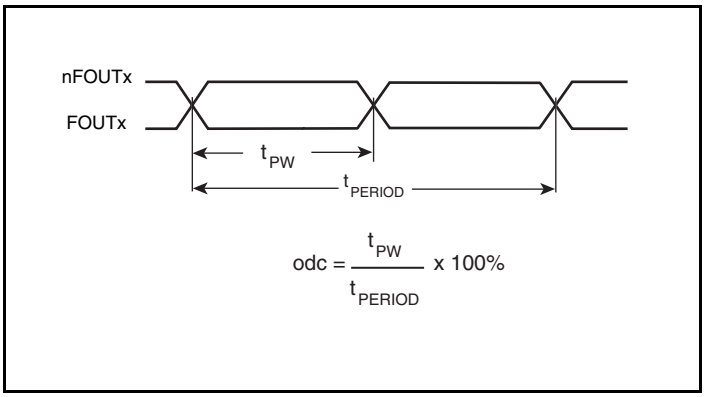
Output Skew



Period Jitter

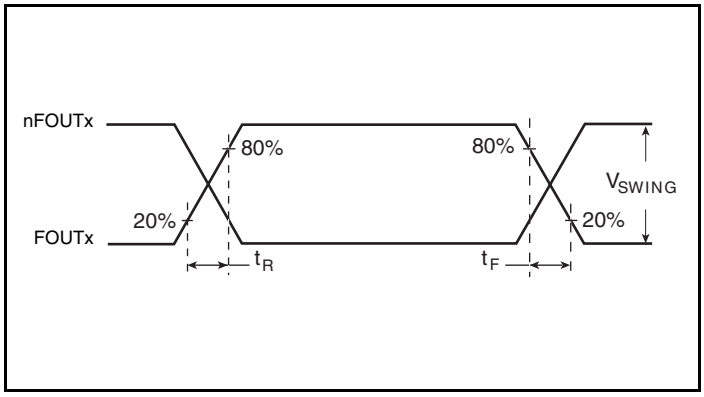


Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8430-62 provides separate power supplies to isolate any high frequency switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

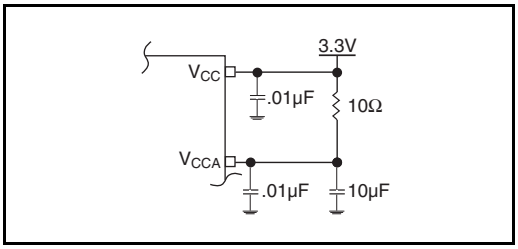


Figure 2. Power Supply Filtering

Crystal Input Interface

The ICS8430-62 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

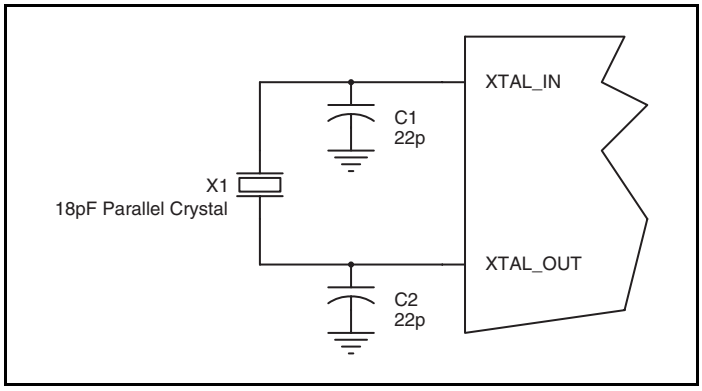


Figure 3. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

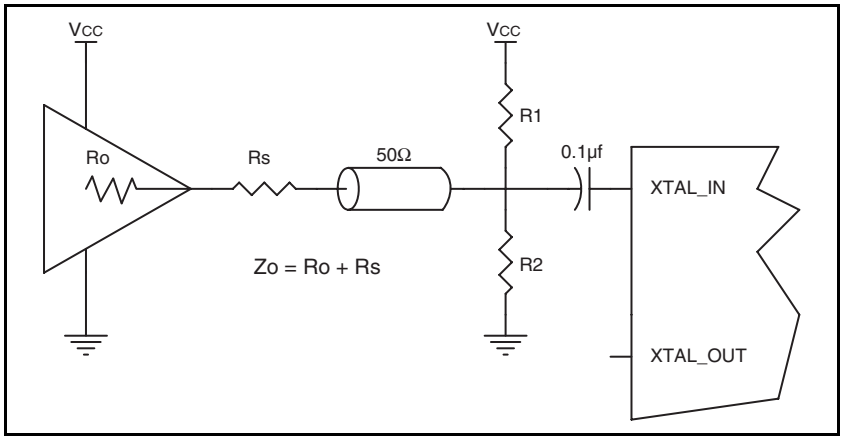


Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

TEST Output

The unused TEST output can be left floating. There should be no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

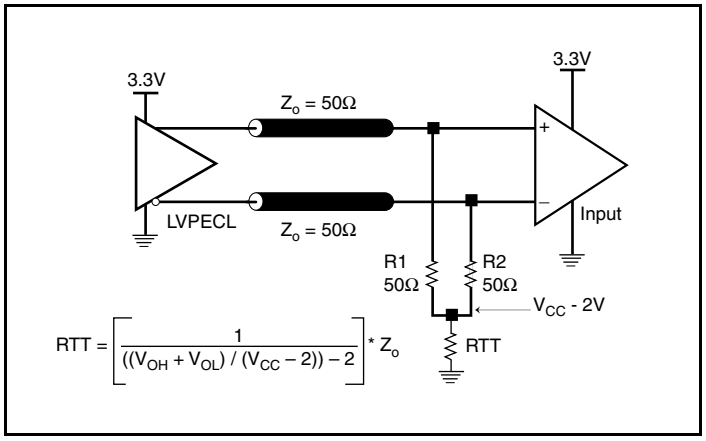


Figure 5A. 3.3V LVPECL Output Termination

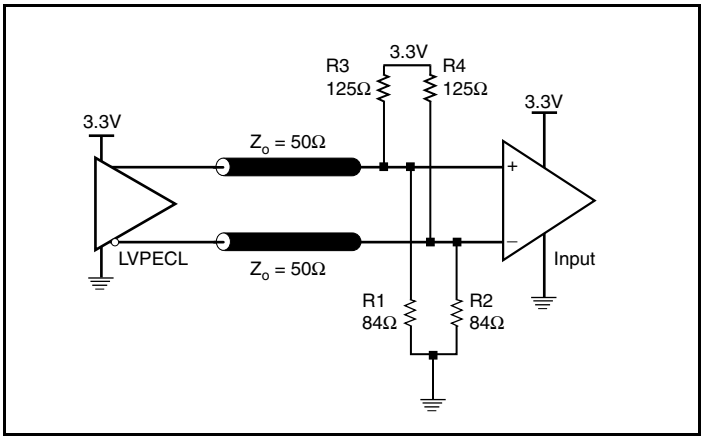


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

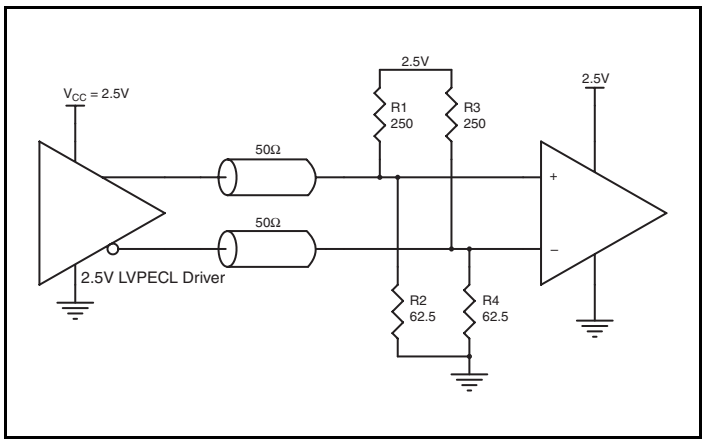


Figure 6A. 2.5V LVPECL Driver Termination Example

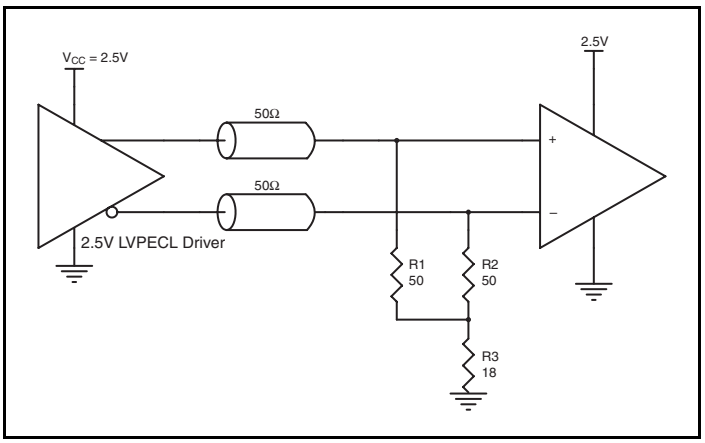


Figure 6B. 2.5V LVPECL Driver Termination Example

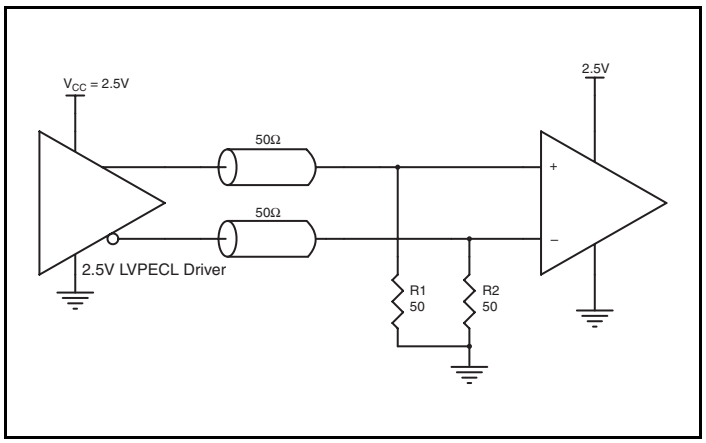


Figure 6C. 2.5V LVPECL Driver Termination Example

Schematic Example

The schematic of the ICS8430-62 layout example used in this layout guideline is shown in *Figure 7A*. The ICS8430-62 recommended PCB board layout for this example is shown in *Figure 7B*. This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

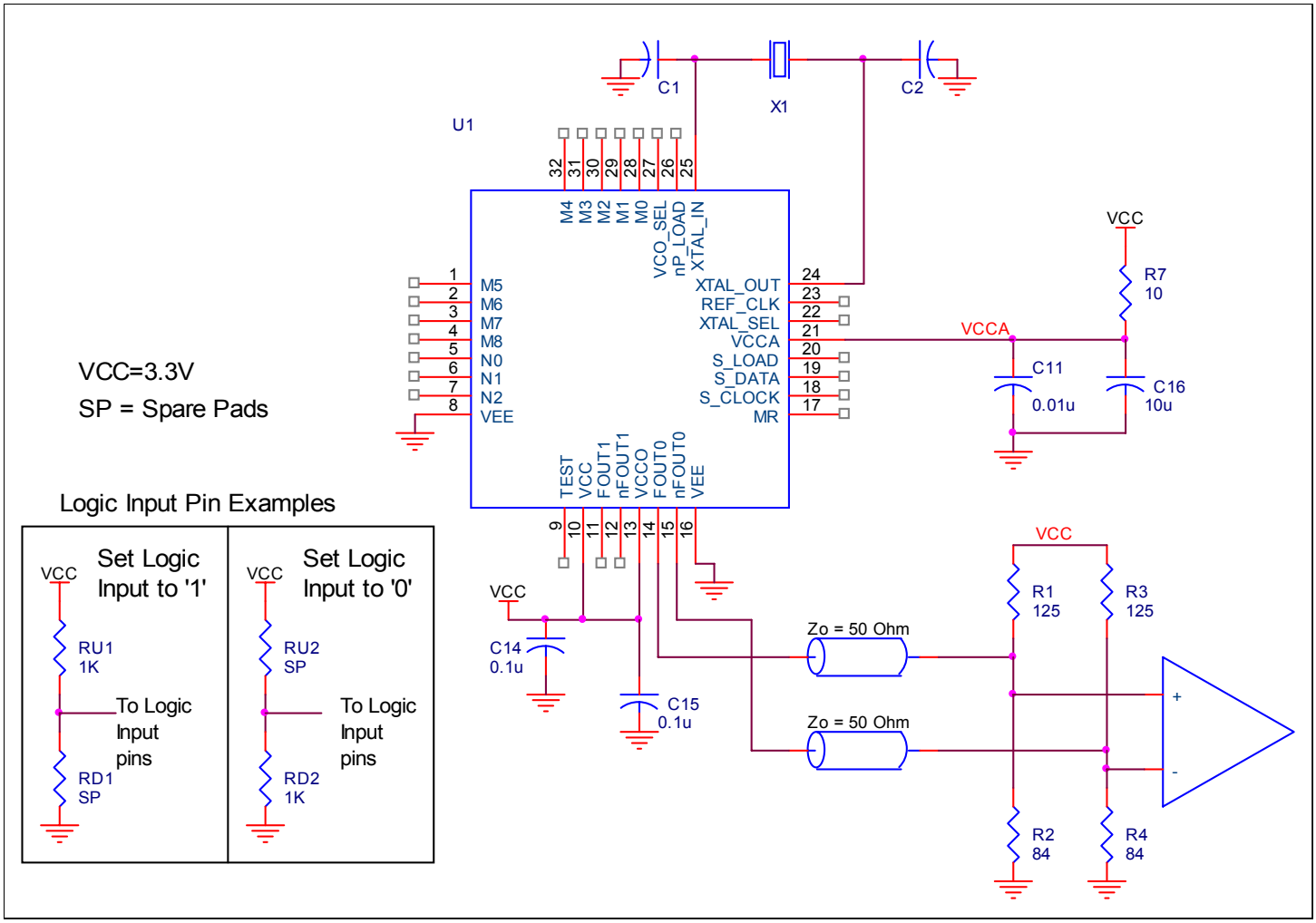


Figure 7A. ICS8430-62 Schematic of Recommended Layout

The following component footprints are used in this layout example. All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C14 and C15, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the pad size of the power (ground) at the decoupling capacitor. Maximize the number of vias between power (ground) and the pads. This can reduce the inductance between the power (ground) plane and the component power (ground) pins.

If V_{CCA} shares the same power supply with $V_{CC,}$ insert the RC filter R7, C11, and C16 in between. Place this RC filter as close to the V_{CCA} pin as possible.

Clock Traces and Termination

The component placements, locations and orientations should be arranged to achieve the best clock signal quality. Poor clock signal quality can degrade the system performance or cause system failure. In the synchronous high-speed digital system, the clock signal is less tolerable to poor signal quality than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The trace shape and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The traces with 50Ω transmission lines TL1 and TL2 at FOUT and nFOUT should have equal delay and run adjacent to each other. Avoid sharp angles on the clock trace.Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock trace on the same layer. Whenever possible, avoid any vias on the clock traces. Any via on the trace can affect the trace characteristic impedance and hence degrade signal quality.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow more space between the clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination schemes can also be used but are not shown in this example.

Crystal

The crystal X1 should be located as close as possible to the pins 24 (XTAL_OUT) and 25 (XTAL_IN). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

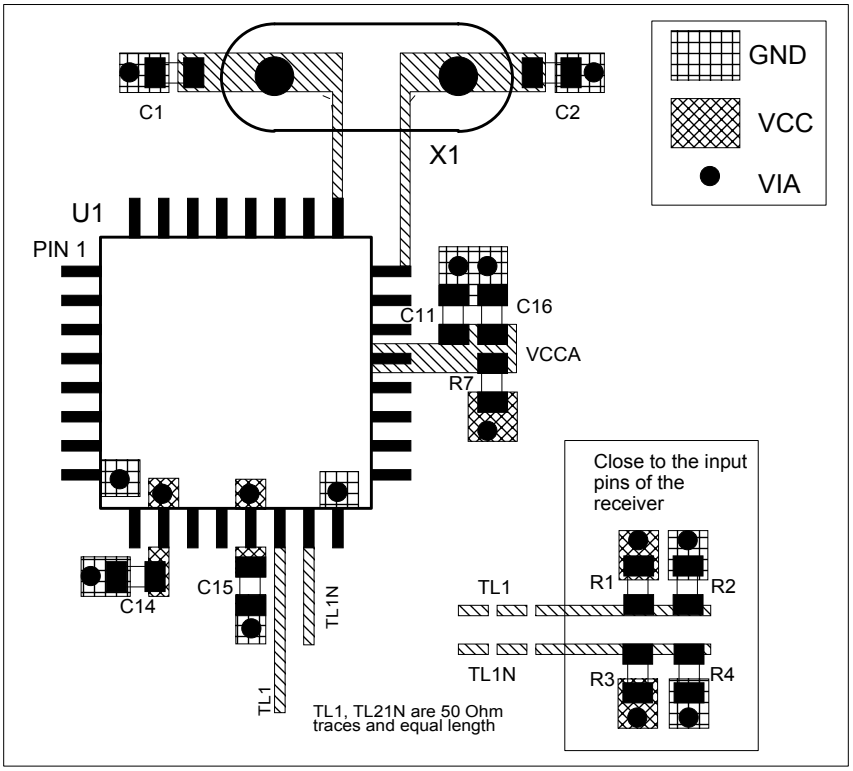


Figure 7B. PCB Board Layout for ICS8430-62

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8430-62.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8430-62 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 130mA = **450.45mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 450.45mW + 60mW = **510.45mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.510W * 65.7°C/W = 103.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

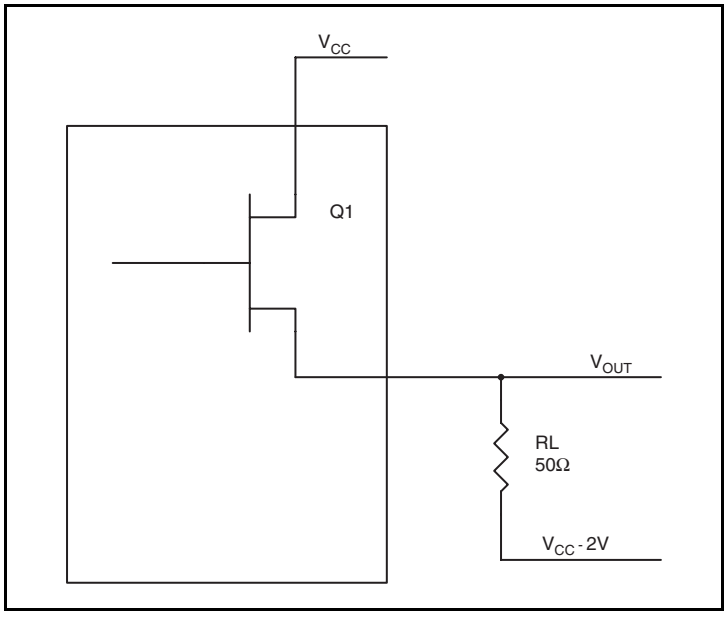


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.9V**
  ($V_{CCO\_MAX} – V_{OH\_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.7V**
  ($V_{CCO\_MAX} – V_{OL\_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

Transistor Count

The transistor count for ICS8430-62 is: 4258

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

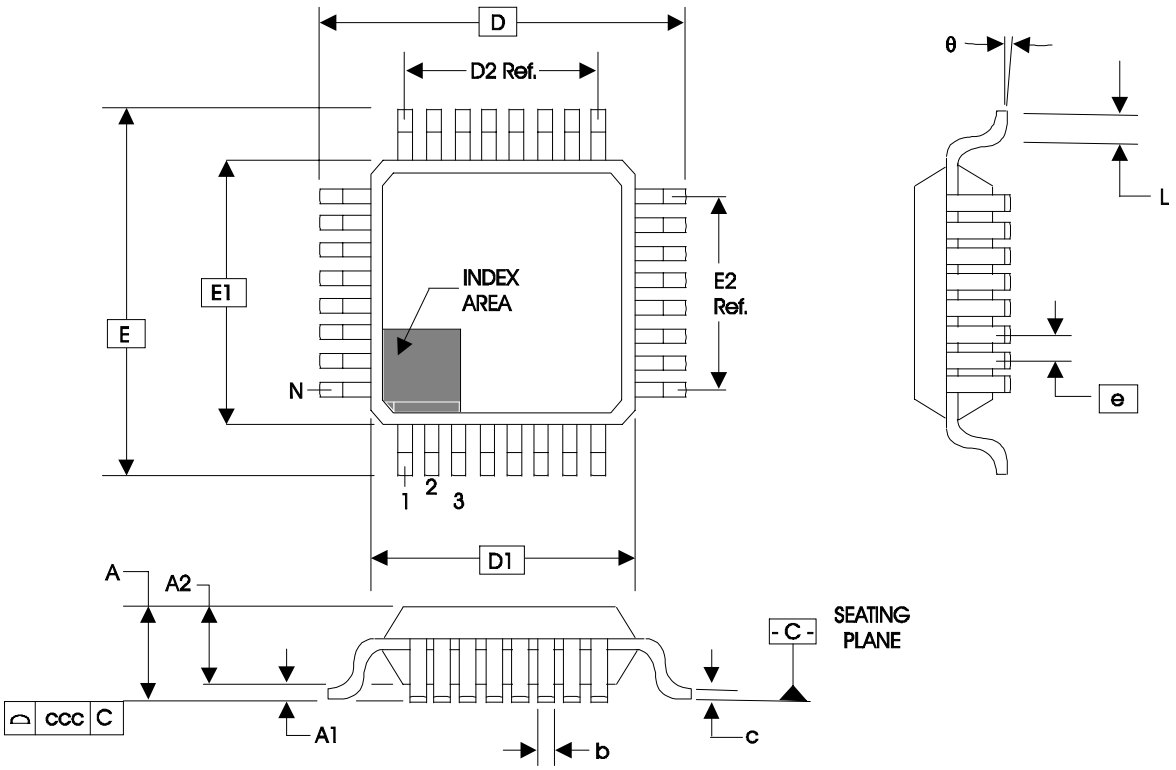


Table 10. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8430AY-62	ICS8430AY-62	32 Lead LQFP	Tray	0°C to 70°C
8430AY-62T	ICS8430AY-62	32 Lead LQFP	1000 Tape & Reel	0°C to 70°C
8430AY-62LF	ICS8430AY62L	“Lead-Free” 32 Lead LQFP	Tray	0°C to 70°C
8430AY-62LFT	ICS8430AY62L	“Lead-Free” 32 Lead LQFP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Block Diagram - output labels were cut-off.	7/2/09

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